

Intel® PRO/10/100/1000/10000 Software Release 16.1
Intel® Boot Agent

Production Version

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Project Component Comparison

Contents	Page
Intel Gigabit Boot Agent	3
Intel 10 GbE PCIe Boot Agent	12
Intel 10/100 Boot Agent	18
Intel 10 GbE PCI-X Boot Agent (obsolete)	19

Intel Gigabit Boot Agent change log

Version 1.3.72

Defect Details:

PXE 82580 fails link using 2/3-pair downshift cable

Root Cause:

Downshift code did not check specifically for 82580 and so was not detecting cable energy status correctly.

Resolution Notes:

Added code to detect PHY cable energy status and wait for downshift if necessary

Defect Details:

82571: Behavior of SPI EEPROM Signals (EE_CS_N, EE_SK, EE_DI) during reset

Root Cause:

BMC reset of system during PXE EEPROM reads may leave EECD.REQ bit set, preventing SW and HW from reading the 82571 EEPROM after the reboot.

Resolution Notes:

Added code to ensure the REQ and GNT bits are cleared in EECD register before the first EEPROM operation.

Defect Details:

82579: PXE Boot fails with 2 or 3 pair cable

Root Cause:

Code to detect and handle PCH2 was omitted from the downshift section of the UNDI driver.

Resolution Notes:

Added code to detect PCH2 downshift status and wait if necessary.

Version 1.3.71

Defect Details:

BootUtil:-IV Command Displays "development Build -Not For Production Use ***Alpha-1"

Root Cause:

NEWHW option used while building BootROM_PXE_Gigabit component

Resolution Notes:

Built component without NEWHW option set.

Version 1.3.70

Change Details:

Add i350 silicon Support

Changes Made:

Added support for i350 silicon. Built with new version of assembly shared code.

Defect Details:

APITEST cannot get IP over DHCP

Root Cause:

Tail register initialization was missing in NICRxEnable UNDI call. This bug was introduced during last changes in UNDI.

Resolution Notes:

Added Tail register initialization to RxEnable function

Version 1.3.65

Change Details:

Support For New PBA EEPROM Format

Changes Made:

Changes in asm shared code (ported e1000_read_pba_string), refactored PXE setup code to use new e1000_read_pba_string.

Version 1.3.64

Defect Details:

LED and Link speed is not properly configured by IBA (PXE driver)

Resolution Notes:

The latest shared code changes implemented in assembly shared code.

Defect Details:

Add support for C0 stepping of the 82579 in PreBoot components

Resolution Notes:

The latest shared code changes ported to assembly shared code

Defect Details:

82576 PXE Failed Issue

Root Cause:

The problem is connected to receiver re-initialization routine and is strictly related to 82575/82576 hardware. In heavy loaded network environment improper receiver state can occur that drives receiver queue to stop. In this state Tail and Head registers point to the same location in descriptor queue (let's say "n"), status values for all the descriptors are equal to zero (which means all the descriptors are freed), RxTail (read index variable) points to location "n+1". This is erroneous situation in which hardware cannot write to queue, because Tail==Head condition means there are no free descriptors. Software doesn't read from queue, because current location pointed by RxTail has descriptor.status == 0, which means there are no new packets written by hardware.

The source of the problem is located in "NICOpenAdapter" function, that is called to initialize Rx/Tx on adapter. The relevant part of this function consists of the following steps:

....

1. Enable receive unit
2. Set Tail register to maximum possible value = 7
3. Enable transmit unit

....

After step 1 hardware immediately starts writing to receive queue. In current implementation value of Head register is accidental at this point. If initial value of Head register is close or equal to 7 (5, 6, 7) it is possible that hardware crosses location 7 and starts writing from 0 before Tail register is set to 7. It is improper situation and it can seldom lead to deadlock condition described above.

Resolution Notes:

Assembly functions NICOpenAdapter(), RxDisable() and RxEnable() have been modified to correct receive queue issue.

Version 1.3.63

Defect

Details:

PXE file transfer significantly slow on 82579 based platform

Root Cause:

PXE code negotiated link to 10MB. Reason for that was assembly shared code in version 2.17 didn't clear OEM config HV_OEM_BITS_LPLU and HV_OEM_BITS_GBE_DIS in PHY register and don't restart PHY autonegotiation after reset.

Resolution Notes:

Fixed in asm shared code 2.19; added new function e1000_oem_bits_config that clears LPLU and GBE_DIS bits in PHY_CTRL register, and restarts PHY autonegotiation.

Version 1.3.62

Change

Details:

82580 Fiber NIC Support

Brief Description:

Support for device 1527 (82589 Fiber)

Changes Made:

Added support for device 1527 (82580 Fiber)

Version 1.3.53

Change Details:

Support for ICH10D+82567V MAC / PHY combination

Brief Description:

New device ID (1525)

Changes Made:

Changes device id in dev_list.inc, new version in i8254x.inc.

No changes in asm shared code because device id exist there already

Version 1.3.52

Defect

Details:

Driver fix for 82576 serdes energy detect bit needs to be ported to PXE

Root Cause:

Assembly code copied shared C code which erroneously configured energy detect unconditionally.

Resolution Notes:

Removed the code that set energy detect, allowing it to be configured via EEPROM.

Defect

Details:

PXE boot cannot work after PC reboots.

Root Cause:

Windows driver change added in 14.8.3 caused PXE to be unable to boot on Calpella non-mgmt SKU after Windows shutdown with NDIS driver loaded.

Resolution Notes:

Added shared code update to restore PHY bus connectivity prior to initializing link; this undoes the NDIS driver shutdown PHY processing.

Version 1.3.51

Defect

Details:

IBA 1.3.36 and newer can't get PXE boot menu from some PXE servers.

Root Cause:

Code added to version 1.3.36 to resolve an earlier issue (PXE boot fails if DHCP option 43 is present but option 60 is not) broke the ability of the base code to handle multiple copies of option 43, which is required in the case of very large PXE boot menus

Resolution Notes:

Modified the code to remove the order dependency between options 43 and 60 that required the original 1.3.36 changes; this restored the ability to process multiple option 43s without bringing back the original issue

Version 1.3.50

Details:

Add 82580 Si Support

Brief Description:

82580 Si Support

Changes Made:

82580 Si Support

Version 1.3.50 Beta 3

Defect

Details:

Cannot flash Intel(R) Ethernet Server Adapter I340-T2 via IBAUTIL after enabling

Root Cause:

The PXE init code that determines if an I/O BAR is present was not working correctly with 32-bit BARs. This forced PXE to use the PCI config space access method, which had a separate bug that could write the wrong value to the PCI config space, potentially corrupting the PCI configuration and preventing normal access to the adapter EEPROM and flash space.

Resolution Notes:

Corrected both bugs to correctly detect 32-bit I/O BARs and to use the correct values when accessing the PCI config space to do I/O.

Version 1.3.50 Beta 2

Defect

Details:

Preboot utility sometimes cannot modify EEPROM bits

Root Cause:

PXE could incorrectly modify the PCI configuration space of the adapter (or even other devices) due to misinterpreting the 32-bit BAR contents and using invalid configuration data.

Resolution Notes:

Modified the code to correctly handle 32-bit BARs and use the correct value when performing I/O using the PCI config space method

Version 1.3.40

Defect

Details:

IBA 1.3.39 fails with 2/3 pair cable

Root Cause:

Shared code changes to increase gigabit link retries caused PXE to timeout too soon during a 10/100 downshift on 82577.

Resolution Notes:

Added code to detect cable presence and if found to be connected, wait for the downshift to complete.

Version 1.3.39

Defect

Details:

PXE fails to connect

Root Cause:

Assembly shared code was not reading wakeup register during HW reset on 82577 due to porting error from C shared code

Resolution Notes:

Removed PHY type check and always read the register for 82577. Also modified the link downshift configuration to improve link-up performance.

Version 1.3.38

Defect

Details:

DOS and PXE drivers do not function well at 10/100 speeds

Root Cause:

PHY tuning changes for HV NVM changes appear to conflict with other HV workarounds in assembly shared code but only at speeds below gigabit

Resolution Notes:

Removed the PHY tuning code and reordered the K1 disable to occur after the PHY is reset

Version 1.3.37

Change

Brief Description:

Added shared code changes for configuring 82577/82578 from NVM during reset

Changes Made:

Ported HV configuration workaround from shared code 3.1.10.2_Release15.1

Silicon Code Name and Stepping:

PCH B3

Change

Details:

Added 82576NS SerDes SKU

Brief Description:

Added 82576NS SerDes SKU

Changes Made:

Added device ID 1518

Version 1.3.36

Defect

Details:

PXE fails when GPI29 WOL enabled on Kingscreek platform

Root Cause:

The issue appears to be caused by code which disables and enables gigabit connectivity around reading the PHY wakeup registers as part of the receive stall workaround.

Resolution Notes:

Removed the code that modified the PHY_CTRL register gigabit setting before and after the wakeup register access.

Defect

Details:

Link is not detected on PRO/1000 MF Server Adapter with IBA 1.3.27

Root Cause:

PHY address was not initialized due to HV changes

Resolution Notes:

Added code to initialize the PHY address for 82545 and 82546 before use

Defect

Details:

PXE boot fails if option 43 is enabled

Root Cause:

DHCP option parsing code assumed that any option 43 data was for PXE when that is not the case

Resolution Notes:

Made option 43 parsing conditional on receiving correct option 60 value as well

Change

Details:

Change completion timeout values when left at default in order to minimize data corruption risk in 82575/82576

Brief Description:

Change completion timeout values when left at default in order to minimize data corruption risk in 82575/82576

Changes Made:

Implemented required shared code changes

Defect

Details:

IBA 1.3.35 PV fails to connect with PXE-E61: Media test failure

Root Cause:

The SW flag semaphore routines were not completely ported from the C code, causing a failure to acquire the semaphore when AMT is active.

Resolution Notes:

Updated the routines to correctly implement the required semaphore algorithm.

Version 1.3.35

New Feature

Feature Description:

- Added Calpella/Piketon support

Changes Made:

- Calpella/Piketon shared code changes ported and integrated

Version 1.3.35 Beta 4

Details

Brief Description:

K1 power mode may cause data corruption if enabled at non-gigabit speeds

Changes Made:

Disable K1 power mode after reset

Silicon Code Name and Stepping:

PCH

Version 1.3.35 Beta 3

Defect

Details:

82574 NIC option ROMs hang the system at boot

Root Cause:

Code added common file to fix an 82599 issue causes the wrong flash address to be used when loading code from the NIC into memory

Resolution Notes:

Removed the 82599 fix code in the gigabit build

Version 1.3.35 Beta 2

New Feature

Feature Description:

Updated Calpella/Piketon support

Changes Made:

Added 14.1 shared code changes

Version 1.3.35 Beta 1

Change

Details:

Calpella platform LAN support

Brief Description:

Calpella platform LAN support

Changes Made:

New shared code port

Version 1.3.32

Defect

Details:

82576 LOM unable to PXE boot

Root Cause:

82576 serdes implementation was incomplete

Resolution Notes:

Added needed checks for 82576 and added extra delays after initializing the PCS link to allow autonegotiation to complete

Defect

Details:

PXE (IBA) hang while establishing link

Root Cause:

Porting error from original 82541/82547 shared code enabled a possible infinite loop while configuring the DSP after link is up

Resolution Notes:

Modified affected code to only run on selected 82541/82547 silicon and also corrected the infinite loop.

Defect

Details:

Initial update of NVM on ICH/PCH systems could take much longer than subsequent updates

Root Cause:

Software flag synchronization register may not be functioning correctly on initial boot

Resolution Notes:

Removed use of the register since it is not really needed in single-threaded PXE environment

Version 1.3.31

Details:

Spurious NVM checksum errors on ICH9 systems

Root Cause:

The default NVM access timeout value for reads was 5 msec. If the BMC firmware was doing an erase on a slow flash, it could take up to 5 seconds to complete before our access was even started (accesses are synchronized by an SPI arbiter in the chipset). This caused us to return an error code indicating that the NVM was possibly corrupt and generated a PXE error message PXE-05. Errors could also be generated by EEUPDATE doing EEPROM tests in a loop from a batch file under DOS.

Resolution Notes:

Increased ICHx NVM flash access timeout value to 10 seconds to handle the worst possible case (BMC starting a 64KB erase just before PXE starts one). This is only the maximum timeout and in most cases will never be reached.

Version 1.3.28

Defect

Details:

PCIe fatal error (malformed TLP issue) during PXE boot

Root Cause:

82575 could generate a zero-length TLP on the PCIe bus, causing a system halt.

Resolution Notes:

Added code to work around the errata and prevent the erroneous TLP.

Version 1.3.27

Defect

Details:

Enable ECC protection by default on 82571EB silicon

Root Cause:

82571EB FIFO ECC is not enabled by default

Resolution Notes:

UNDI driver changed to enable FIFO ECC after every reset

Version 1.3.24

Defect

Details:

WDS install image loads via PXE are too slow

Root Cause:

If the receive descriptor was updated in memory by the hardware between the time the driver read the length from the descriptor and the time the driver checked the descriptor completion status, the driver would drop the packet thinking its length was 0, which is invalid.

Resolution Notes:

Modified the code to retrieve the length after checking the descriptor completion status. That way the length field is guaranteed to be correct.

Version 1.3.21

Details:

IBA speed and duplex settings port map swapped on 82575-based adapter

Root Cause:

UNDI driver was fetching the wrong EEPROM word when forcing speed/duplex on multi-port adapters

Resolution Notes:

Corrected the code to use the right word

Version 1.3.21

New Feature

Feature Description:

Added support for 82576 controller

Changes Made:

Added required device Ids

Version 1.3.21

New Feature

Feature Description:

ICH10D platform LAN support

Changes Made:

Added required device Ids

Version 1.3.21

New Feature

Feature Description:

Added support for 82574 controller

Changes Made:

Added required device Ids

Version 1.3.10

New Feature

Feature Description:

ICH10/ICH10R platform LAN support

Changes Made:

Added required device Ids

Defect

Details:

82567 does not link to some switches over 2-/3-pair cable

Root Cause:

82567 PHY code was incorrectly setting the PHY page register when reading extended registers.

Resolution Notes:

Modified shared code to correctly handle the page registers on the 82567

Version 1.3.00

New Feature

Feature Description:

Support for PCI BIOS 3.0 specification

Changes Made:

Initialization code updated to detect PCI BIOS version and act accordingly

Defect

Details:

DF185972 - PE1850 systems are not adhering to PXE2.1 standard

Root Cause:

PXE UDP_READ API was being called with interrupts disabled. This prevented the real-time clock interrupt from firing and therefore the timer mechanism to terminate the API if no packets are received did not function, since it depends on the BIOS tick counter, which is incremented by the real-time clock interrupt.

Resolution Notes:

Modified the UNDI driver packet poll routine to temporarily enable interrupts, allowing the clock interrupt to occur. This matches the behavior in the 10/100 UNDI driver, which did not show the same problem.

New Feature

Feature Description:

Support for forcing speed/duplex on ICHx

Changes Made:

UNDI loader passes value of word 30h to UNDI driver at startup for use in case the driver cannot read the EEPROM itself, as is the case with ICHx. On all other silicon, the UNDI driver will read the EEPROM for itself and ignore the passed-in value.

Intel PCIe 10GbE Boot Agent change log

Current Version: 2.1.81
Previous Version: 2.0.11 Alpha 3

Version 2.1.81

Change Details:

Add X540 Silicon and NIC Support

Brief Description:

Add X540 Silicon and NIC Support

Changes Made:

X540 related C shared code changes ported to 10Gig assembly shared code. Changes made to 10Gig UNDI.

Version 2.1.71

Change Details:

Support For New PBA EEPROM Format

Changes Made:

Changes in asm shared code (ported e1000_read_pba_string), refactored PXE setup code to use new e1000_read_pba_string.

Change Details:

82599 FCoE SKU

Brief Description:

New device IDs: 1529, 152A

Changes Made:

Added new device IDs: 1529, 152A

Change Details:

82599 Support for 1000BASE-T SFP Modules

Brief Description:

82599 Support for 1000BASE-T SFP Modules

Changes Made:

Assembly Shared Code updated to support requirements.

Version 2.1.71 Beta 3

Change Details:

82599 FCoE SKU

Brief Description:

Add 82599 FCoE SKU

Changes Made:

Additional updates to Assembly Shared Code and PXE. Defines for FCOE IDs aligned with C Shared Code.

Version 2.1.70

Add Wake from S5 support to 82599 KR connections

Brief Description:

Add Wake from S5 support to 82599 KR connections

Changes Made:

Added code to reset WUS register during initialization to enable following WOL events

Change

Details:

82599 10GBASE-T Device Support

Brief Description:

Add device ID support for 10GBASE-T device

Changes Made:

Added requested device ID

Change

Details:

Add 10G support for active DA cables

Version 2.1.60

Defect Details:

Modify 82598 PCIe Completion Timeout Values

Root Cause:

82598 default PCIe completion timeout value is below PCIe spec recommend 10ms.

Resolution Notes:

Write a value to PCIe config space to increase the PCIe completion timeout value above 10ms if and only if system BIOS left timeout at default value. Also disable Completion timeout resend for packets that do timeout. See 82598 Specification Update, Specification Clarification #2 for more details.

Change Details:

Copper link speeds 1Gbps and 10Gbps

Root Cause:

Need support for 82599 NICs with multispeed copper

Resolution Notes:

Added support for 82599 NICs with multispeed copper

Version 2.1.50

Change

Details:

82599 Combined Backplane Support

Resolution Notes:

Added support for 82599 combined backplane device.

Change Details:

82599 CX4 Support

Root Cause:

New product introduction.

Resolution Notes:

Added support for 82599 combined backplane device.

Version 2.1.41

Details:

82598 second generation NIC Support

Brief Description:

Added support for 82598 second generation NIC PXE.

Changes Made:

Added support for 82598 second generation NIC PXE.

Version 2.1.40 Beta 6

Defect

Details:

82599 XAUI Support

Root Cause:

New requirement for XAUI support.

Resolution Notes:

Added support for Device ID 10FC

Version 2.1.40 Beta 5

Defect

Details:

IBA/PXE Option ROM: When Good Semaphores Go Bad - Utilities unable to update EEPROM after boot

Root Cause:

The SWSM register was being read during PXE initialization code. This was occurring because on the system in the test lab the BIOS was setting the value of BAR2 to a value that was lower than BAR0.

Specifically:

BAR0: F8180000

BAR2: F817C000

The PXE init code would interpret BAR2 as a Flash BAR, when it is actually the MSI-X BAR in 82599.

The init code would do a scan to find the option ROM image, starting at BAR2 and checking every 16 bytes for 512K of memory. Due to the BIOS configuration this would read the memory addressed by BAR0, which is the register configuration space of the device itself, including the SWSM register at offset 0x10140 (on a 16 byte boundary). The SWSM register is a set on read for bit 0, so this errant read would set the semaphore so other utilities, like LANConf or EEUPDATE, couldn't get the semaphore.

Resolution Notes:

Added code in PXE init to check for option ROM header before searching for 512K.

New Feature

Change Title:

82599 SFI Multi-Speed Pluggable Support.

Brief Description:

Added support for multispeed fiber modules.

Changes Made:

Added support for multispeed fiber modules.

Version 2.1.40 Beta 4

Defect

Details:

1. Fixed bug in multispeed fiber where it didn't work if connected to a 1GbE switch. Now works BTB and with a switch in 1GbE mode.

2. Fixed bug that caused several second delay before getting link.

Root Cause:

1. For multispeed fiber I needed to force autonegotiation to be true.

2. End of list value for PHY init code in EEPROM was incorrect resulting in several second delay.

Resolution Notes:

1. Fixed bug in multispeed fiber where it didn't work if connected to a 1GbE switch. Now works BTB and with a switch in 1GbE mode.

2. Fixed bug that caused several second delay before getting link.

Version 2.1.40 Beta 3

Defect

Details:

Could not link with 82598.

Root Cause:

Changes made for 82599 multispeed fiber broke the 82598 link initialization.

Resolution Notes:

Fixed 82598 link code to correctly test for what speed to link at.

Version 2.1.40 Beta 1

Change

Details:

Pluggable SFP Support

Title:

Pluggable SFP Support

Brief Description:

Added support for Intel "branded" SFP+ modules.

Changes Made:

Added support for Intel "branded" SFP+ modules.

Change

Details:

82599 SFI Multi-Speed Pluggable Support

Title:

DCN 755: 82599 SFI Multi-Speed Pluggable Support

Brief Description:

Added support for multispeed fiber SFP+ modules for 82599.

Changes Made:

Added support for multispeed fiber SFP+ modules for 82599.

Version 2.1.40 Alpha 1

Defect

Details:

Implement DRV_LOAD bit to properly set/clear

Root Cause:

DRV_LOAD bit was not being set in PXE.

Resolution Notes:

Now set the DRV_LOAD bit when the UNDI driver is initialized.

Version 2.1.22 Alpha 1

Defect

Details:

Add support for new PRO 10 Gigabit AT Server NIC

Root Cause:

Didn't have support for new PRO 10 Gigabit AT Server NIC

Resolution Notes:

Added support for new PRO 10 Gigabit AT Server NIC.

Version 2.1.21

Defect Details:

IBA should ignore LAN Function Select bit 10gig

Root Cause:

Init code was reading the STATUS register to determine which port it was on. This register is influenced by LAN Function Select. The tools set the EEPROM configuration words based on PCI Function number. This caused the init code to use the wrong configuration words with the 82598 because LAN Function Select bit is always set.

Resolution Notes:

Changed init code to always use PCI function number to determine which EEPROM configuration words to read.

Version 2.1.20

Details:

Support the 82598 SFP+ LOM with Pluggable Optics

Brief Description:

Added support for the 82598 SFP+ LOM with Pluggable Optics.

Defect

Details:

IBA setup menu disable/enable toggled for both ports from first port setting

Root Cause:

Support for dual port devices was not in place in the 82598 source code.

Resolution Notes:

Added support for dual port devices using words 34 & 35 in EEPROM.

Defect

Details:

SFP+ LOM: Intel® 10 Gigabit AF Dual Port Server Adapter ignores DHCP offers with LR optics installed, no link on Function 1.

Root Cause:

Bug in PHY detection code due to type in equate name. Was checking the 1GB comp codes, not 10GB comp codes.

Resolution Notes:

Fixed typo in equate name. Also changed IXGBE_CONTROL_EOL_NL from 0FFFFh to 00FFFh, bug found in C shared code.

Version 2.1.20 Alpha 2

Defect

Details:

APITEST failed to get DHCP address after restarting network connection.

Root Cause:

Memory corruption from an errant pointer.

Resolution Notes:

Fixed an issue where APITEST was failing to get a DHCP address when running newtest.exe.

Fixed an issue where APITEST was failing NICGetMcstAddr and NICSetPacketFilter.

Fixed xgbe_get_sfp_init_sequence_offsets, it was corrupting memory due to an errant pointer.

Version 2.1.11

Defect

Details:

Intel® 10 Gigabit Dual Port Express Module - PXE fails to load correctly on x6000 chassis

Root Cause:

The functions for doing I/O reads and writes were not protected to be atomic operations. What caused the problem is that RDT was not getting updated because of an interrupt occurring between the address and data writes of RDT. Following is the flow from bus trace #2 that shows what went wrong:

Packet	Address	Data	Function	Register
96761	8C00	1018	IOW	RDT
96766	8C00	0800	IOW	EICR
96771	8C04	0002	IOR	
96775	8C00	0888	IOW	EIMC
96779	8C04	FFFFFFFF	IOW	
96783	8C04	0004	IOW	

Int occurs right after this.

This is supposed to be RDT new value.

So what happened is the missed write of RDT occurred 16 times in a row so we never updated tail and RDH eventually wrapped back to RDT causing the RX logic to not update the driver.

Resolution Notes:

Added disable and enable interrupts around the I/O functions to make the operation atomic.

Version 2.1.10

New Feature

Feature Description:

Support for Intel® 10 Gigabit AF Dual Port Server Adapter and Intel® 10 Gigabit Dual Port Express Module

Changes Made:

Device IDs and PHY initialization from EEPROM were added

Version 2.1.10 Alpha 1

Defect

Details:

PXE fails to time out after not finding PXE link

Root Cause:

The low-level link check routine had a 10-second retry loop where it should have returned immediately.

Resolution Notes:

Link detection timeout is now handled correctly by the UNDI driver and not the shared code. BTW, PXE would eventually timeout after about 20 minutes... :)

Version 2.1.01 Alpha 3

New Feature

Details:

Added support for Intel® 10 Gigabit Dual Port Express Module device ID 10E1.

Changes Made:

Added support for Intel® 10 Gigabit Dual Port Express Module device ID 10E1.

Defect

Details:

Fix for PXE boot from cold power up for Intel® 10 Gigabit AF Dual Port Server Adapter and Intel® 10 Gigabit Dual Port Express Module adapters.

Root Cause:

Fix for PXE boot from cold power up for Intel® 10 Gigabit AF Dual Port Server Adapter and Intel® 10 Gigabit Dual Port Express Module adapters.

Resolution Notes:

Fix for PXE boot from cold power up for Intel® 10 Gigabit AF Dual Port Server Adapter and Intel® 10 Gigabit Dual Port Express Module adapters.

Defect

Details:

Link problems with Intel® 10 Gigabit AF Dual Port Server Adapter adapters.

Root Cause:

Needed extra logic to get true link state from Twinax direct attach PHY's.

Resolution Notes:

Added extra logic to check for link on Intel® 10 Gigabit AF Dual Port Server Adapter adapters to account for link flap and "sticky" link register bit in the PHY.

Version 2.1.01 Alpha 1

Brief Description:

Added support for Intel® 10 Gigabit AF Dual Port Server Adapter NIC. This includes initializing the PHY from EEPROM sections for SFP+ pluggable PHY's. Currently only support Twinax direct connect cable. Device ID 10F1.

Changes Made:

Added support for Intel® 10 Gigabit AF Dual Port Server Adapter NIC. This includes initializing the PHY from EEPROM sections for SFP+ pluggable PHY's. Currently only support Twinax direct connect cable. Device ID 10F1.

Version 2.1.00

Brief Description:

Intel® 10 Gigabit XF LR Support

Changes Made:

Added support for Intel® 10 Gigabit XF LR.

Customization

Details:

PXE code would not time out when trying to get a packet due to interrupts being disabled.

Brief Description:

PXE code would not time out when trying to get a packet due to interrupts being disabled.

Changes Made:

Added enabled interrupt (STI) to NICProcessInterrupt if not in first case.

Version 2.1.00

New Feature

Feature Description:

Support for PCI BIOS 3.0 specification

Changes Made:

Initialization code updated to detect PCI BIOS version and act accordingly

Intel 10/100 Boot Agent change log

Version 4.2.03

Defect

Details:

IBA takes almost three minutes to detect no link present on 82552

Root Cause:

A little-used PHY control function was missing a RET instruction at the end of the routine, causing execution to fall into the delay function with an abnormally large delay value.

Resolution Notes:

Added the missing instruction. Now link failure is detected within 5 to 10 seconds.

Version 4.2.02

New Feature

Feature Description:

Added support for 82552

Changes Made:

Added device ID 10FE.

Version 4.2.00

New Feature

Feature Description:

Support for PCI BIOS 3.0 specification

Changes Made:

Initialization code updated to detect PCI BIOS version and act accordingly

Intel PCI-X 10GbE Boot Agent change log

Version 1.0.11

No Changes