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C	<div>SHUMWAY</div> <div>SANDY BRIDGE EP (AND/OR) SANDY BRIDGE EN</div> <div>CAVE CREEK (AND/OR) CAVE CREEK</div> <div>FAB A (DP-EP SOCKETED FAB A)</div>								C																																											
B	<div>Shumway Board Configurations</div> <table><tr><th colspan="2">Config</th><th>SNB SKTR (CPU0)</th><th>CCK PCH0</th><th>CCK EP0</th><th>SNB SKTB2 (CPU1)</th><th>CCK PCH1</th><th>CCK EP1</th><th>Comments</th></tr><tr><td rowspan="2">EP Boot</td><td>DP-SKTR-2EP</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>PWR OFF</td><td>ON</td><td>SKTR Boot Default (board build SKU)</td></tr><tr><td>UP-SKTR-EP0</td><td>ON</td><td>ON</td><td>ON</td><td>Removed from Socket</td><td>CCK0 Removed from Socket</td><td></td><td>No solder rework required to switch from the default above</td></tr><tr><td rowspan="2">EN Boot</td><td>DP-SKTB2-2EP</td><td>ON</td><td>PWR OFF</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>No solder rework required to switch from the default above</td></tr><tr><td>UP-SKTB2-EP1</td><td>Removed from Socket</td><td>CCK0 Removed from Socket</td><td></td><td>ON</td><td>ON</td><td>ON</td><td>No solder rework required to switch from the default above</td></tr></table>								Config		SNB SKTR (CPU0)	CCK PCH0	CCK EP0	SNB SKTB2 (CPU1)	CCK PCH1	CCK EP1	Comments	EP Boot	DP-SKTR-2EP	ON	ON	ON	ON	PWR OFF	ON	SKTR Boot Default (board build SKU)	UP-SKTR-EP0	ON	ON	ON	Removed from Socket	CCK0 Removed from Socket		No solder rework required to switch from the default above	EN Boot	DP-SKTB2-2EP	ON	PWR OFF	ON	ON	ON	ON	No solder rework required to switch from the default above	UP-SKTB2-EP1	Removed from Socket	CCK0 Removed from Socket		ON	ON	ON	No solder rework required to switch from the default above	B
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A	<div>BOARD CONFIGURATION NOTE</div> <div>THIS SCHEMATICS PROVIDES BASIS FOR THE SHUMWAY PB DESIGN AND IS DESIGNED TO REFLECT THE DP-SKTR-2EP CONFIGURATION</div> <div><table><tr><td colspan="3">INTEL CORPORATION</td></tr><tr><td colspan="3">5000 W. Chandler Blvd. Chandler, AZ 85226</td></tr><tr><td>TITLE Shumway</td><td>DOCUMENT NUMBER E97822-100</td><td>REV 1.0</td></tr><tr><td>SHUMWAY TITLE PAGE Intel Confidential</td><td colspan="2">SHEET 1 OF 315</td></tr></table></div>								INTEL CORPORATION			5000 W. Chandler Blvd. Chandler, AZ 85226			TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0	SHUMWAY TITLE PAGE Intel Confidential	SHEET 1 OF 315		A																															
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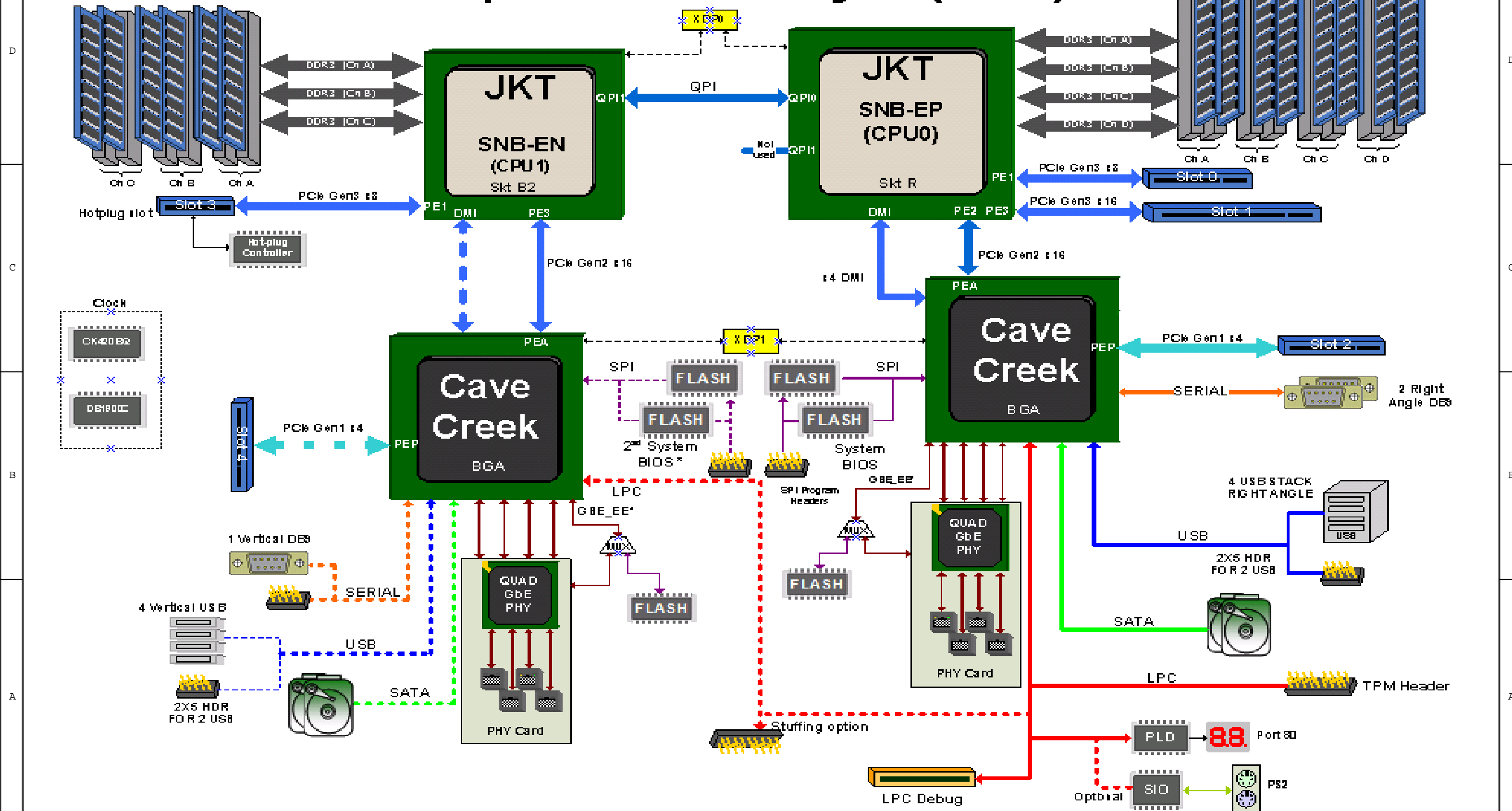
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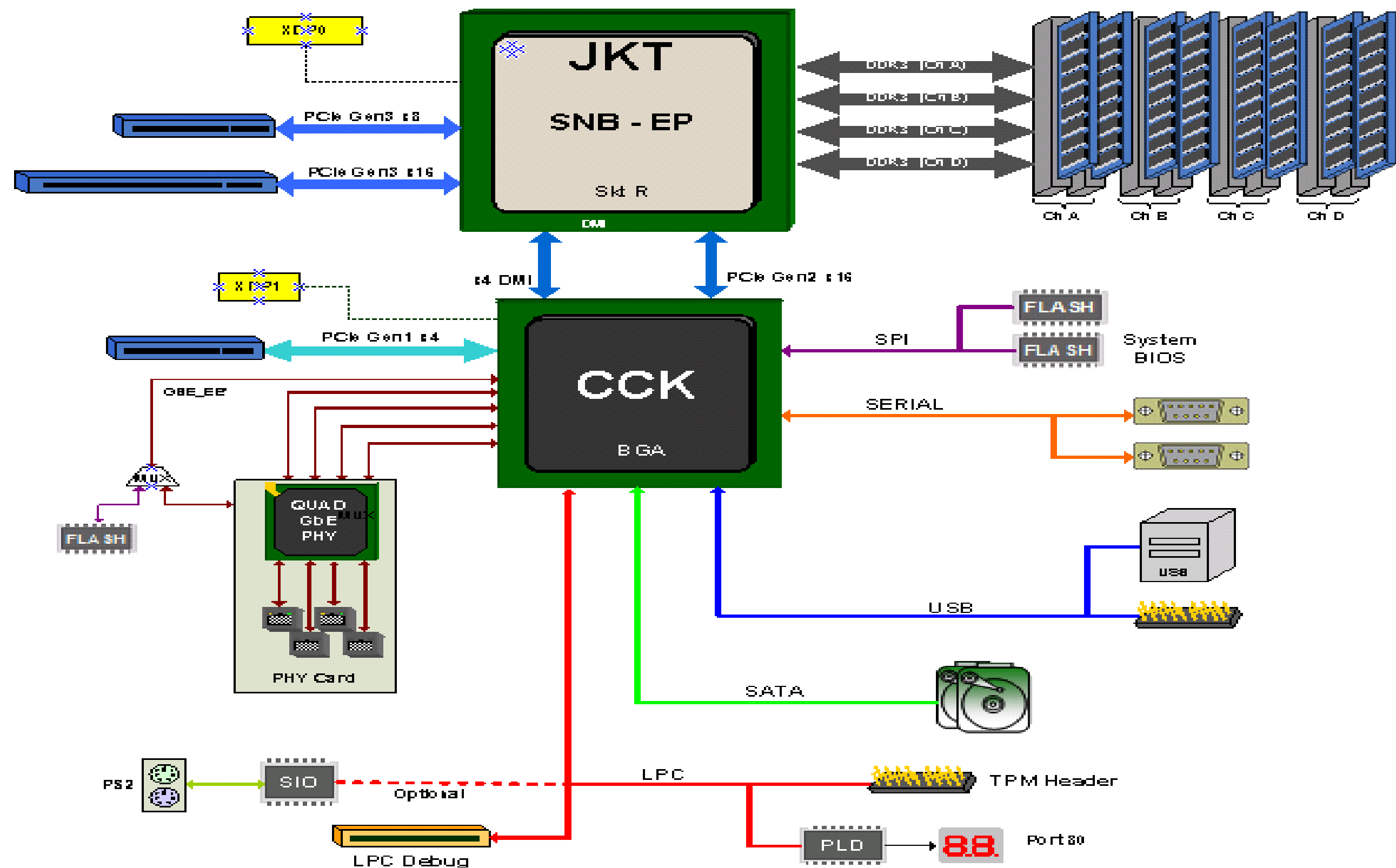
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# Shumway Platform Block Diagram (DP-EP)





## D

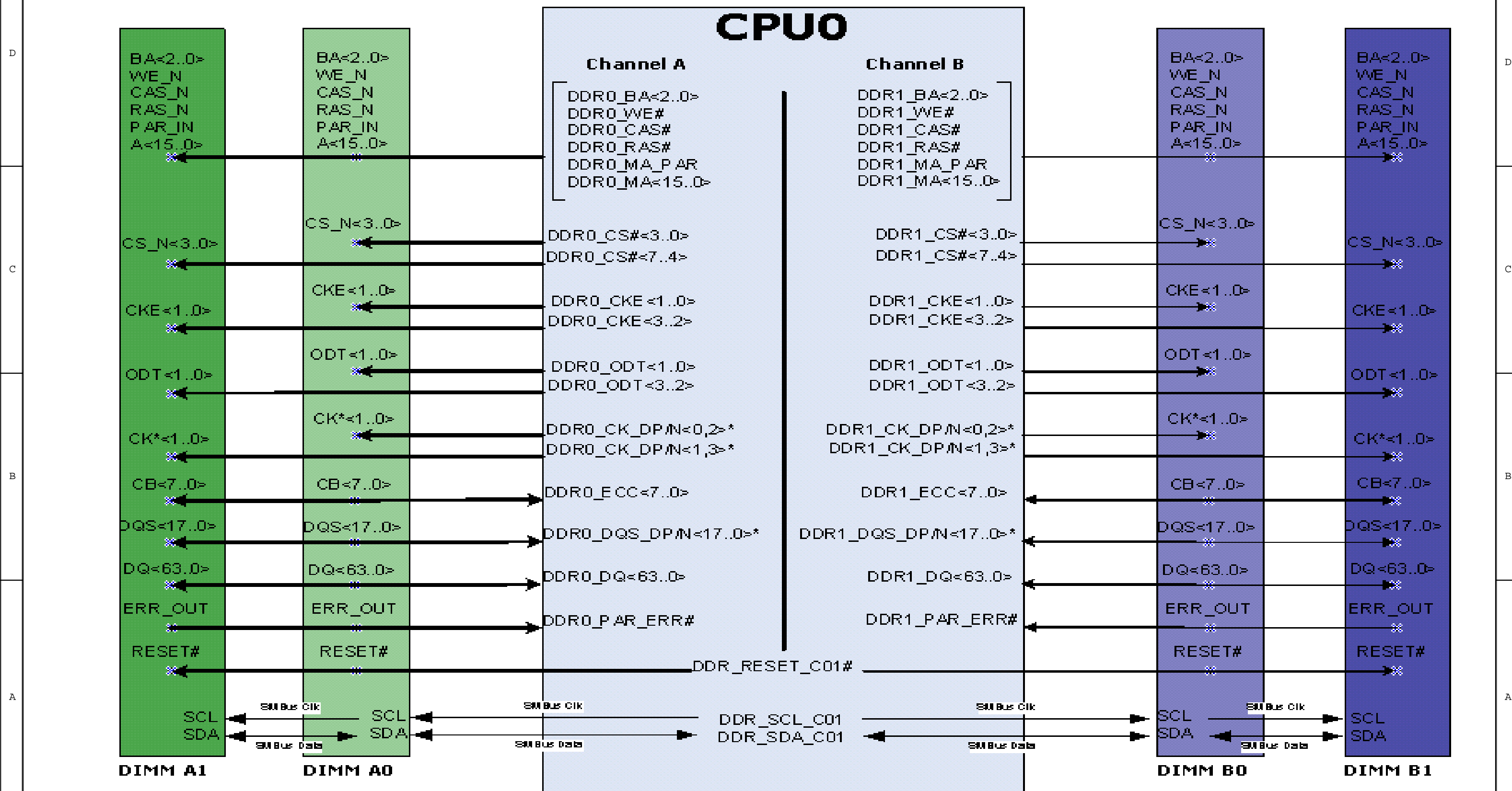


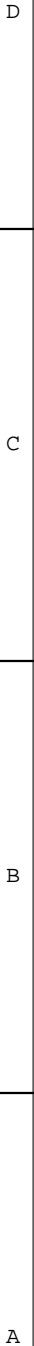
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Shumway Board Configuration Jumper Settings																
Item	Sch Page	Ref Des	Config# 1 DP, SNB-SKTR CPU Boot		Config# 2 UP, SNB-SKTR CPU Boot	Config# 3 DP, SNB-SKTB2 CPU Boot		Config# 4 UP, SNB-SKTB2 CPU Boot	Function							
			CPU0 Boot + CPU1 PCH0 EP0	CPU0 Boot + CPU1 PCH0 EP0 + EP1	CPU0 Boot PCH0 EP0	CPU0 + CPU1 Boot PCH1 EP1	CPU0 + CPU1 Boot PCH1 EP0 + EP1	CPU1 Boot PCH1 EP1								
0	161	J4F1	1-2	1-2	1-2	2-3	2-3	2-3	Select 1.8V for MUX clock U4E7							
1	172	J9F1	Open	Open	Open	1-2	1-2	1-2	CPU0 Socket ID0							
2	172	J7D1	1-2	1-2	1-2	Open	Open	Open	CPU1 Socket ID0							
3	190	J3F1	2-3	2-3	2-3	1-2	1-2	1-2	SPI select to boot from PCH0 or PCH1 To program the SPI flash memory: J3F1 = 1-2							
4	190	J3F2	1-2	1-2	1-2	2-3	2-3	2-3								
5	201	J2H3	1-2	1-2	1-2	Open	Open	Open	Enable PCH0 power supplies/signals J2H3 = 1-2							
6	202	J2H2	1-2	1-2	1-2	Open	1-2	Open	Enable EP0 power supplies/signals J2H3 = 1-2							
7	203	J2D4	Open	Open	Open	1-2	1-2	1-2	Enable PCH1 power supplies/signals J2D4 = 1-2							
8	204	J2D2	Open	1-2	Open	1-2	1-2	1-2	Enable EP1 power supplies/signals J2D2 = 1-2							
9	216	J1F2	1-2	1-2	1-2	2-3	2-3	2-3	Select RTC_PCH power rail PCH0 = 1-2 PCH1 = 2-3							
10	282	J6E6	2-3	2-3	2-3	2-3	2-3	2-3	CPUITP Socket Select = 2-3 Manual override = 1-2 (bypass CPU0)							
11	282	J6F2	2-3	2-3	2-3	2-3	2-3	2-3	CPUITP Socket Select = 2-3 Manual override = 1-2 (bypass CPU1)							
12	282	J6E2	1-2	1-2	1-2	2-3	2-3	2-3	CPU TAP Voltage Select: VTT_CPU = VTT_CPU0 = 1-2 VTT_CPU = VTT_CPU1 = 2-3							
13	293	J2E1	Open	Open	Open	Open	Open	Open	for Debug or validation only Disable EP JTAG Chain = 1-2							
14	296	J2D8	2-3	2-3	2-3	2-3	2-3	2-3	for Debug or validation only Disable PCH JTAG chain = 1-2							
15	296	J2D6	1-2	1-2	1-2	2-3	2-3	2-3	PCH TAP voltage select: VTAP = PCH0 = 1-2 VTAP = PCH1 = 2-3							
										INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226						
										TITLE Shumway				DOCUMENT NUMBER E97822-100		REV 1.0
										CONFIGURATION SETTING Intel Confidential				SHEET 9 OF 315		
8		7		6		5		4		3		2		1		

	8	7	6	5	4	3	2	1
D								
	Board Configuration		Status LEDs					
			VTT_CPU0 DS4F1	VCC1P0_PCH0 DS4F2	VCC1P0_EP0 DS4F3	VTT_CPU1 DS4F4	VCC1P0_PCH1 DS4F5	VCC1P0_EP1 DS4F6
C	Config# 1 DP SNB-SKTR CPU Boot	CPU0 Boot + CPU1 PCH0 EP0	ON	ON	ON	ON	off	off
		CPU0 Boot + CPU1 PCH0 EP0 + EP1	ON	ON	ON	ON	off	ON
C	Config# 2 UP SNB-SKTR CPU Boot	CPU0 Boot PCH0 EP0	ON	ON	ON	off	off	off
B	Config# 3 DP SNB-SKTB2 CPU Boot	CPU0 + CPU1 Boot PCH1 EP1	ON	off	off	ON	ON	ON
		CPU0 + CPU1 Boot PCH1 EP0 + EP1	ON	off	ON	ON	ON	ON
B	Config# 4 UP SNB-SKTB2 CPU Boot	CPU1 Boot PCH1 EP1	off	off	off	ON	ON	ON
A								
	8	7	6	5	4	3	2	1

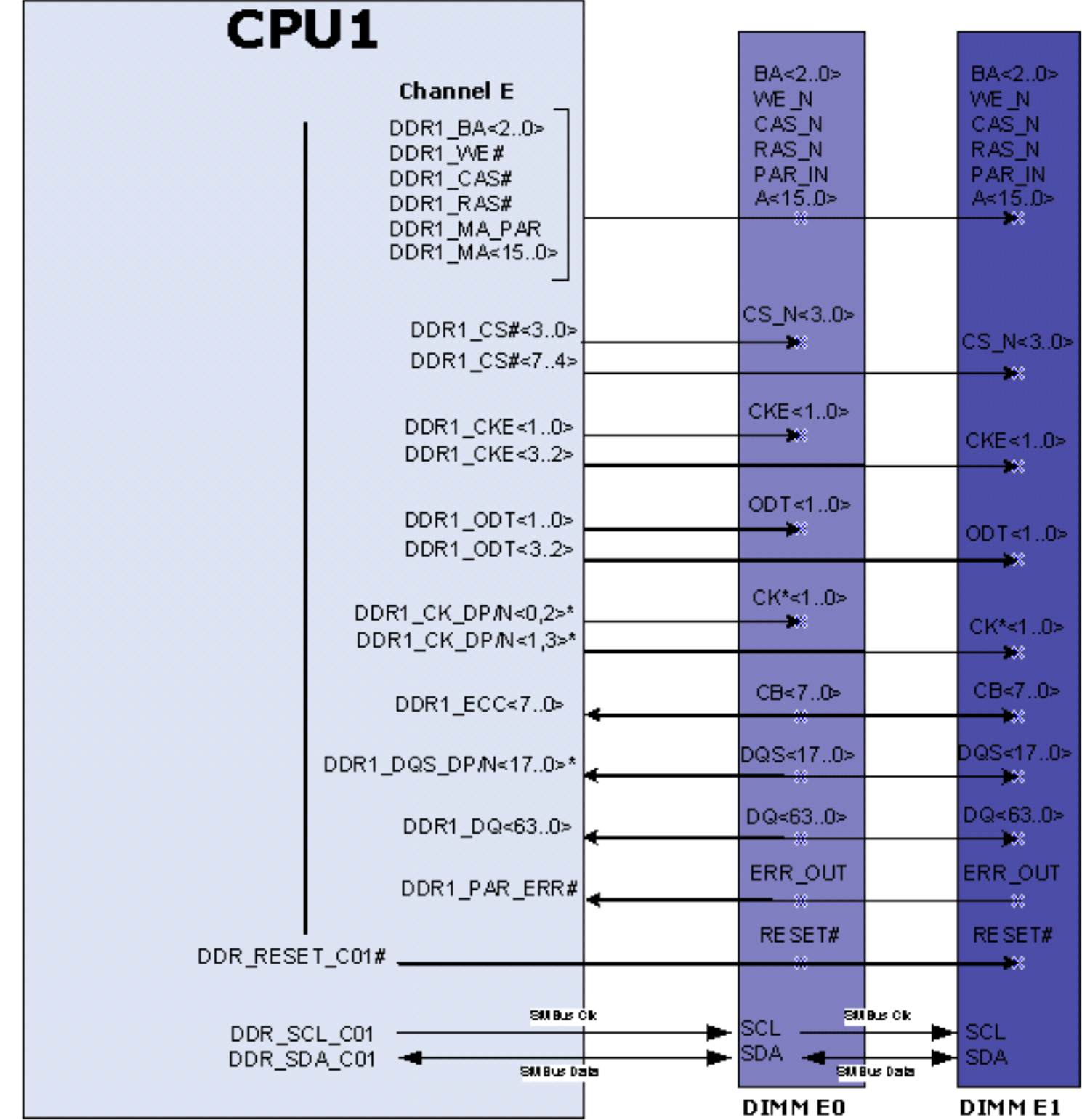


# Shumway DDR3 Chan A and B (CPU0)



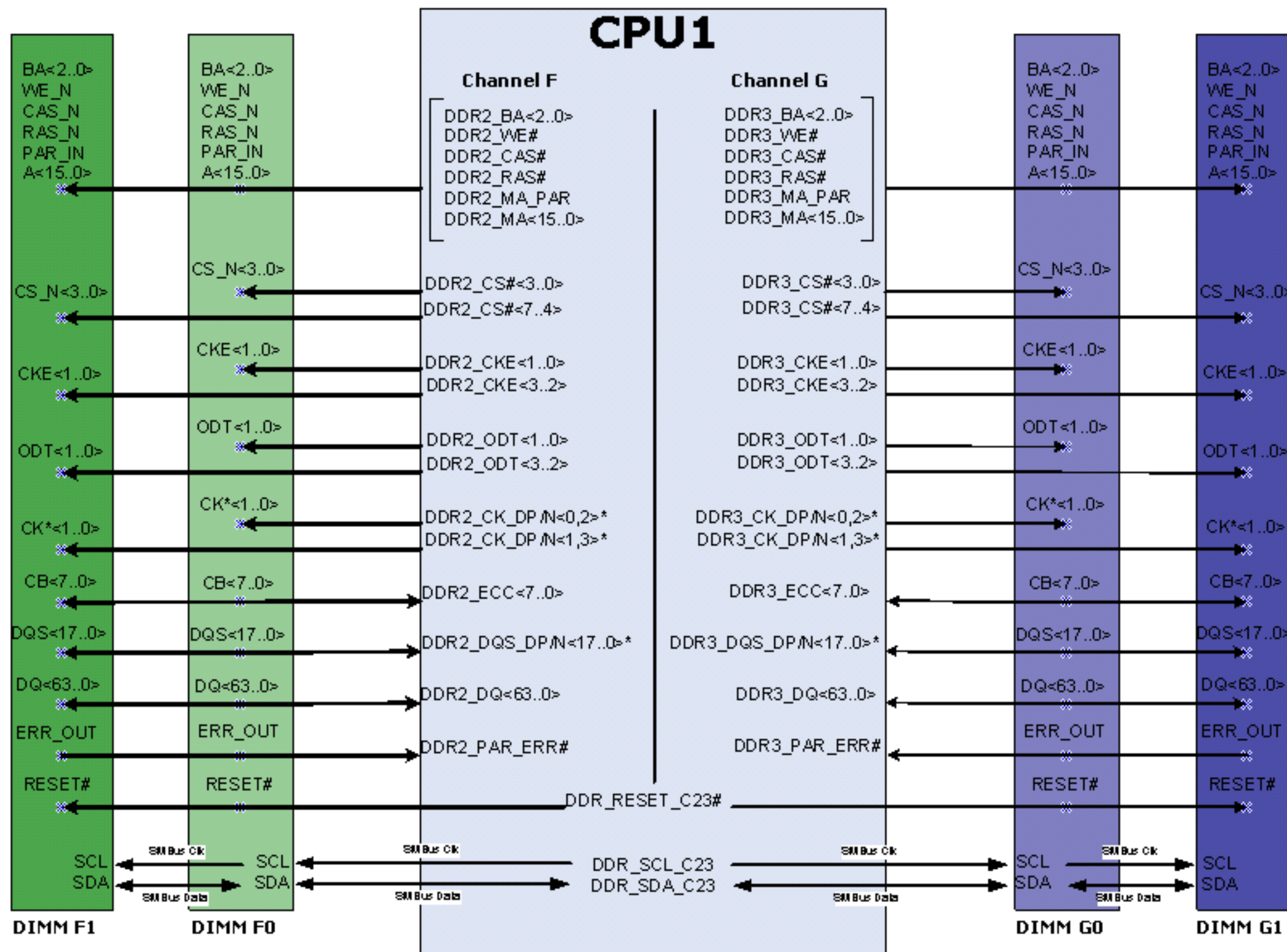


# Shumway DDR3 Chan E (CPU1)



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DDR3 BD - CHAN E Intel Confidential	SHEET 13 OF 315	

# Shumway DDR3 Chan F and G (CPU1)



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1.0







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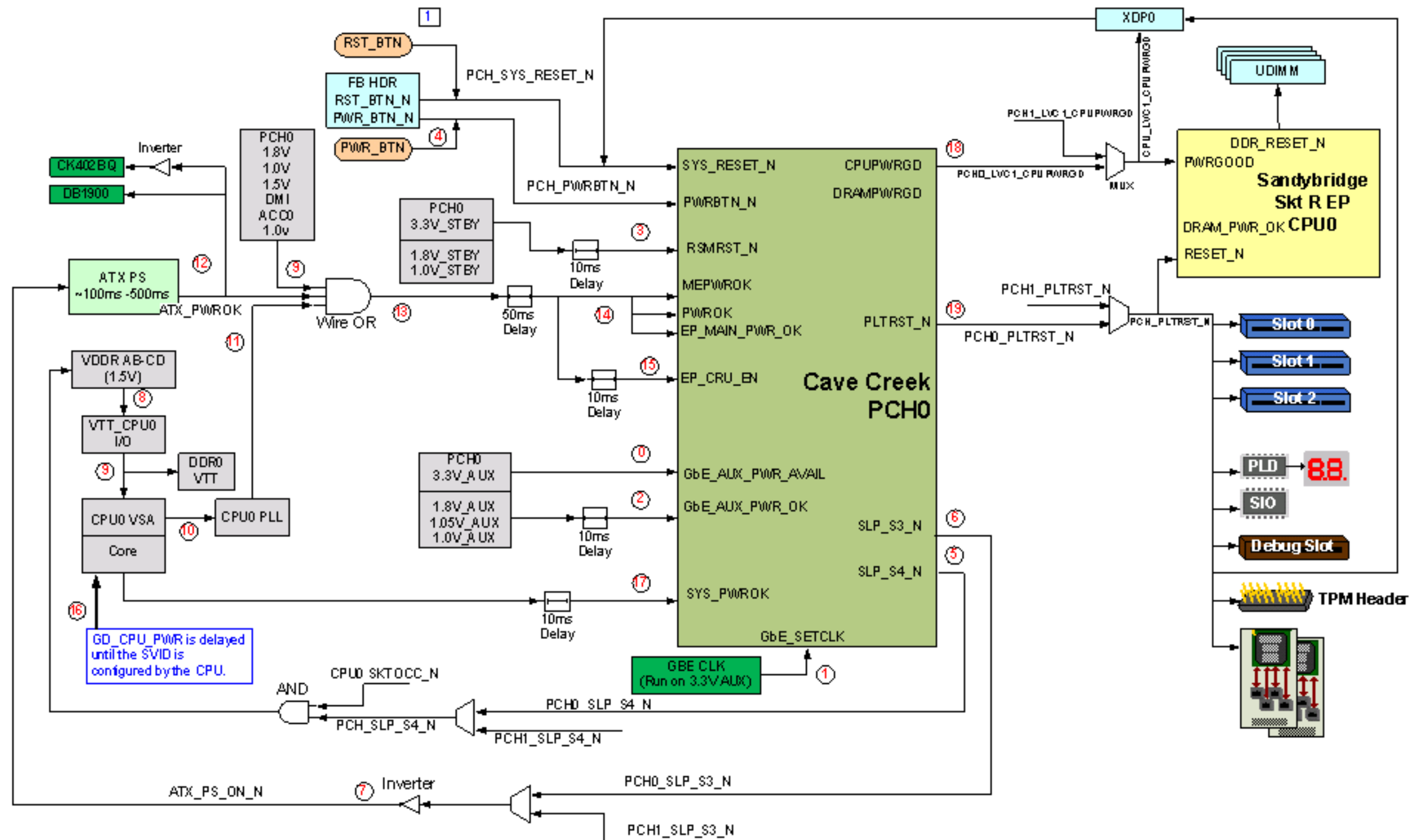
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Power Net Name		Voltage (v)		Power well		Source		Active in States		Usage					
VCC12_PS		+12V		main		24-Pin CONN ATX		S0		Various					
VCC12N_PS		-12V		main		24-Pin CONN ATX		S0		Various					
VCC5_PS		+5V		main		24-Pin CONN ATX		S0		Various					
VCC3P3_PS		+3.3V		main		24-Pin CONN ATX		S0		Various					
VCC5_PS_STBY		+5V		standby		24-Pin CONN ATX		S0 - S5		Various					
VCC12A1_PS		+12V		main		8-Pin CONN ATX		S0		CPU0					
VCC12A2_PS		+12V		main		8-Pin CONN ATX		S0		DDR3 DIMMs Channel AB, CD					
VCC12B1_PS		+12V		main		8-Pin CONN ATX		S0		CPU0					
VCC12B2_PS		+12V		main		8-Pin CONN ATX		S0		DDR3 DIMMs Channel EFG					
V12_V5_STBY_A		+12V / +5V		AUX		VCC12A2_PS / VCC5_PS_STBY		S0 - S5		DDR3 DIMMs Channel AB, CD					
V12_V5_STBY_B		+12V / +5V		AUX		VCC12B2_PS / VCC5_PS_STBY		S0 - S5		DDR3 DIMMs Channel EFG					
VCC3P3_STBY		+3.3V		standby		VCC5_PS_STBY		S0 - S5		Various					
VCC5_AUX		+5V		AUX		VCC5_PS / VCC5_PS_STBY		S0 - S5		Various					
VCC3P3_AUX		+3.3V		AUX		VCC3P3_PS / VCC3P3_STBY		S0 - S5		Various					
VCC3P3_EP0_AUX		+3.3V		AUX		VCC3P3_AUX		S0 - S5		EP0 (in PCH0)					
VCC1P8_EP0_AUX		+3.3V		AUX		VCC3P3_AUX		S0 - S5		EP0 (in PCH0)					
VCC1P05_EP0_AUX		+1.05V		AUX		VCC1P8_EP0_AUX		S0 - S5		EP0 (in PCH0)					
VCC1P0_EP0_AUX		+1.0V		AUX		VCC1P8_EP0_AUX		S0 - S5		EP0 (in PCH0)					
VCC1P8_PCH0_STBY		+1.8V		standby		VCC3P3_STBY		S0 - S5		PCH0					
VCC1P0_PCH0_STBY		+1.0V		standby		VCC1P8_PCH0_STBY		S0 - S5		PCH0					
VCC1P8_PCH0		+1.8V		main		VCC3P3_PS		S0		PCH0					
VCC1P5_PCH0		+1.5V		main		VCC3P3_PS		S0		PCH0					
VCC1P05_PCH0		+1.05V		main		VCC3P3_PS		S0		PCH0					
VCC1P0_PCH0		+1.0V		main		VCC5_PS		S0		PCH0					
VCC1P8_EP0		+1.8V		main		VCC3P3_PS		S0		EP0 (in PCH0)					
VCC1P0_EP0		+1.0V		main		VCC5_PS		S0		EP0 (in PCH0)					
VCCDMI_PCH0		1.05V or 1.0V		main		VCC3P3_PS		S0		PCH0 and EP0					
												INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226			
TITLE Shumway										DOCUMENT NUMBER E97822-100		REV 1.0			
VOLTAGE TABLE (1) Intel Confidential										SHEET 17 OF 315					
8		7		6		5		4		3		2		1	

A	B	C	D
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SHEET 18 OF 315



# Shumway Power\_Up/Reset Diagram (CPU0 with PCH0)



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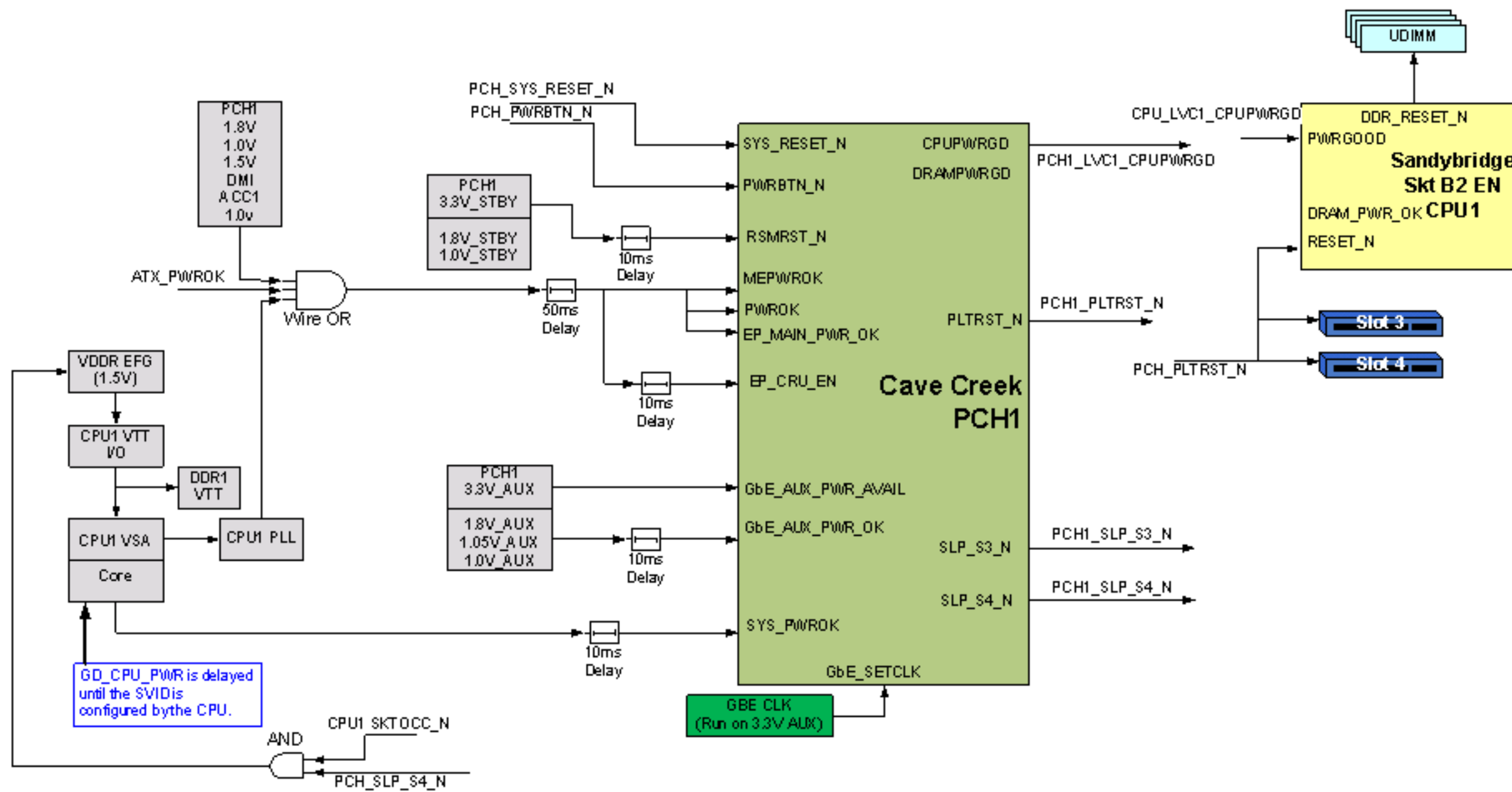
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TITLE Shumway

PU/RST BD (CPU0-PCH0)  
Intel ConfidentialDOCUMENT NUMBER  
E97822-100REV  
1.0

SHEET 19 OF 315

## Shumway Power\_Up/Reset Diagram (CPU1 with PCH1)



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TITLE Shumway

PU/RST BD (CPU1-PCH1)  
Intel Confidential

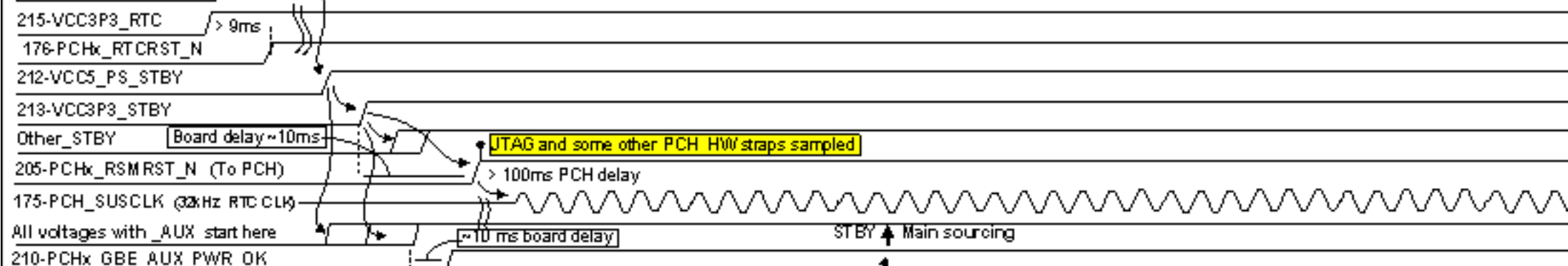
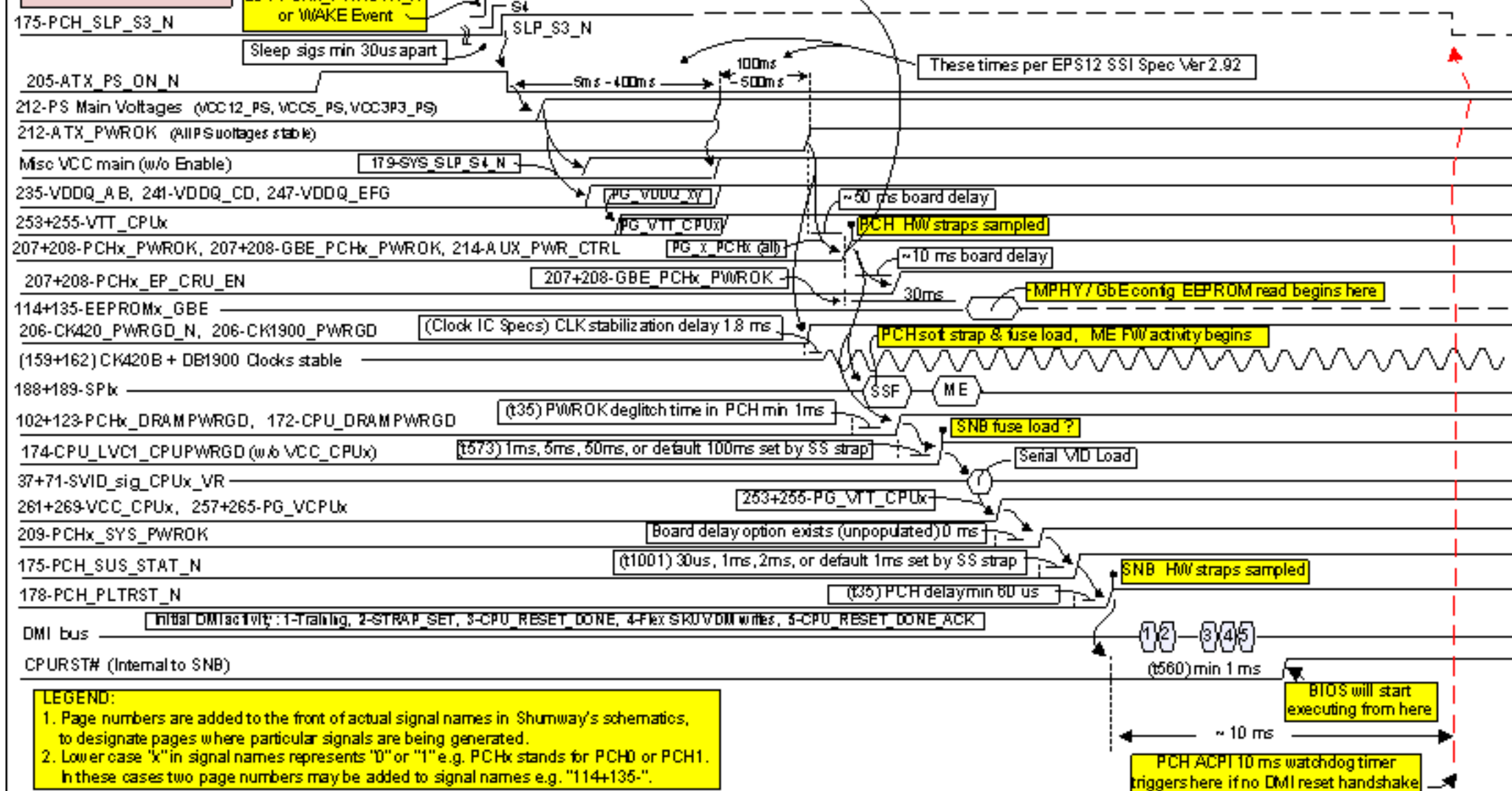
DOCUMENT NUMBER

E97822-100

REV

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**RTC / STBY / AUX  
Wells Power-Up****MAIN Well Power-Up**

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TITLE Shumway

POWER SEQUENCE DIAGRAM  
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- Step 0: GBE\_AUX\_PWR\_AVAIL asserts when VCC3P3\_AUX power become stable; GBE Clock starts as VCC3P3\_AUX is available.
- Step 1: CLK\_100M\_PCH\_GBE\_DP\_p/n (GBE Clock) is stable before GBE\_AUX\_PWR\_OK is asserted.
- Step 2: GBE\_AUX\_PWR\_OK asserted after VCC1P8\_AUX, VCC1P05\_AUX and VCC1P0\_AUX are stable for 10ms.
- Step 3: PCH\_RSMRST\_N (resume reset) de-asserts (High) after the VCC3P3\_STBY stables for at least 10 ms.
- Step 4: PCH\_PWR\_BTN\_N (power button) is pressed (Low); this sends the signal to PCH to wake the system up.
- Step 5: PCH\_SLP\_S4\_N (Sleep state 4) de-asserts (High) from PCH; enables the 1.5V for DDR AB-CD and DDR EFG (for CPU1) power supply.
- Step 6: PCH\_SLP\_S3\_N (Sleep state 3) de-asserts (High) from PCH.
- Step 7: Inverted version of the PCH\_SLP\_S3\_N goes to ATX power supply as ATX\_PS\_ON\_N (power supply on).
- Step 8: PG\_VDDQ\_AB/CD (VDDQ\_AB/CD's power good for CPU0) asserts (High) to enable VTT\_CPU0.
- Step 9: PG\_VTT\_CPU0 (VTT\_CPU0's power good) asserts (high) to enable VTT\_DDR\_AB/CD and VCCSA\_CPU0.
- Power signals from **PCH0** 1.8V, 1.0V, 1.5v and DMI; **EPO** 1.0V asserts (high).
- Step 10: PG\_PVSA\_VCPU0 (VCCSA\_CPU0's power good) asserts (high) to enable VCCPLL\_CPU0.
- Step 11: PG\_VPLL\_CPU0 (VCCPLL\_CPU0's power good) asserts (high).
- Step 12: ATX\_PWROK asserts (High which delayed 100-500ms from ATX\_PS\_ON\_N) to enable CK420 and DB1900.
- Step 13: From Step 9, 11 and 12; ALL\_PCH0\_PWROK asserts (High) with delay 50ms then asserts PCH0\_PWROK (High).
- Step 14: PWROK, MEPWROK and EP\_MAIN\_PWR\_OK are activated by PCH0\_PWROK (High).
- Step 15: EP\_CRU\_EN is activated by PCH0\_EP\_CRU\_EN CPU\_PWRGD (High) after 10ms delay.
- Step 16: After CPU\_PWRGD, the CPU will send SVID to configure VCC\_CORE\_CPU power supply.
- Once the CORE voltage is stable, the VCCP\_PWRGD asserts and enables PCH\_SYS\_PWROK (High).
- Step 17: PG\_VCPU0 asserts (high) then asserts PCH0\_SYS\_PWROK after 10ms.
- Step 18: CPUPWRGD asserts (high)
- Step 19: PCH\_PLTRST\_N de-asserts (High)

**Note: The same sequence is applied to CPU1 as a boot CPU.**

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POWER SEQUENCE DIAGRAM  
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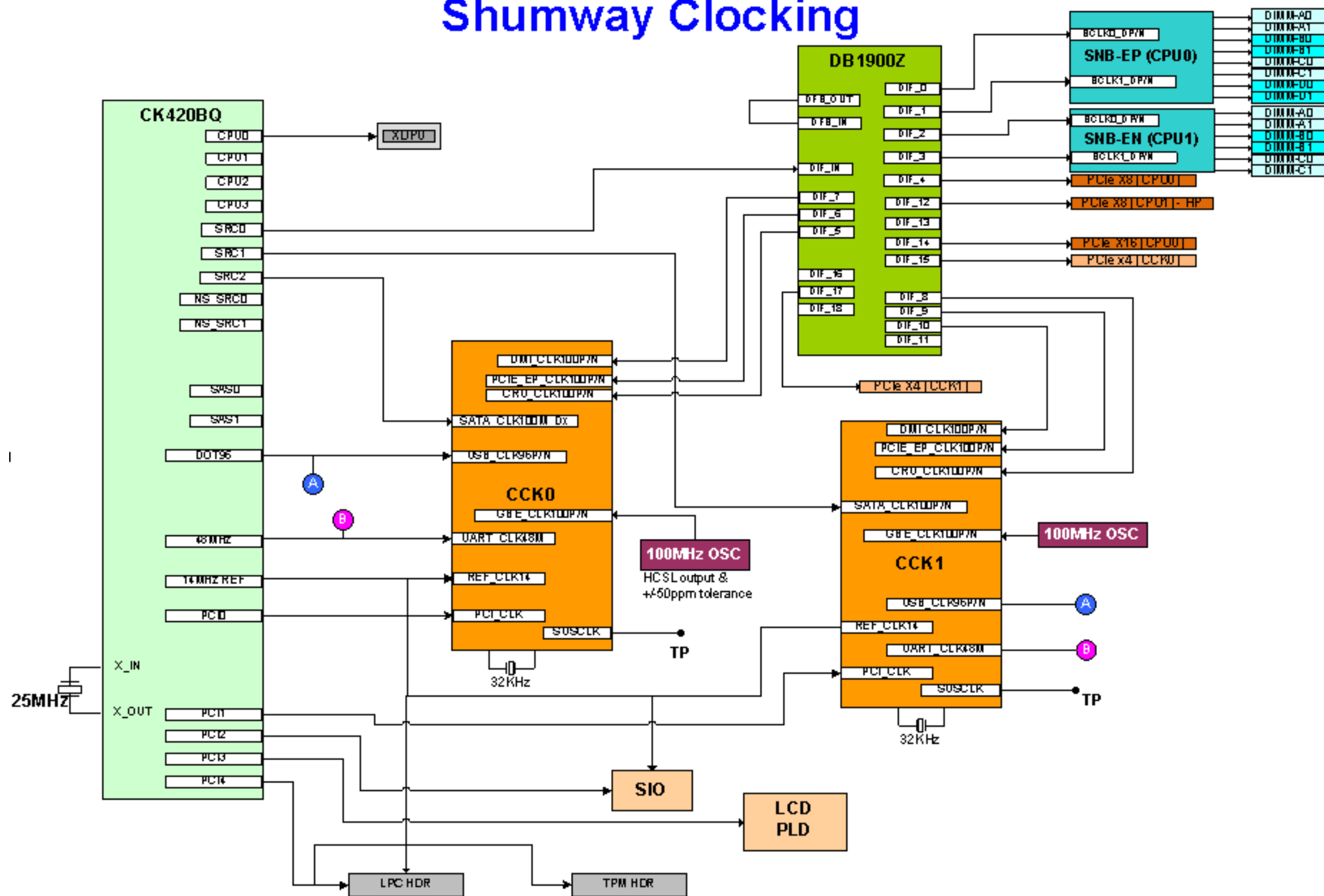
E97822-100

REV

1.0

SHEET 22 OF 315

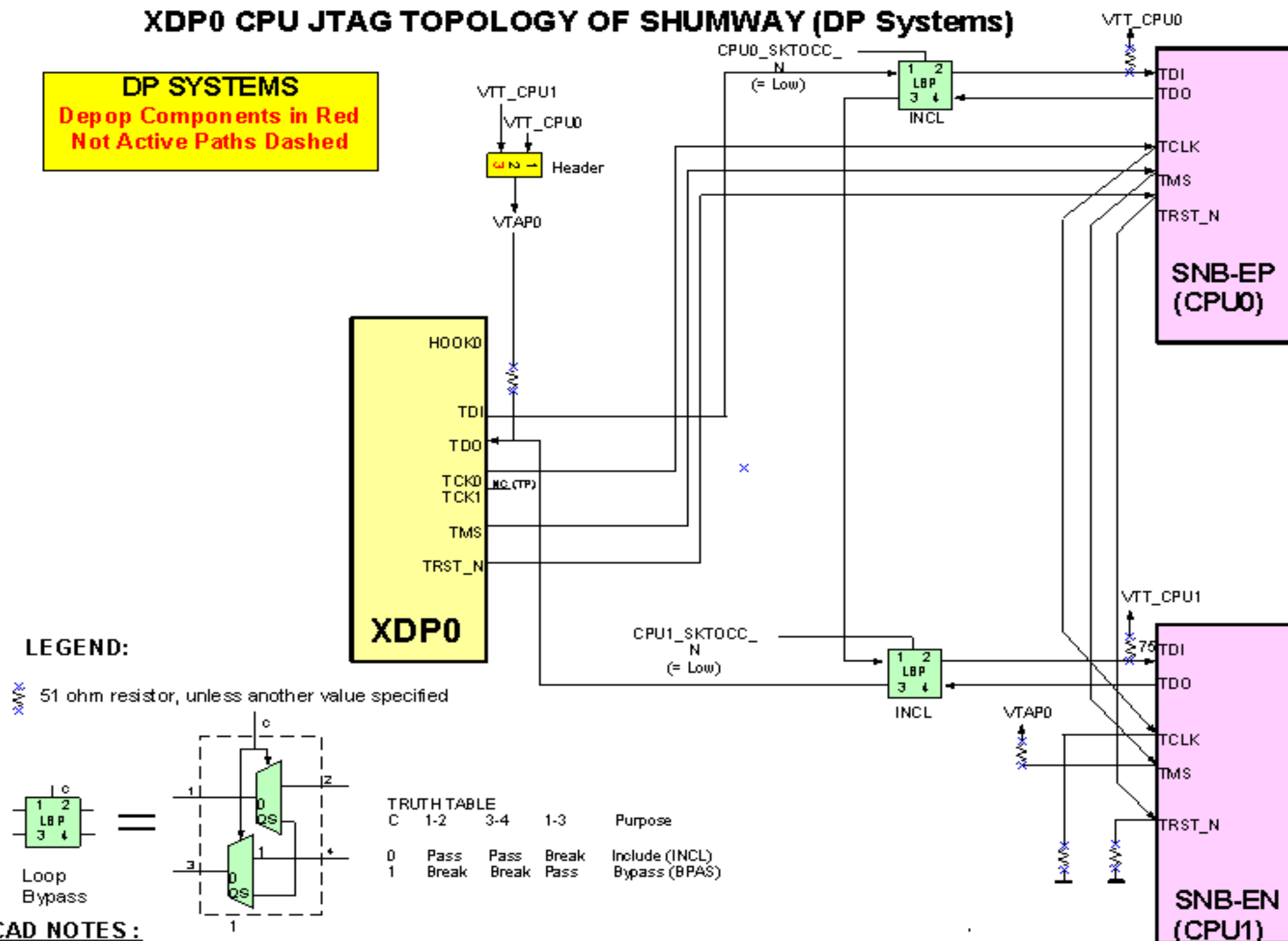
# Shumway Clocking





# XDP0 CPU JTAG TOPOLOGY OF SHUMWAY (DP Systems)

**DP SYSTEMS**  
Depop Components in Red  
Not Active Paths Dashed



## CAD NOTES:

1. Max routing length of JTAG signals from XDP0 to CPU1 is 1.5ns (< 9 inch)
2. Follow recommendations in Crystal Forest DPDG [1]

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XDP CPU JTAG TOPOLOGY  
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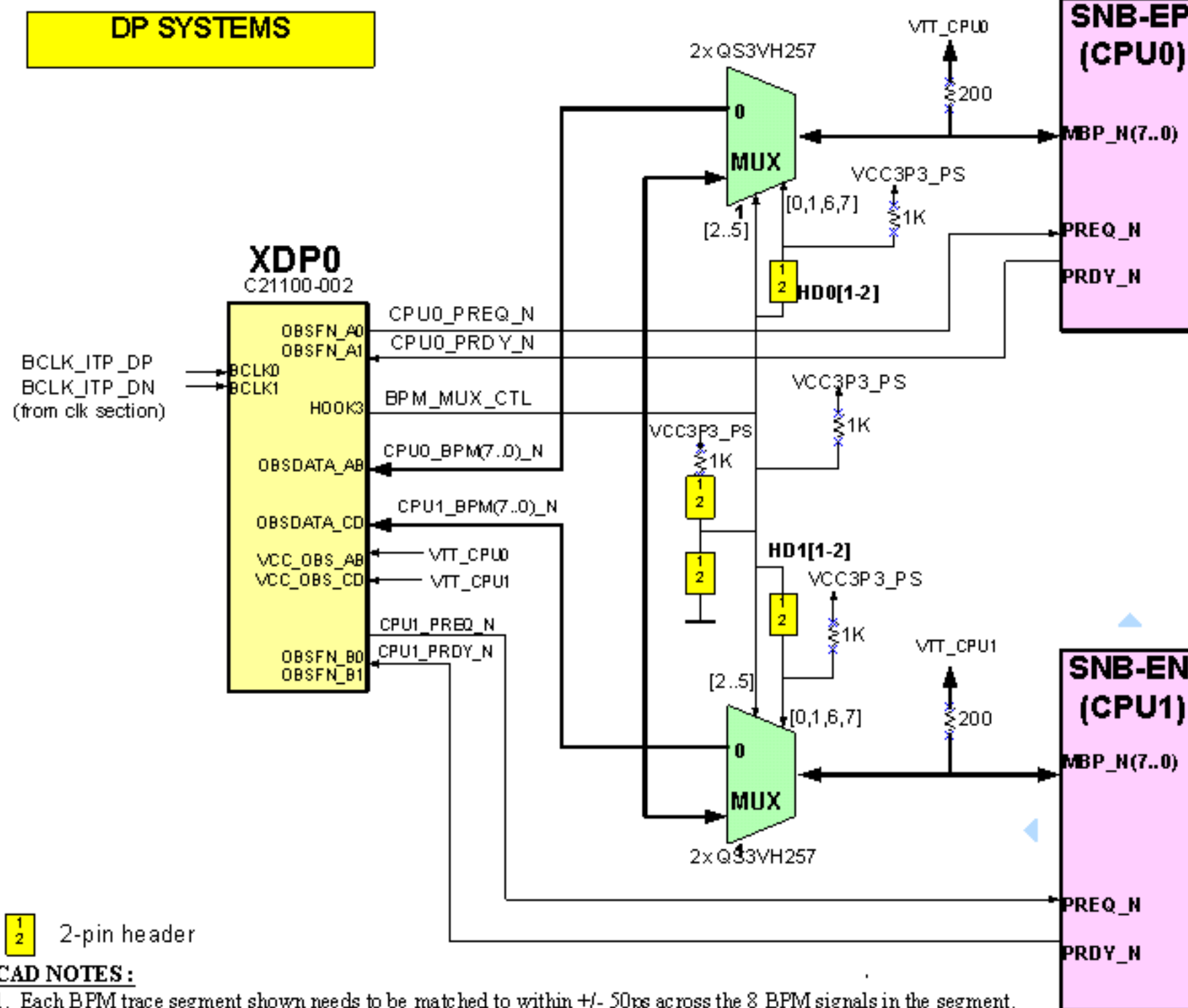
DOCUMENT NUMBER  
E97822-100

REV  
1.0

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# XDP0 CPU OBS TOPOLOGY OF SHUMWAY (DP SYSTEMS)



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TITLE Shumway

XDP CPU OBS TOPOLOGY  
Intel ConfidentialDOCUMENT NUMBER  
E97822-100

SHEET 26 OF 315

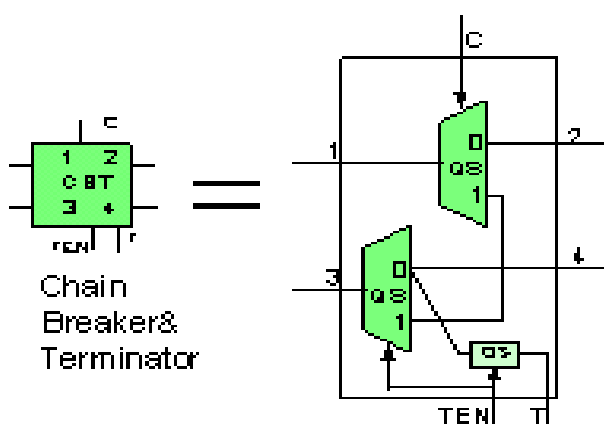
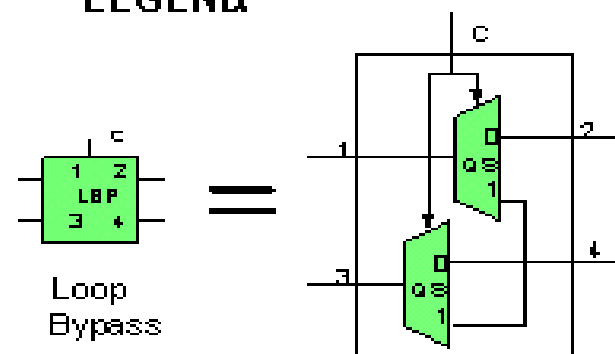
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# XDP1 CCK JTAG TOPOLOGY OF SHUMWAY(DP-SKTR-2 EP)

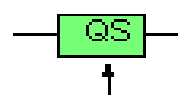
**DP-SKTR-2 EP**
**DEFAULT SYSTEM**
**Depop Components In Red**  
**Not Active Paths Dashed**

## LEGEND



51 ohm term resistor unless value specified

Quick Switch Buffer



## Connect to

- VCC1P0\_PCH0\_STBY
- VCC1P0\_PCH1\_STBY
- VCC1P0\_EP0\_AUX
- VCC1P0\_EP1\_AUX

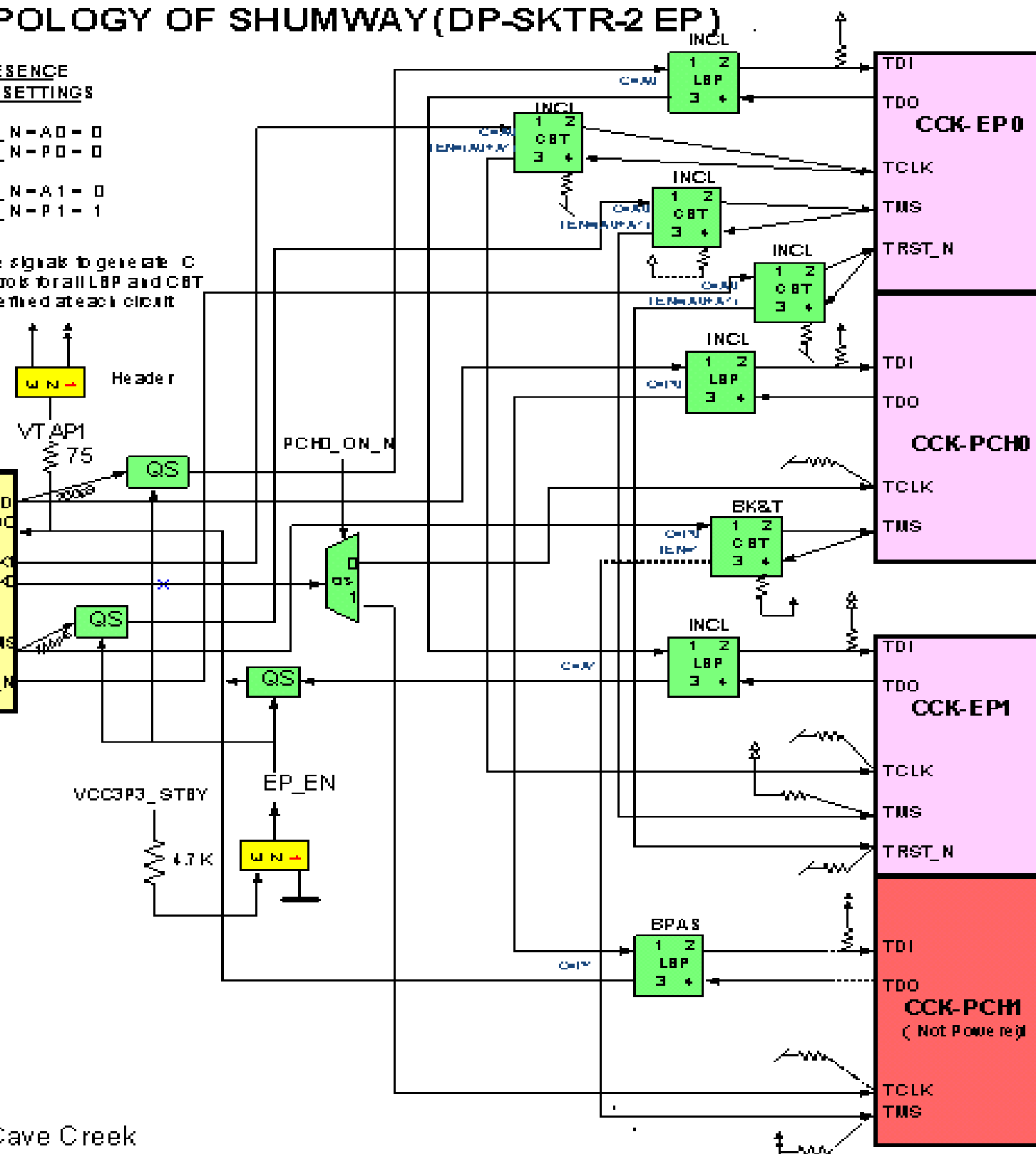
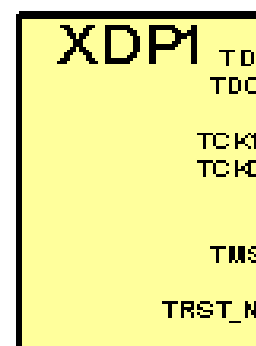
## CCK PRESENCE JUMPER SETTINGS

EP0\_ON\_N=A0=0  
 PCH0\_ON\_N=P0=0

EP1\_ON\_N=A1=0  
 PCH1\_ON\_N=P1=1

## NOTE

Use the above signals to generate C and TEN controls for all LBP and CBT clients as is defined at each client.


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TITLE Shumway

 XDP PCH JTAG TOPOLOGY  
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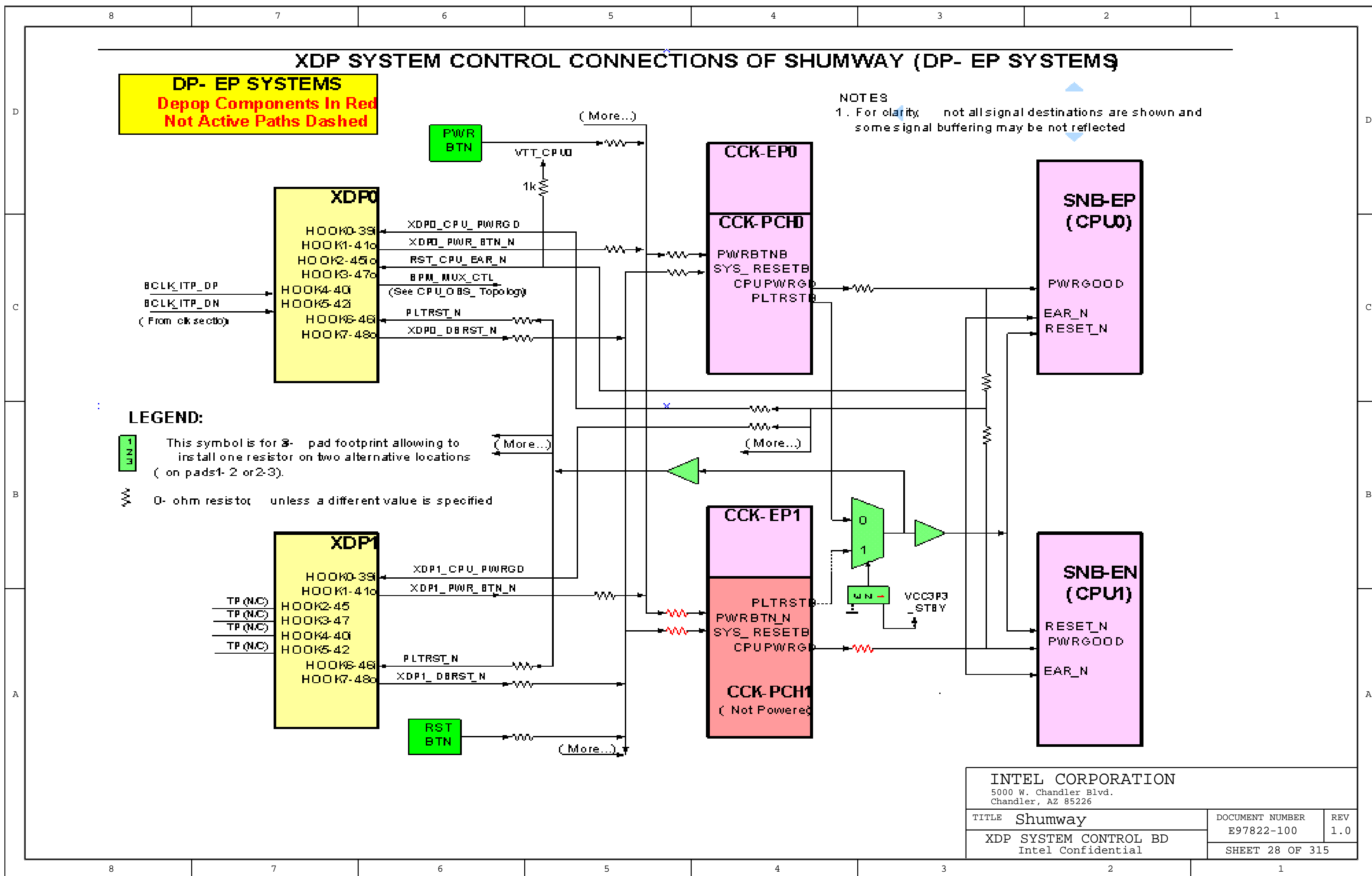
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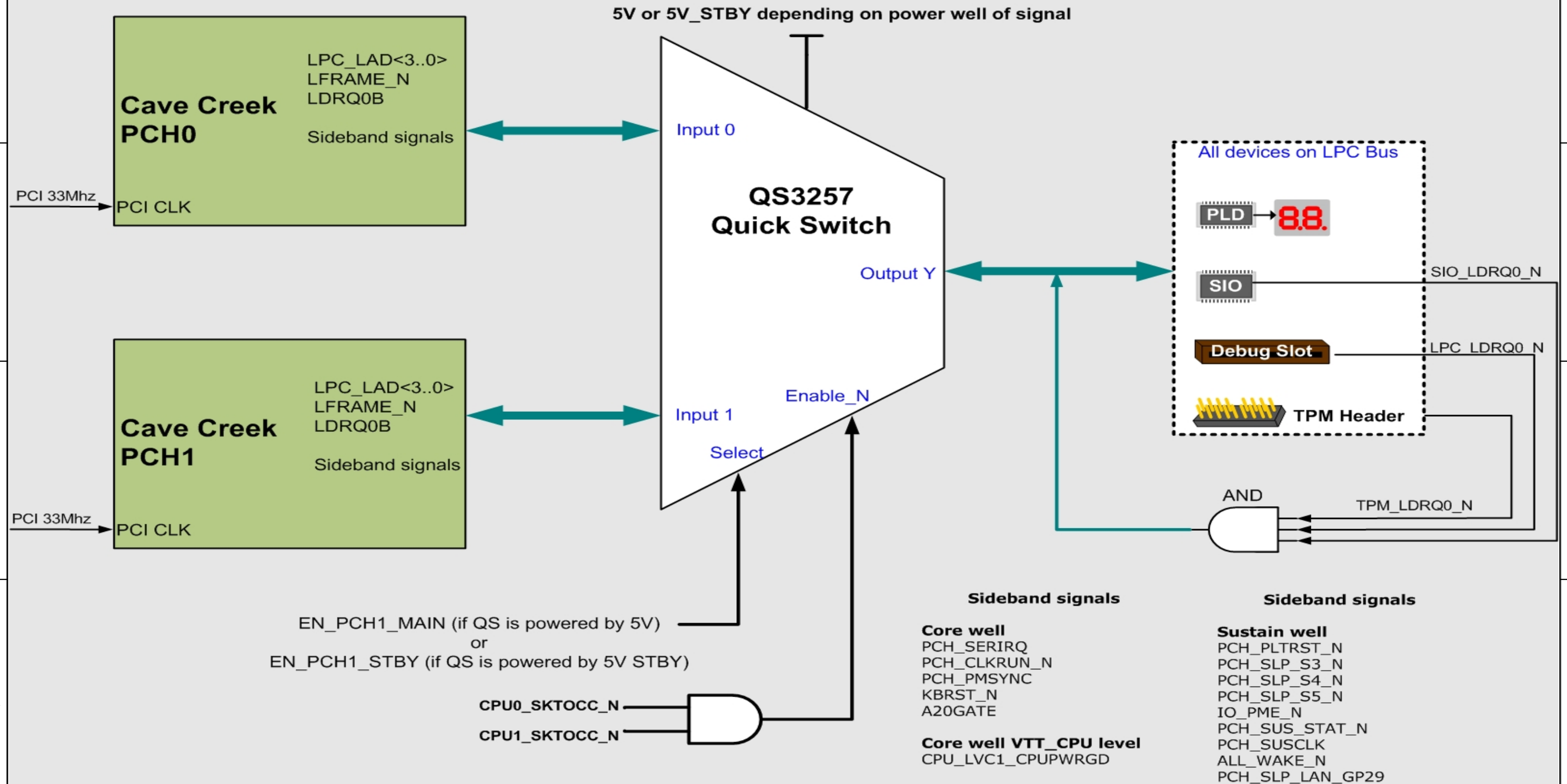
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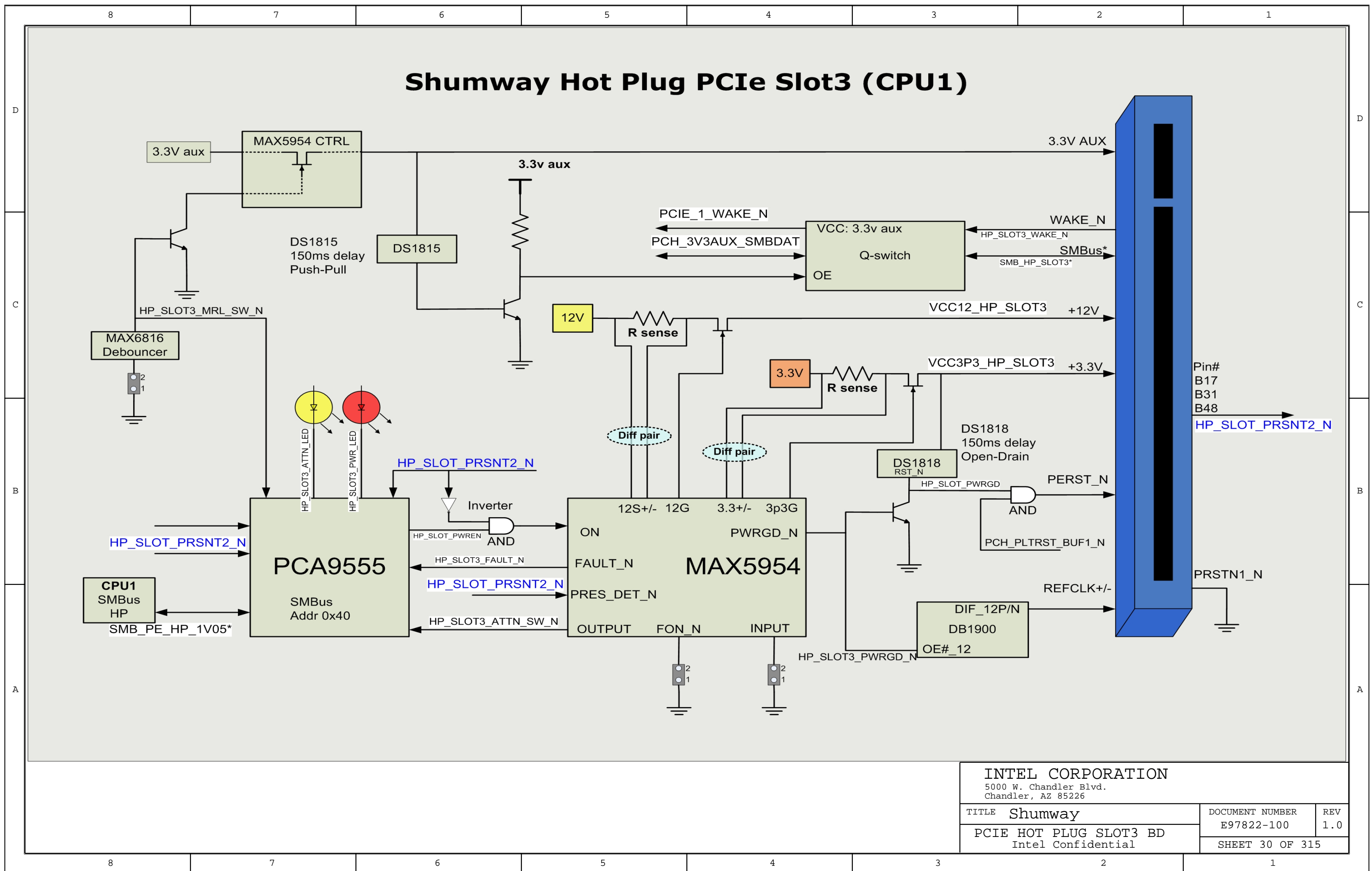


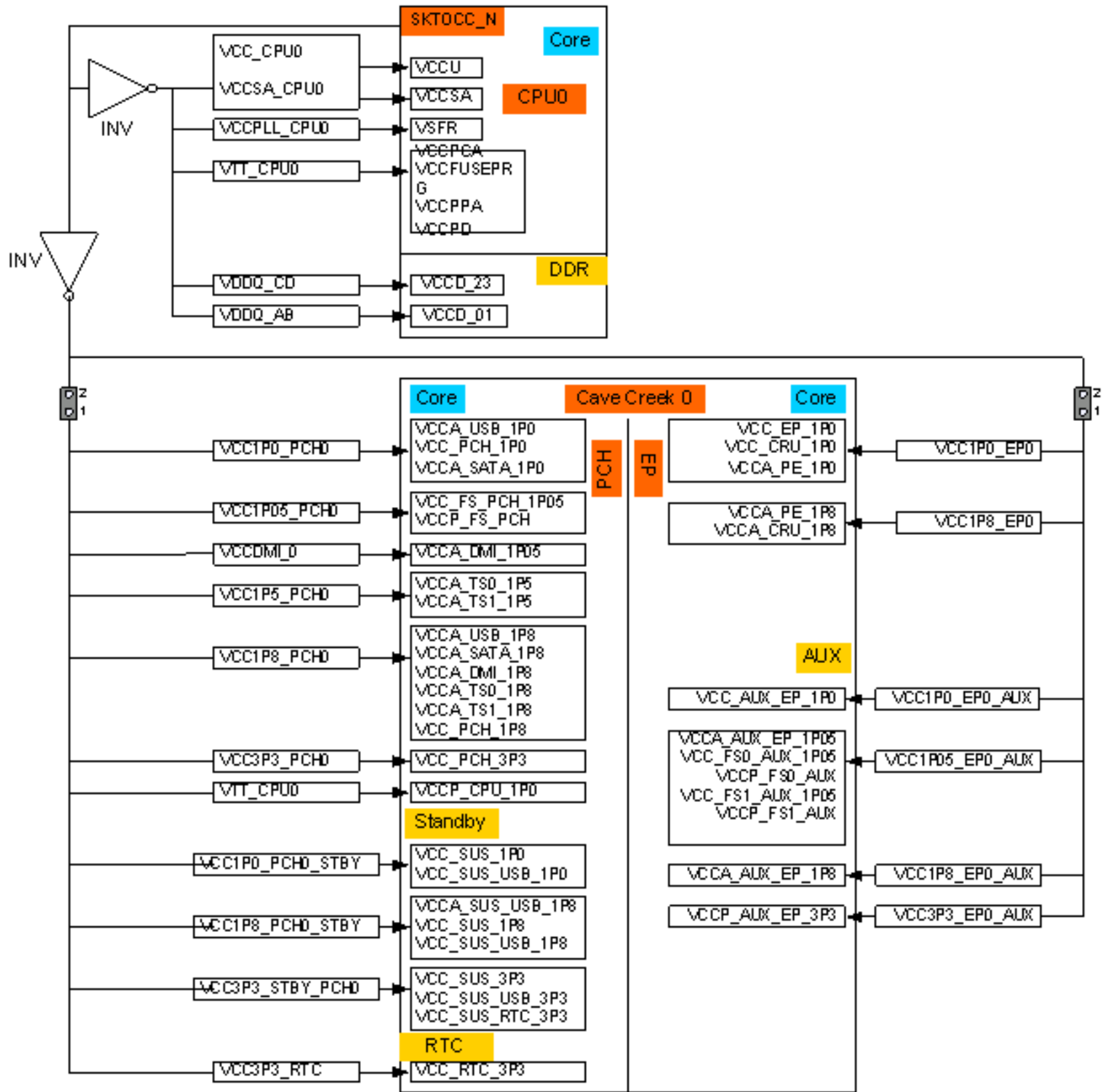
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Chandler, AZ 85226

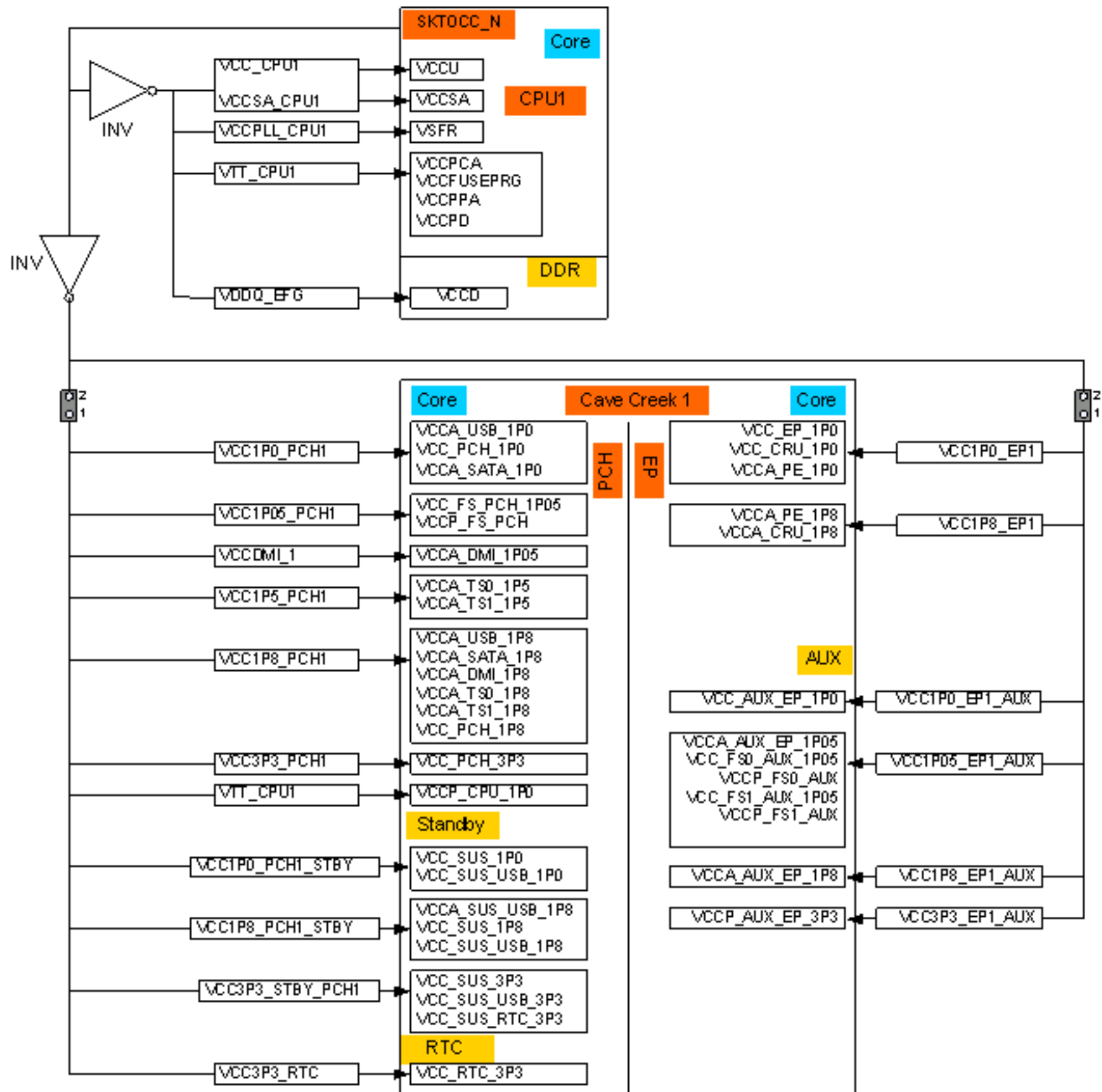
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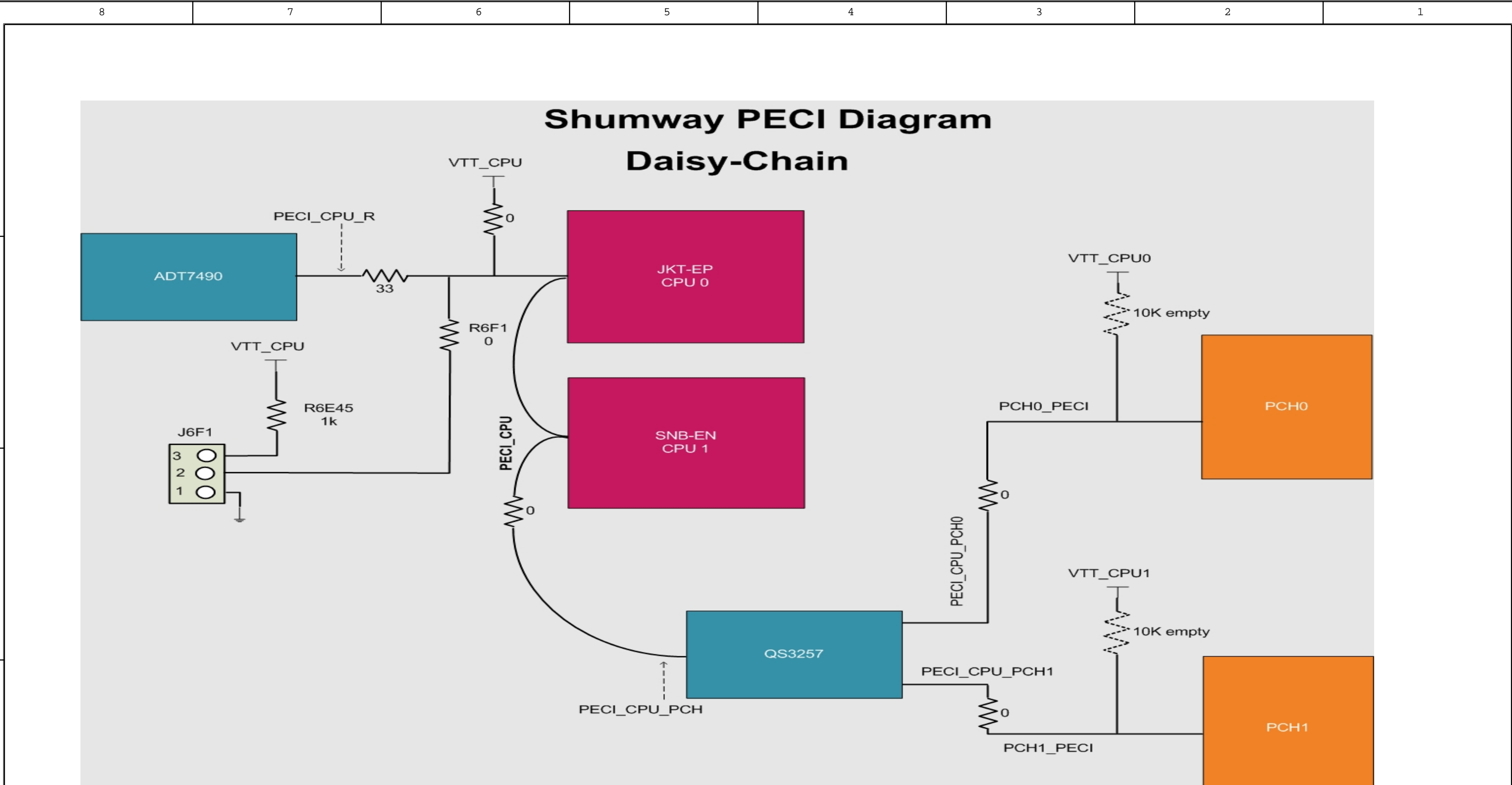
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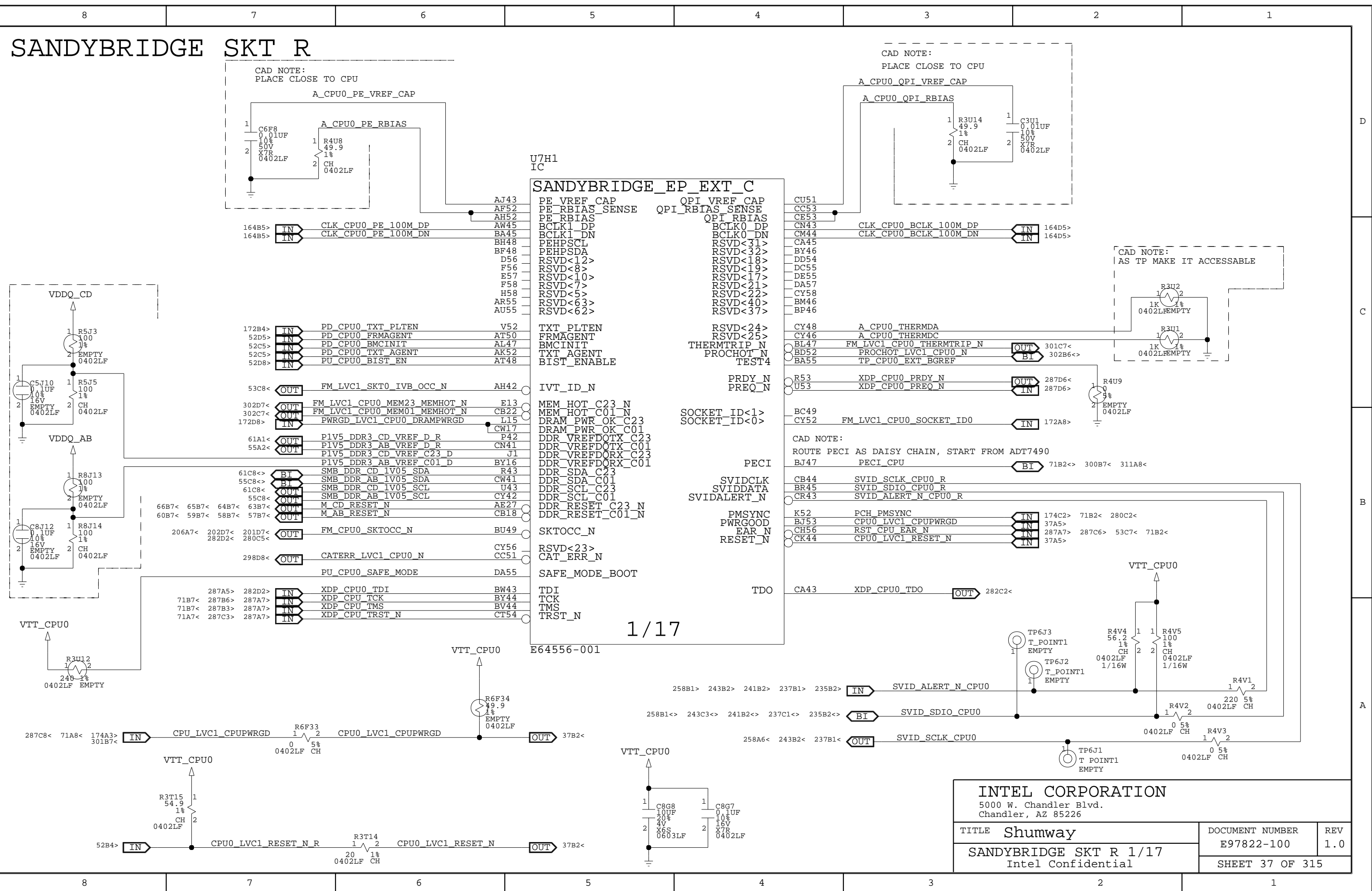


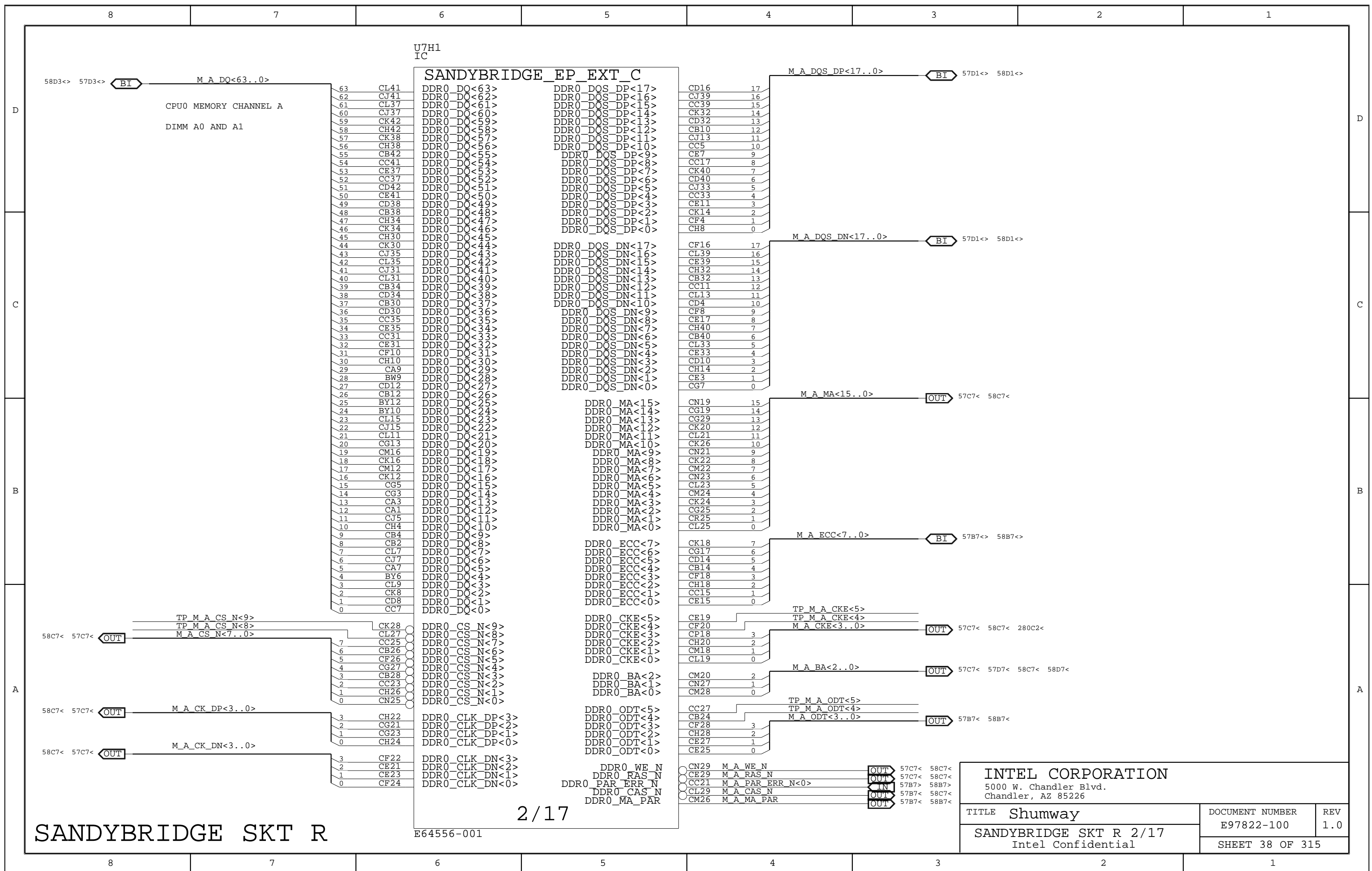


8	7	6	5	4	3	2	1
D	Shumway Status LED						
	Item	Sch Page	LED Ref Des	Fuction	Color		
C	0	117	DS1H1	PCH0 GBE STATUS LED	GREEN		
	1	117	DS1H2	PCH0 GBE STATUS LED	YELLOW		
	2	117	DS1H3	PCH0 GBE STATUS LED	GREEN		
	3	117	DS1H4	PCH0 GBE STATUS LED	YELLOW		
	4	138	DS2C1	PCH1 GBE STATUS LED	GREEN		
	5	138	DS2C2	PCH1 GBE STATUS LED	YELLOW		
	6	138	DS2B1	PCH1 GBE STATUS LED	GREEN		
B	7	138	DS2B2	PCH1 GBE STATUS LED	YELLOW		
	8	149	DS9B2	HOT PLUG ATTENTION LED	YELLOW		
	9	149	DS9B3	HOT PLUG POWER LED	GREEN		
	10	205	DS4A1	SATA LED	BLUE		
	11	280	DS3F1	ADR LED	BLUE		
	12	299	DS6E1	CATERR LED	RED		
	13	302	DS2F3	DIMM C-D HOT STATUS LED	YELLOW		
A	14	302	DS2F2	DIMM A-B HOT STATUS LED	YELLOW		
	15	302	DS2F1	CPU0 HOT (PROCHOT) LED	YELLOW		
	16	303	DS8D2	DIMM E-F-G HOT STATUS LED	YELLOW		
	17	303	DS8D1	CPU1 HOT (PROCHOT) LED	YELLOW		
	18	311	DS4E2	PLTRST LED	YELLOW		
	19	311	DS4E1	S3 STATUS LED	YELLOW		
	20	311	DS2D1	PCH CONFIGURE ERROR LED	RED		
8	7	6	5	4	3	2	1
					INTEL CORPORATION		
					5000 W. Chandler Blvd. Chandler, AZ 85226		
					TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
					STATUS LEDs Intel Confidential	SHEET 35 OF 315	

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<b>TITLE</b> Shumway	<b>DOCUMENT NUMBER</b> E97822-100	<b>REV</b> 1.0
<b>TEST HEADERS</b> Intel Confidential	<b>SHEET 36 OF 315</b>	

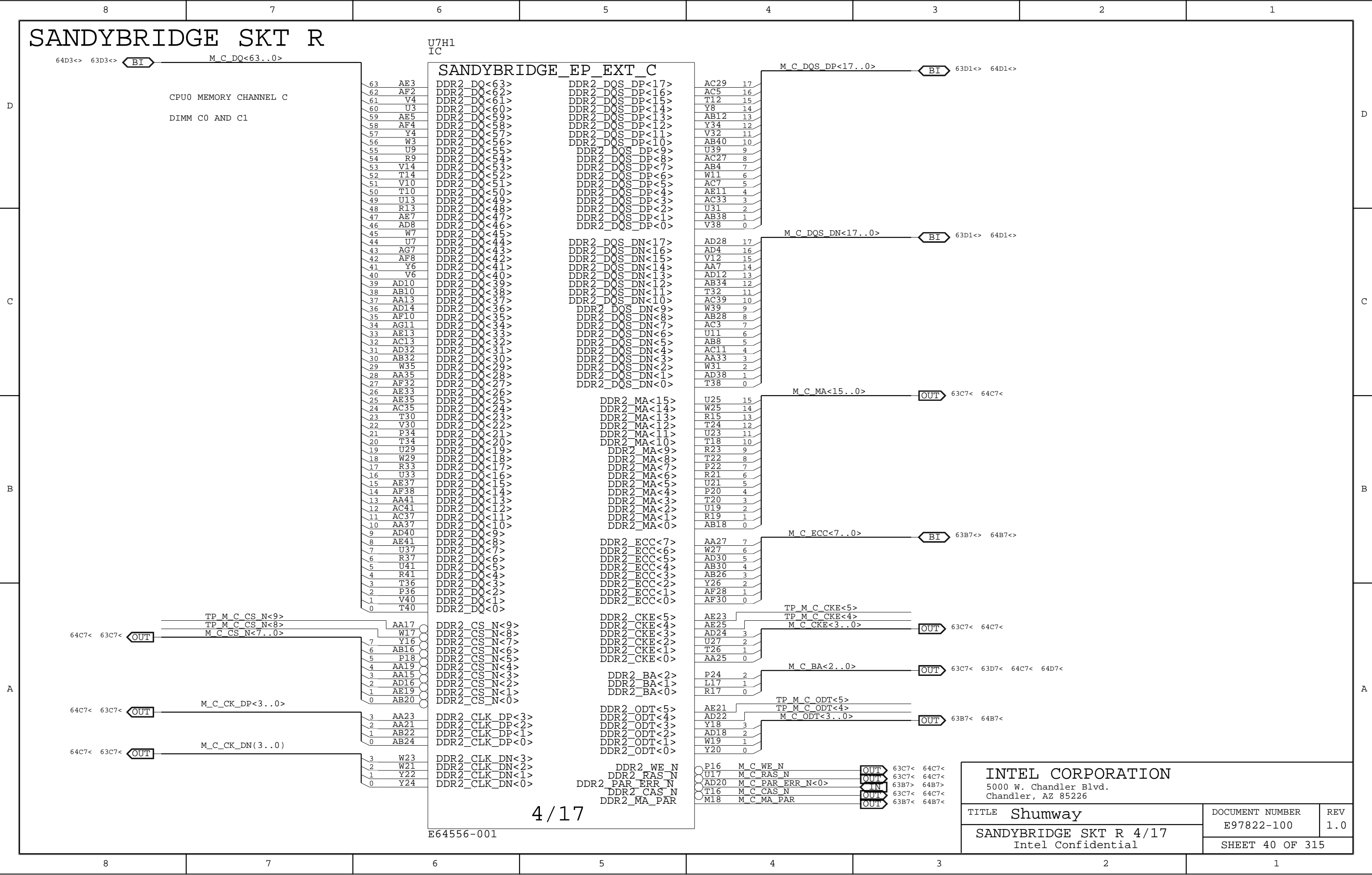


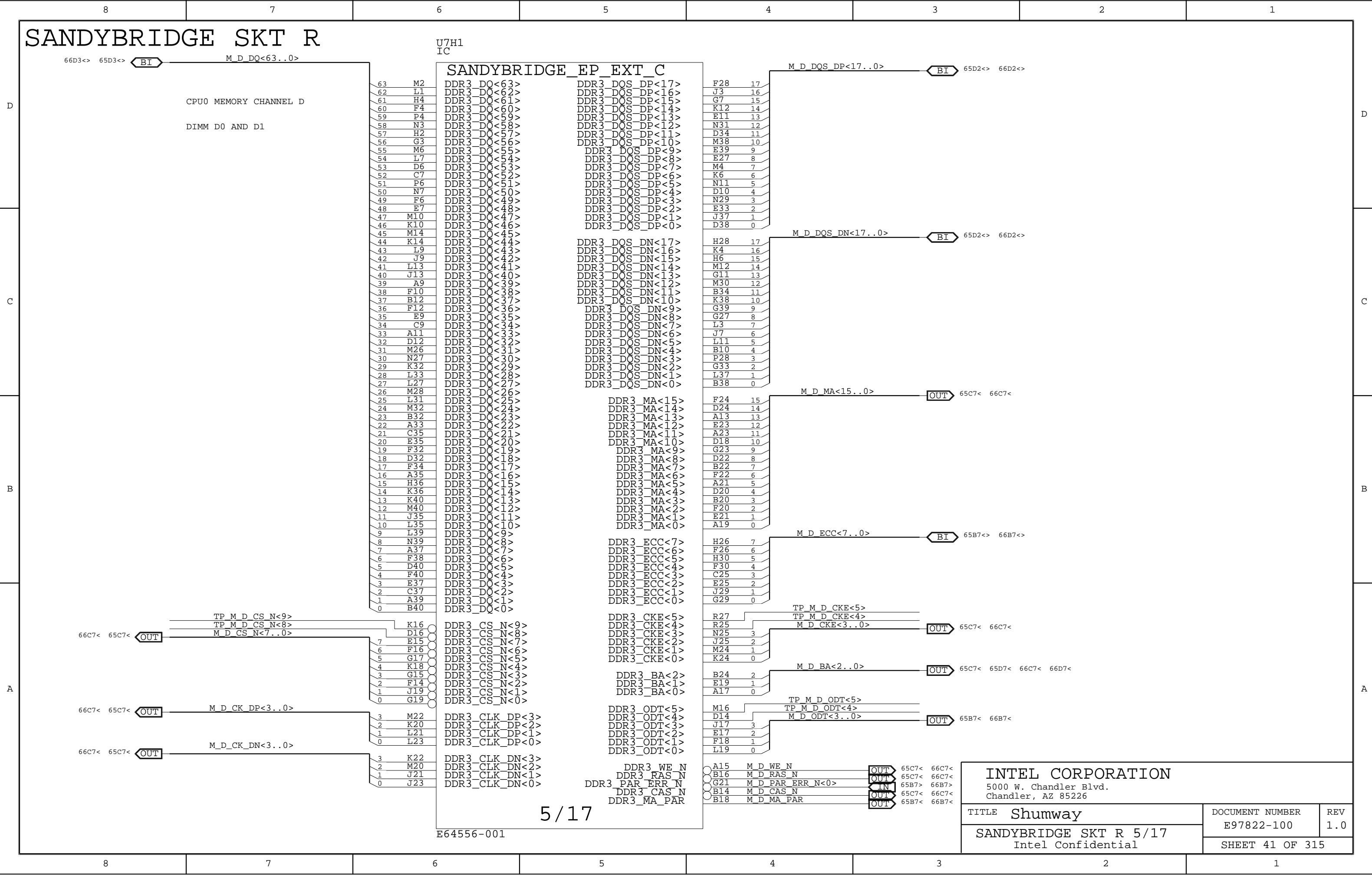


U7H1  
IC

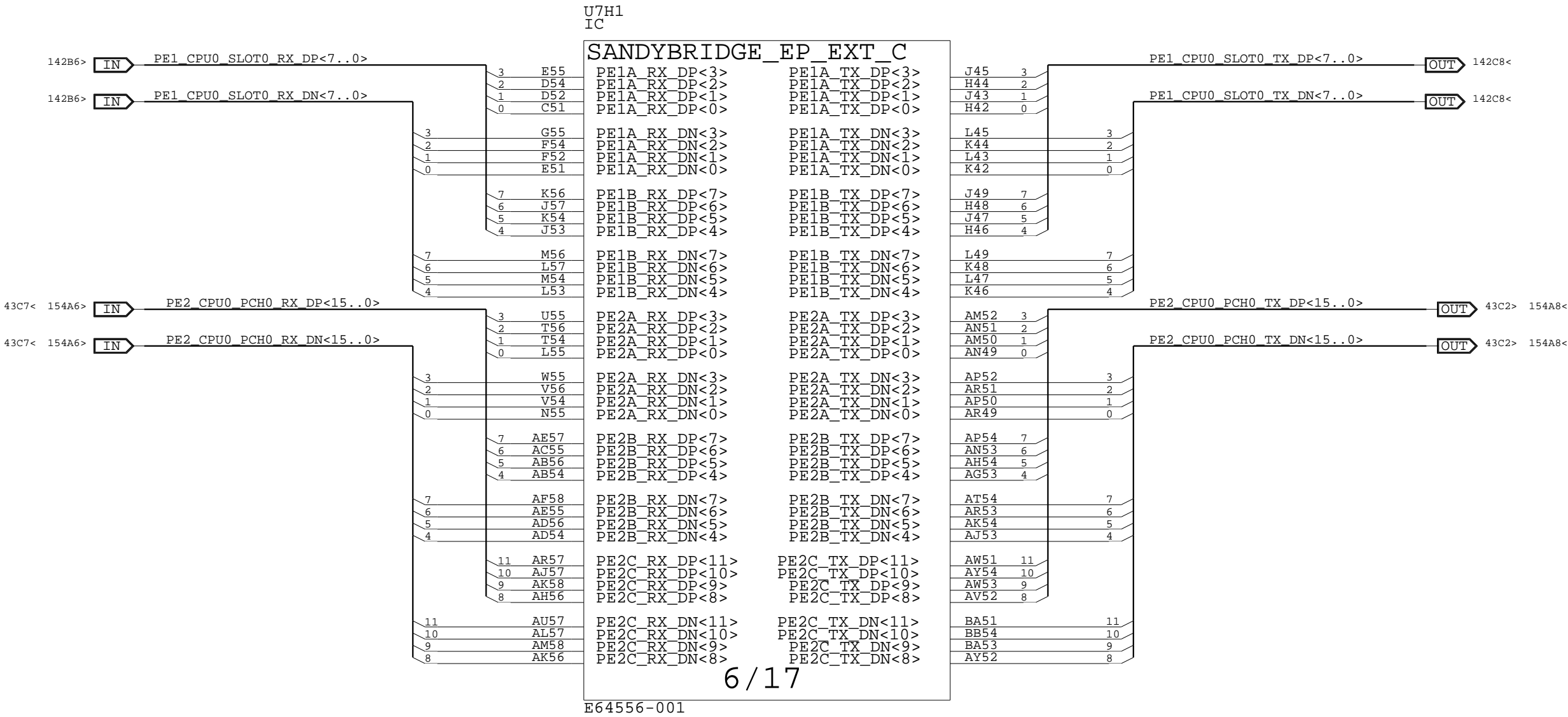
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<b>TITLE</b> Shumway	<b>DOCUMENT NUMBER</b> E97822-100	<b>REV</b> 1.0
SANDYBRIDGE SKT R 3/17 Intel Confidential	SHEET 39 OF 315	





SANDYBRIDGE SKT R



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SANDYBRIDGE SKT R 6/17  
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DOCUMENT NUMBER

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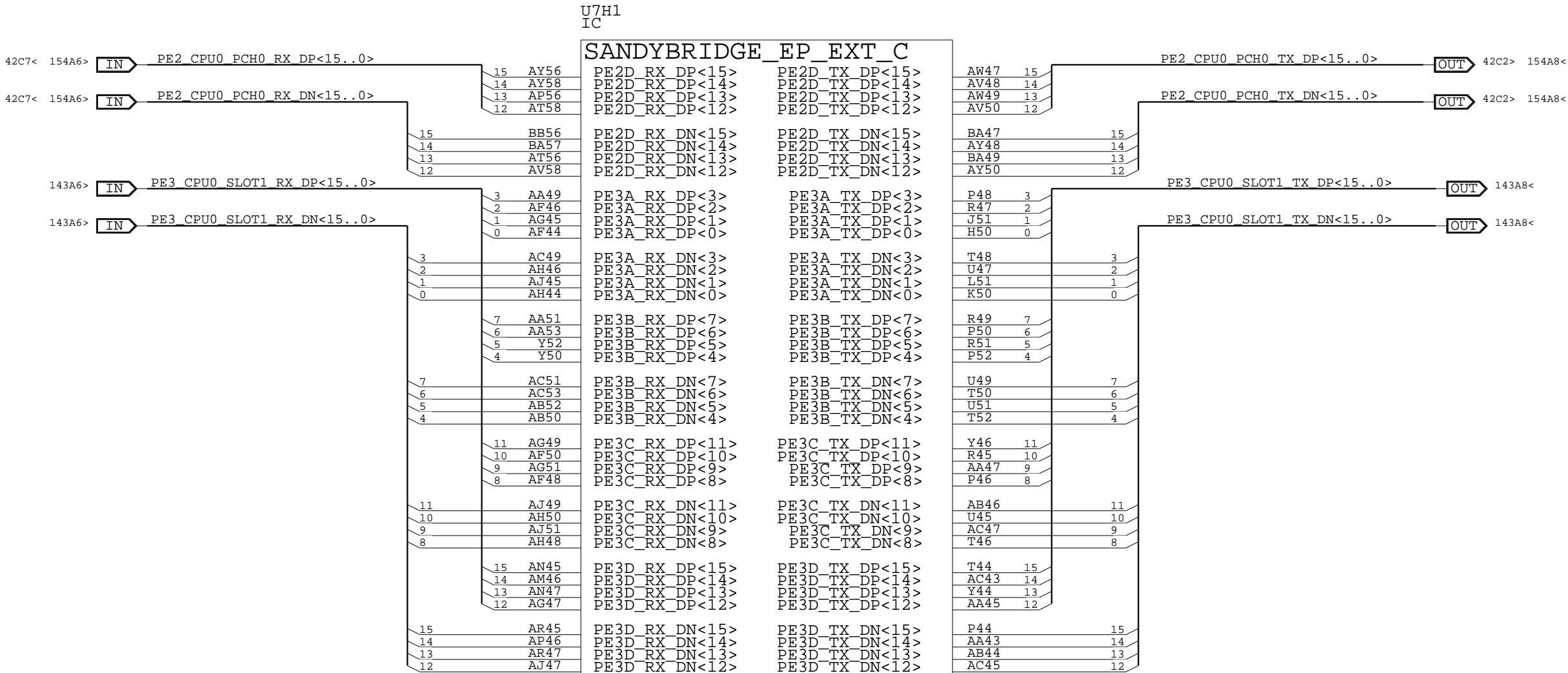
REV

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SANDYBRIDGE SKT R



7/17

E64556-001

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TITLE Shumway

SANDYBRIDGE SKT R 7/17  
Intel Confidential

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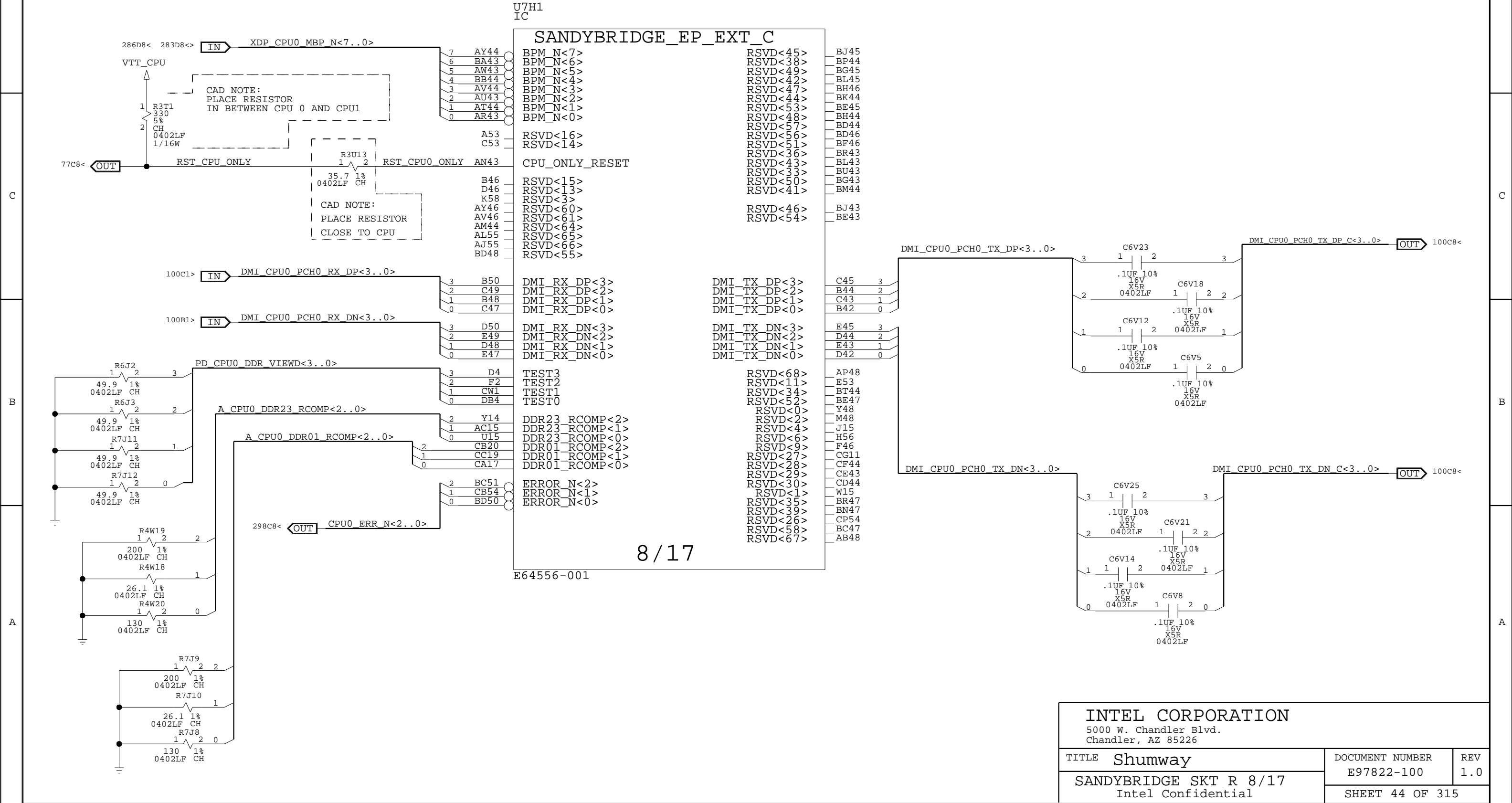
E97822-100

REV

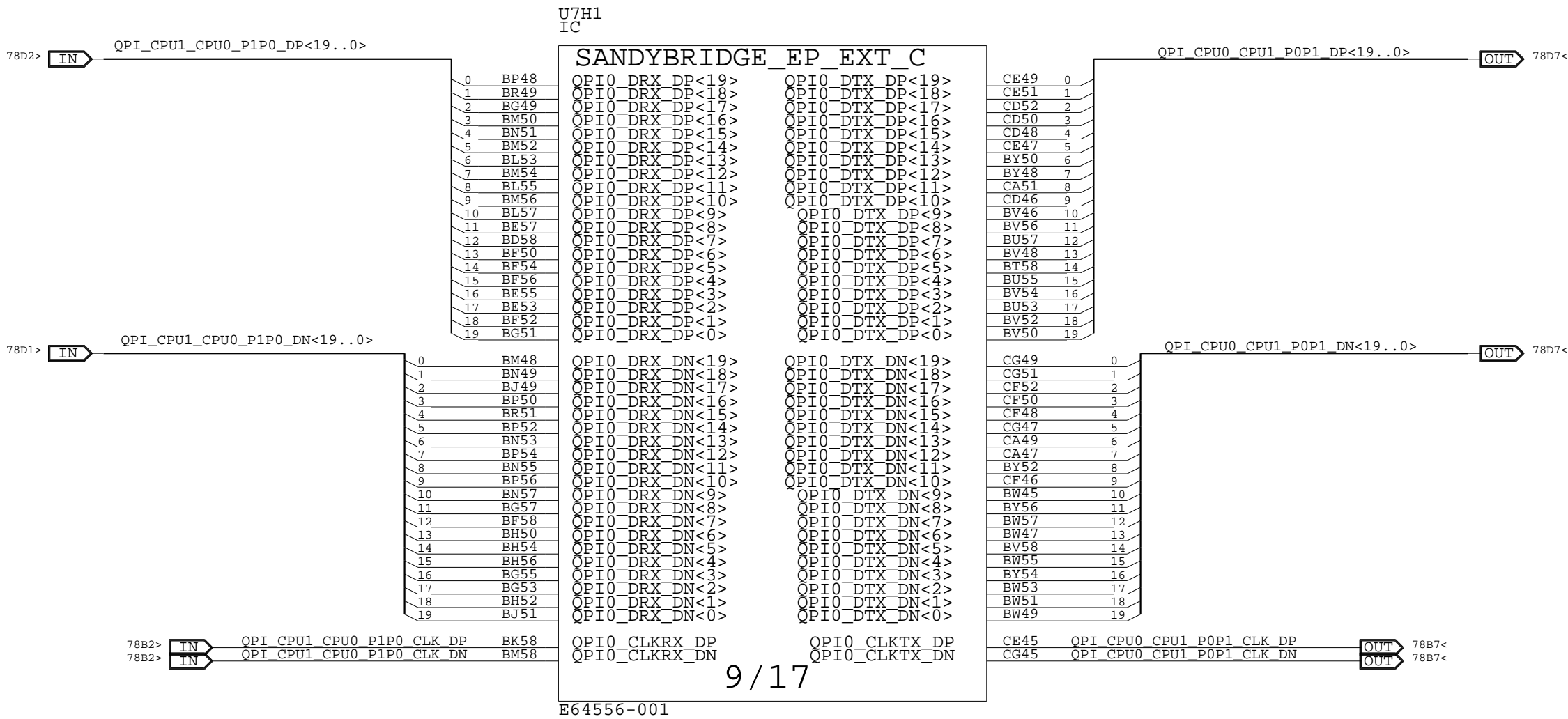
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D	SANDYBRIDGE SKT R	D
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SANDYBRIDGE SKT R



SANDYBRIDGE SKT R

UNUSED QPI

U7H1  
IC

SANDYBRIDGE_EP_EXT_C		
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CK46	OPI1_DRX_DP<18>	OPI1_DTX_DP<18>
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CK48	OPI1_DRX_DP<16>	OPI1_DTX_DP<16>
CN49	OPI1_DRX_DP<15>	OPI1_DTX_DP<15>
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CU53	OPI1_DRX_DP<11>	OPI1_DTX_DP<11>
CK52	OPI1_DRX_DP<10>	OPI1_DTX_DP<10>
CJ53	OPI1_DRX_DP<9>	OPI1_DTX_DP<9>
CT56	OPI1_DRX_DP<8>	OPI1_DTX_DP<8>
CR57	OPI1_DRX_DP<7>	OPI1_DTX_DP<7>
CP58	OPI1_DRX_DP<6>	OPI1_DTX_DP<6>
CK54	OPI1_DRX_DP<5>	OPI1_DTX_DP<5>
CK56	OPI1_DRX_DP<4>	OPI1_DTX_DP<4>
CJ55	OPI1_DRX_DP<3>	OPI1_DTX_DP<3>
CD54	OPI1_DRX_DP<2>	OPI1_DTX_DP<2>
CD56	OPI1_DRX_DP<1>	OPI1_DTX_DP<1>
CC55	OPI1_DRX_DP<0>	OPI1_DTX_DP<0>
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CM46	OPI1_DRX_DN<18>	OPI1_DTX_DN<18>
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CM48	OPI1_DRX_DN<16>	OPI1_DTX_DN<16>
CL49	OPI1_DRX_DN<15>	OPI1_DTX_DN<15>
CK50	OPI1_DRX_DN<14>	OPI1_DTX_DN<14>
CL51	OPI1_DRX_DN<13>	OPI1_DTX_DN<13>
CT52	OPI1_DRX_DN<12>	OPI1_DTX_DN<12>
CR53	OPI1_DRX_DN<11>	OPI1_DTX_DN<11>
CM52	OPI1_DRX_DN<10>	OPI1_DTX_DN<10>
CL53	OPI1_DRX_DN<9>	OPI1_DTX_DN<9>
CV56	OPI1_DRX_DN<8>	OPI1_DTX_DN<8>
CU57	OPI1_DRX_DN<7>	OPI1_DTX_DN<7>
CT58	OPI1_DRX_DN<6>	OPI1_DTX_DN<6>
CM54	OPI1_DRX_DN<5>	OPI1_DTX_DN<5>
CM56	OPI1_DRX_DN<4>	OPI1_DTX_DN<4>
CL55	OPI1_DRX_DN<3>	OPI1_DTX_DN<3>
CF54	OPI1_DRX_DN<2>	OPI1_DTX_DN<2>
CF56	OPI1_DRX_DN<1>	OPI1_DTX_DN<1>
CE55	OPI1_DRX_DN<0>	OPI1_DTX_DN<0>
CR55	OPI1_CLKRX_DP	OPI1_CLKTX_DP
CU55	OPI1_CLKRX_DN	OPI1_CLKTX_DN

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SANDYBRIDGE SKT R

VCC\_CPU0

U7H1  
IC

SANDYBRIDGE\_EP\_EXT\_C

CA29	VCC<207>	VCC<155>
CA25	VCC<206>	VCC<154>
BY40	VCC<205>	VCC<153>
BY38	VCC<204>	VCC<152>
BY36	VCC<203>	VCC<151>
BY34	VCC<202>	VCC<150>
BY32	VCC<201>	VCC<149>
BY30	VCC<200>	VCC<148>
BY28	VCC<199>	VCC<147>
BY26	VCC<198>	VCC<146>
BY18	VCC<197>	VCC<145>
BV8	VCC<196>	VCC<144>
BV6	VCC<195>	VCC<143>
BV4	VCC<194>	VCC<142>
BV2	VCC<193>	VCC<141>
BV16	VCC<192>	VCC<140>
BV14	VCC<191>	VCC<139>
BV12	VCC<190>	VCC<138>
BV10	VCC<189>	VCC<137>
BU9	VCC<188>	VCC<136>
BU7	VCC<187>	VCC<135>
BU5	VCC<186>	VCC<134>
BU3	VCC<185>	VCC<133>
BU17	VCC<184>	VCC<132>
BU15	VCC<183>	VCC<131>
BU13	VCC<182>	VCC<130>
BU11	VCC<181>	VCC<129>
BU1	VCC<180>	VCC<128>
BT8	VCC<179>	VCC<127>
BT6	VCC<178>	VCC<126>
BT4	VCC<177>	VCC<125>
BT2	VCC<176>	VCC<124>
BT16	VCC<175>	VCC<123>
BT14	VCC<174>	VCC<122>
BT12	VCC<173>	VCC<121>
BT10	VCC<172>	VCC<120>
BR9	VCC<171>	VCC<119>
BR7	VCC<170>	VCC<118>
BR5	VCC<169>	VCC<117>
BR3	VCC<168>	VCC<116>
BR17	VCC<167>	VCC<115>
BR15	VCC<166>	VCC<114>
BR13	VCC<165>	VCC<113>
BR11	VCC<164>	VCC<112>
BR1	VCC<163>	VCC<111>
BP8	VCC<162>	VCC<110>
BP6	VCC<161>	VCC<109>
BP4	VCC<160>	VCC<108>
BP2	VCC<159>	VCC<107>
BP16	VCC<158>	VCC<106>
BP14	VCC<157>	VCC<105>
BP12	VCC<156>	VCC<104>

VCC\_CPU0

BP10

BN9
BN7
BN5
BN3
BN17
BN15
BN13
BN11
BN1
BK8
BK6
BK4
BK2
BK16
BK14
BK12
BK10
BJ9
BJ7
BJ5
BJ3
BJ17
BJ15
BJ13
BJ11
BJ1
BH8
BH6
BH4
BH2
BH16
BH14
BH12
BH10
BG9
BG7
BG5
BG3
BG17
BG15
BG13
BG11
BG1
BF8
BF6
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BF2
BF16
BF14
BF12
BF10

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VCC\_CPU0

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IC

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BE9	VCC<103>	VCC<51>
BE7	VCC<102>	VCC<50>
BE5	VCC<101>	VCC<49>
BE3	VCC<100>	VCC<48>
BE17	VCC<99>	VCC<47>
BE15	VCC<98>	VCC<46>
BE13	VCC<97>	VCC<45>
BE11	VCC<96>	VCC<44>
BE1	VCC<95>	VCC<43>
BB8	VCC<94>	VCC<42>
BB6	VCC<93>	VCC<41>
BB4	VCC<92>	VCC<40>
BB2	VCC<91>	VCC<39>
BB16	VCC<90>	VCC<38>
BB14	VCC<89>	VCC<37>
BB12	VCC<88>	VCC<36>
BB10	VCC<87>	VCC<35>
BA9	VCC<86>	VCC<34>
BA7	VCC<85>	VCC<33>
BA5	VCC<84>	VCC<32>
BA3	VCC<83>	VCC<31>
BA17	VCC<82>	VCC<30>
BA15	VCC<81>	VCC<29>
BA13	VCC<80>	VCC<28>
BA11	VCC<79>	VCC<27>
BA1	VCC<78>	VCC<26>
AY8	VCC<77>	VCC<25>
AY6	VCC<76>	VCC<24>
AY4	VCC<75>	VCC<23>
AY2	VCC<74>	VCC<22>
AY16	VCC<73>	VCC<21>
AY14	VCC<72>	VCC<20>
AY12	VCC<71>	VCC<19>
AY10	VCC<70>	VCC<18>
AW9	VCC<69>	VCC<17>
AW7	VCC<68>	VCC<16>
AW5	VCC<67>	VCC<15>
AW3	VCC<66>	VCC<14>
AW17	VCC<65>	VCC<13>
AW15	VCC<64>	VCC<12>
AW13	VCC<63>	VCC<11>
AW11	VCC<62>	VCC<10>
AW1	VCC<61>	VCC<9>
AV8	VCC<60>	VCC<8>
AV6	VCC<59>	VCC<7>
AV4	VCC<58>	VCC<6>
AV2	VCC<57>	VCC<5>
AV16	VCC<56>	VCC<4>
AV14	VCC<55>	VCC<3>
AV12	VCC<54>	VCC<2>
AV10	VCC<53>	VCC<1>
AU9	VCC<52>	VCC<0>

VCC\_CPU0

AU7

AU5
AU3
AU17
AU15
AU13
AU11
AU1
AP8
AP6
AP4
AP2
AP16
AP14
AP12
AP10
AN9
AN7
AN5
AN3
AN17
AN15
AN13
AN11
AN1
AM8
AM6
AM4
AM2
AM16
AM14
AM12
AM10
AL9
AL7
AL5
AL3
AL17
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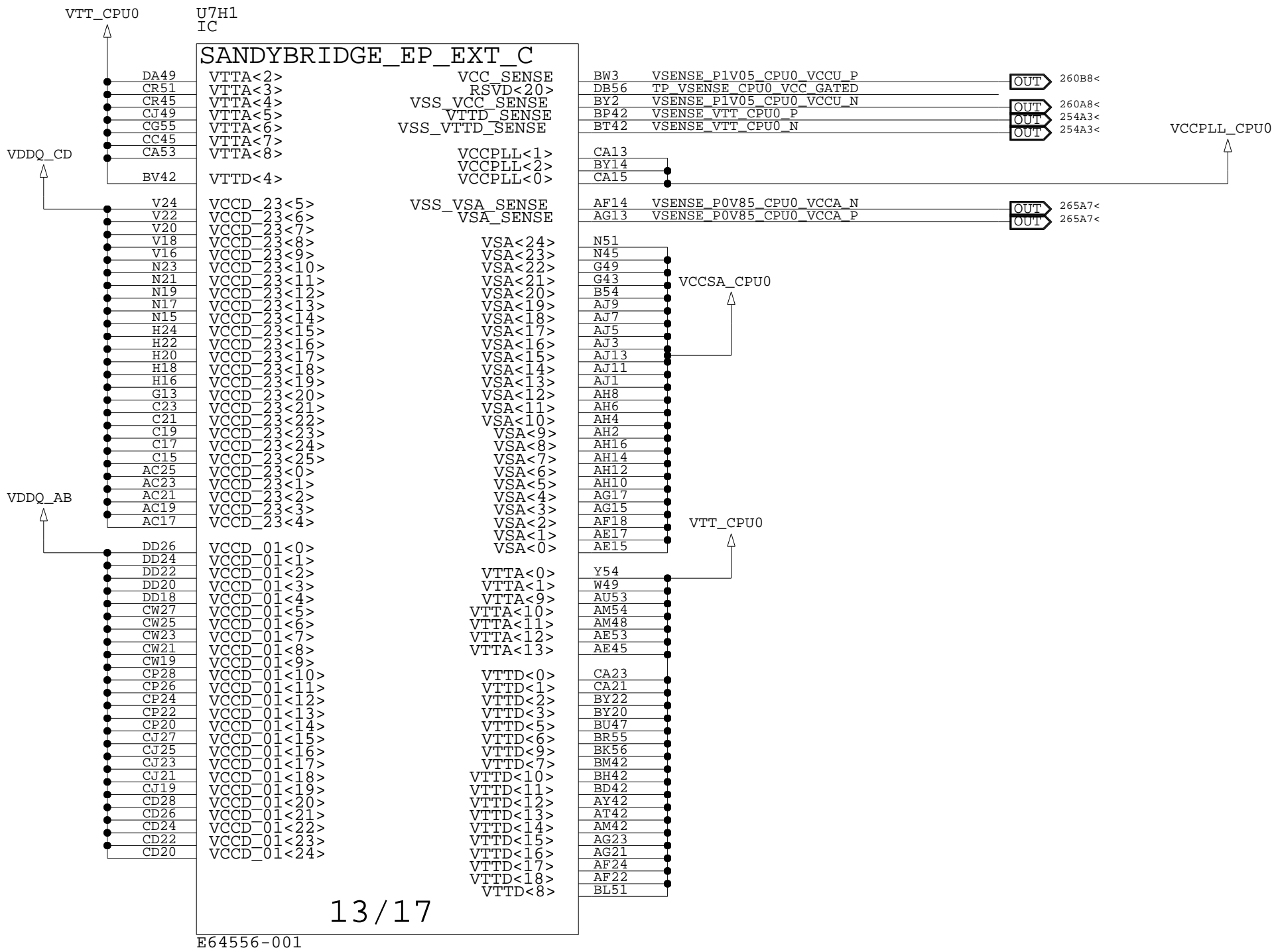
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SANDYBRIDGE SKT R



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SANDYBRIDGE SKT R

U7H1  
IC

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CY40	VSS<547>	N9
AW55	VSS<546>	N53
AG43	VSS<545>	N5
CW51	VSS<544>	N49
C3	VSS<543>	N47
D2	VSS<542>	N43
DB2	VSS<541>	N41
DC3	VSS<540>	N37
E1	VSS<539>	N35
V46	VSS<538>	N33
BG47	VSS<537>	N13
BK50	VSS<536>	M8
AU51	VSS<535>	M52
Y56	VSS<534>	M50
Y42	VSS<533>	M46
Y40	VSS<532>	M44
Y38	VSS<531>	M42
Y36	VSS<530>	M36
Y32	VSS<529>	M34
Y30	VSS<528>	L5
Y28	VSS<527>	L41
Y12	VSS<526>	L29
Y10	VSS<525>	L25
W9	VSS<524>	K8
W53	VSS<523>	K34
W51	VSS<522>	K30
W5	VSS<521>	K28
W47	VSS<520>	K2
W45	VSS<519>	J55
W43	VSS<518>	J5
W41	VSS<517>	J41
W37	VSS<516>	J39
W33	VSS<515>	J33
W13	VSS<514>	J31
V8	VSS<513>	J27
V50	VSS<512>	J11
V48	VSS<511>	H8
V44	VSS<510>	H54
V42	VSS<509>	H52
V36	VSS<508>	H40
V34	VSS<507>	H38
V28	VSS<506>	H34
V26	VSS<505>	H32
U5	VSS<504>	K26
U35	VSS<503>	H14
T8	VSS<502>	H12
T6	VSS<501>	H10
T42	VSS<500>	G9
T4	VSS<499>	G57
T28	VSS<498>	G53
R7	VSS<497>	G51
R55	VSS<496>	G5
R5	VSS<495>	G47
R39	VSS<494>	G45
R35	VSS<493>	G41
R31	VSS<492>	G37
R3	VSS<491>	G35
R29	VSS<490>	G31
R11	VSS<489>	G1
P8	VSS<488>	F8
P56	VSS<487>	F50
P54	VSS<486>	F48
P40	VSS<485>	F44
P38	VSS<484>	F42
P32	VSS<483>	F36
P30	VSS<482>	G25
P26	VSS<481>	E5
P14	VSS<480>	E41
P12	VSS<479>	
P10	VSS<478>	

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U7H1  
IC

SANDYBRIDGE\_EP\_EXT\_C

E31	VSS<409>	VSS<341>	CV34
E3	VSS<408>	VSS<340>	CV32
E29	VSS<407>	VSS<339>	CV30
DF8	VSS<406>	VSS<338>	CV18
DF52	VSS<405>	VSS<337>	CV14
DF50	VSS<404>	VSS<336>	CU5
DF48	VSS<403>	VSS<335>	CU35
DF46	VSS<402>	VSS<334>	CU3
DF44	VSS<401>	VSS<333>	CU11
DF42	VSS<400>	VSS<332>	CU1
DF36	VSS<399>	VSS<331>	CT42
DF12	VSS<398>	VSS<330>	CT28
DE7	VSS<397>	VSS<329>	CR9
DE53	VSS<396>	VSS<328>	CR5
DE41	VSS<395>	VSS<327>	CR49
DE17	VSS<394>	VSS<326>	CR47
DD6	VSS<393>	VSS<325>	CR35
DD38	VSS<392>	VSS<324>	CR11
DD36	VSS<391>	VSS<323>	CP56
DD34	VSS<390>	VSS<322>	CP52
DD14	VSS<389>	VSS<321>	CP48
DD12	VSS<388>	VSS<320>	CP46
DD10	VSS<387>	VSS<319>	CP44
DC5	VSS<386>	VSS<318>	CP40
DC41	VSS<385>	VSS<317>	CP36
DB58	VSS<384>	VSS<316>	CP16
		VSS<315>	CP12
		VSS<314>	CN9
DB36	VSS<383>	VSS<313>	CN7
DB32	VSS<382>	VSS<312>	CN57
DB12	VSS<381>	VSS<311>	CN55
DA9	VSS<380>	VSS<310>	CN53
DA51	VSS<379>	VSS<309>	CN5
DA5	VSS<378>	VSS<308>	CP42
DA47	VSS<377>	VSS<307>	CN39
DA45	VSS<376>	VSS<306>	CN37
DA43	VSS<375>	VSS<305>	CN35
DA41	VSS<374>	VSS<304>	CN33
DA3	VSS<373>	VSS<303>	CN31
DA11	VSS<372>	VSS<302>	CN3
D8	VSS<371>	VSS<301>	CN17
D36	VSS<370>	VSS<300>	CN15
D26	VSS<369>	VSS<299>	CN13
CY8	VSS<368>	VSS<298>	CN11
CY50	VSS<367>	VSS<297>	CM8
CY44	VSS<366>	VSS<296>	CM6
CY36	VSS<365>	VSS<295>	CM42
CY2	VSS<364>	VSS<294>	CM40
CY16	VSS<363>	VSS<293>	CM38
CY12	VSS<362>	VSS<292>	CM36
CY10	VSS<361>	VSS<291>	CM34
CW7	VSS<360>	VSS<290>	CM32
CW57	VSS<359>	VSS<289>	CM30
CW55	VSS<358>	VSS<288>	CM14
CW53	VSS<357>	VSS<287>	CM10
CW5	VSS<356>	VSS<286>	CL5
CW39	VSS<355>	VSS<285>	CL43
CW37	VSS<354>	VSS<284>	CL17
CW35	VSS<353>	VSS<283>	CK6
CW33	VSS<352>	VSS<282>	CK4
CW31	VSS<351>	VSS<281>	CK36
CW29	VSS<350>	VSS<280>	CK10
CW15	VSS<349>	VSS<279>	CJ9
CW13	VSS<348>	VSS<278>	CJ51
CW11	VSS<347>	VSS<277>	CJ47
CV6	VSS<346>	VSS<276>	CJ45
CV58	VSS<345>	VSS<275>	CJ43
CV54	VSS<344>	VSS<274>	CJ3
CV42	VSS<343>		
CV38	VSS<342>		

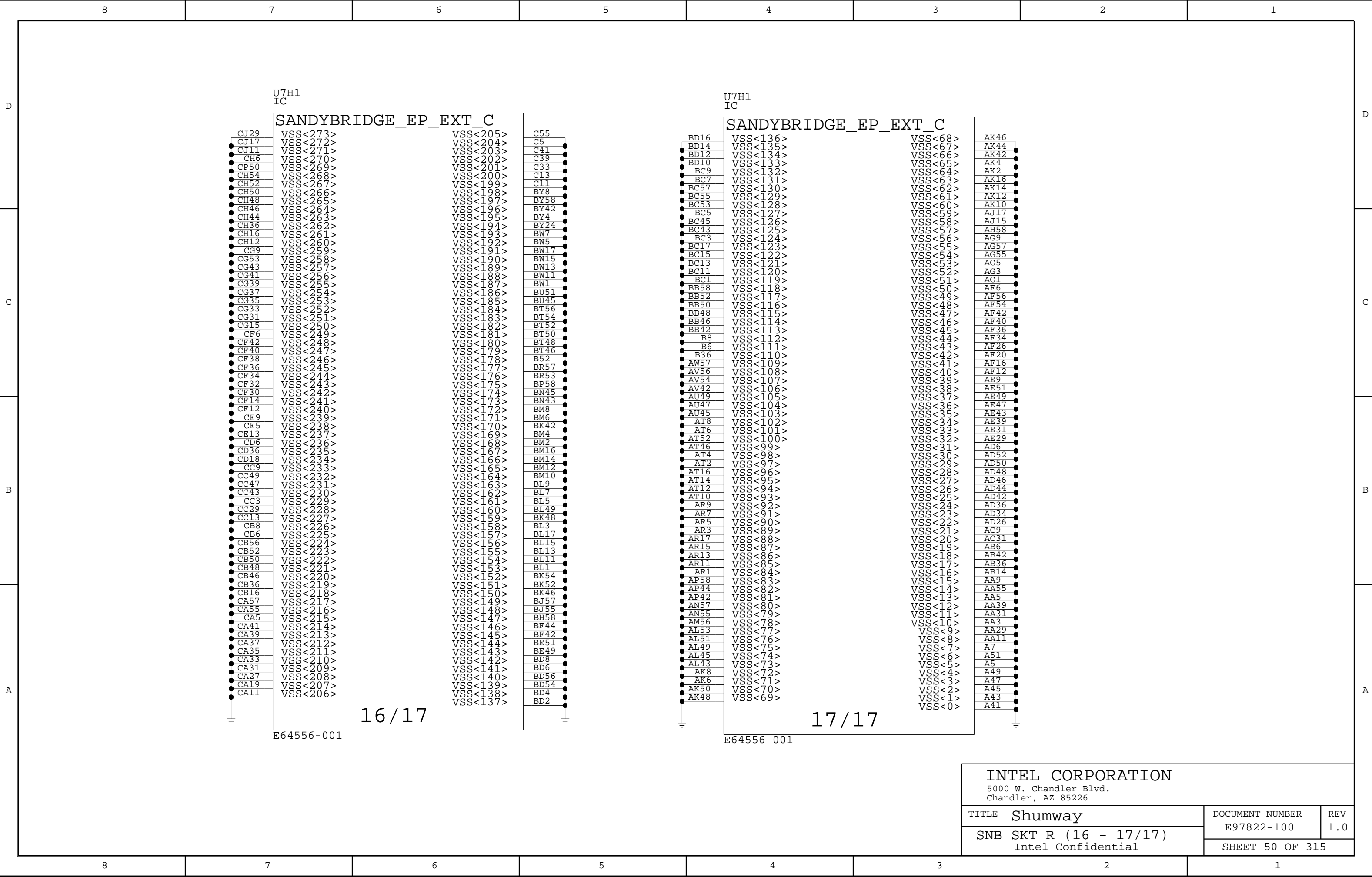
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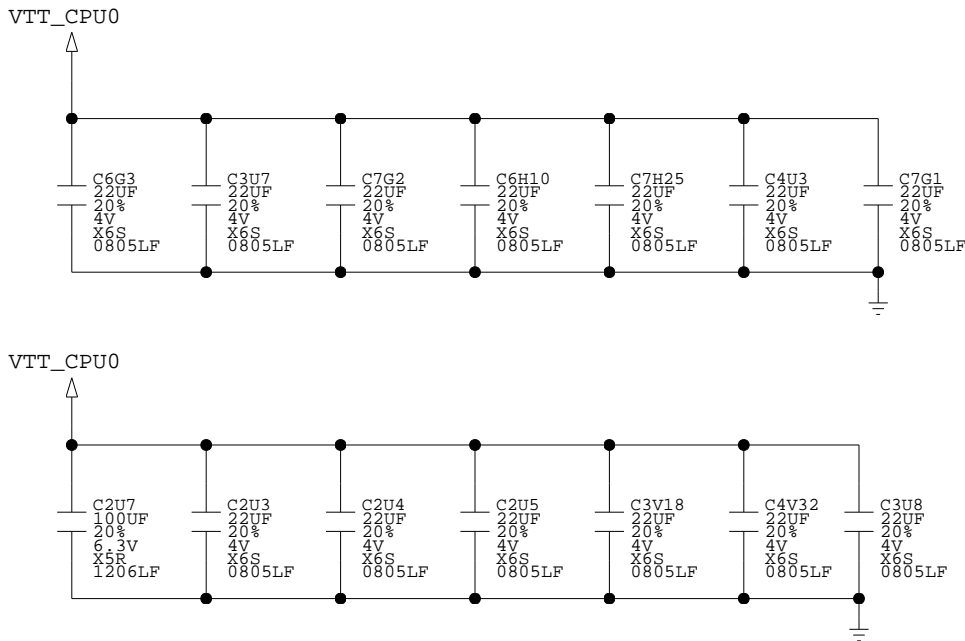
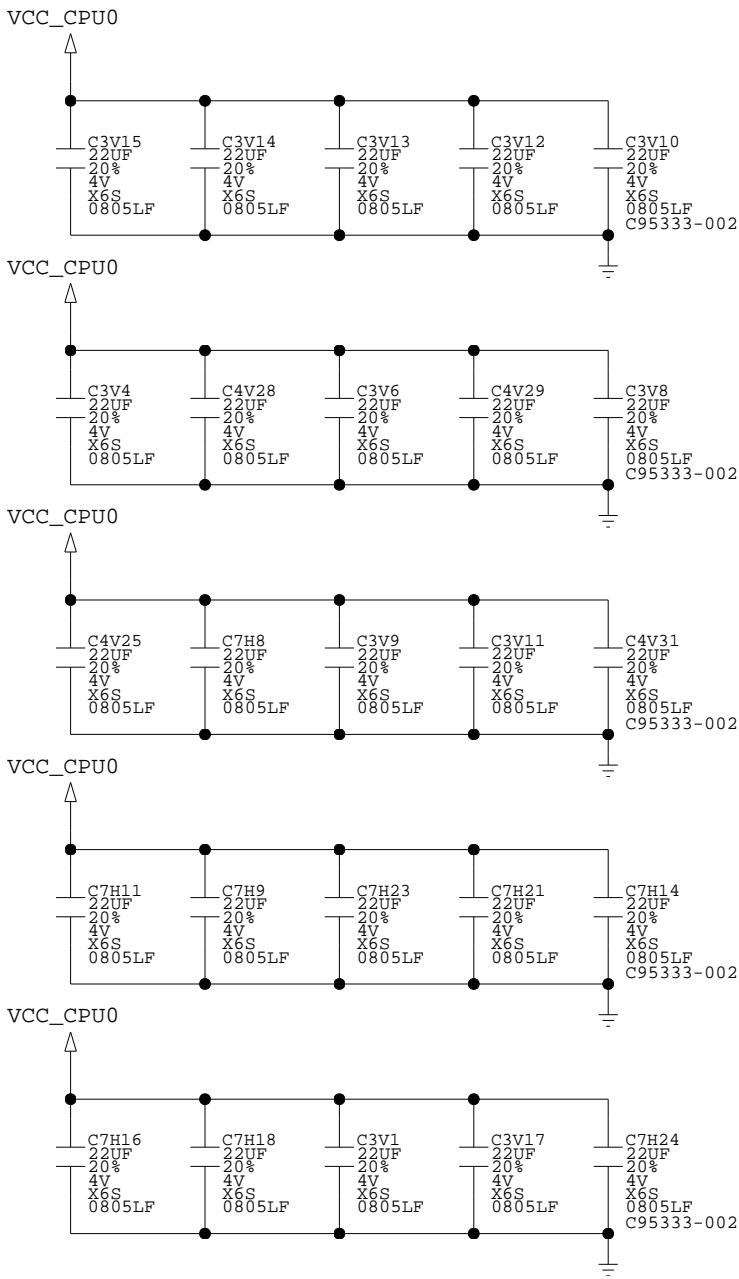
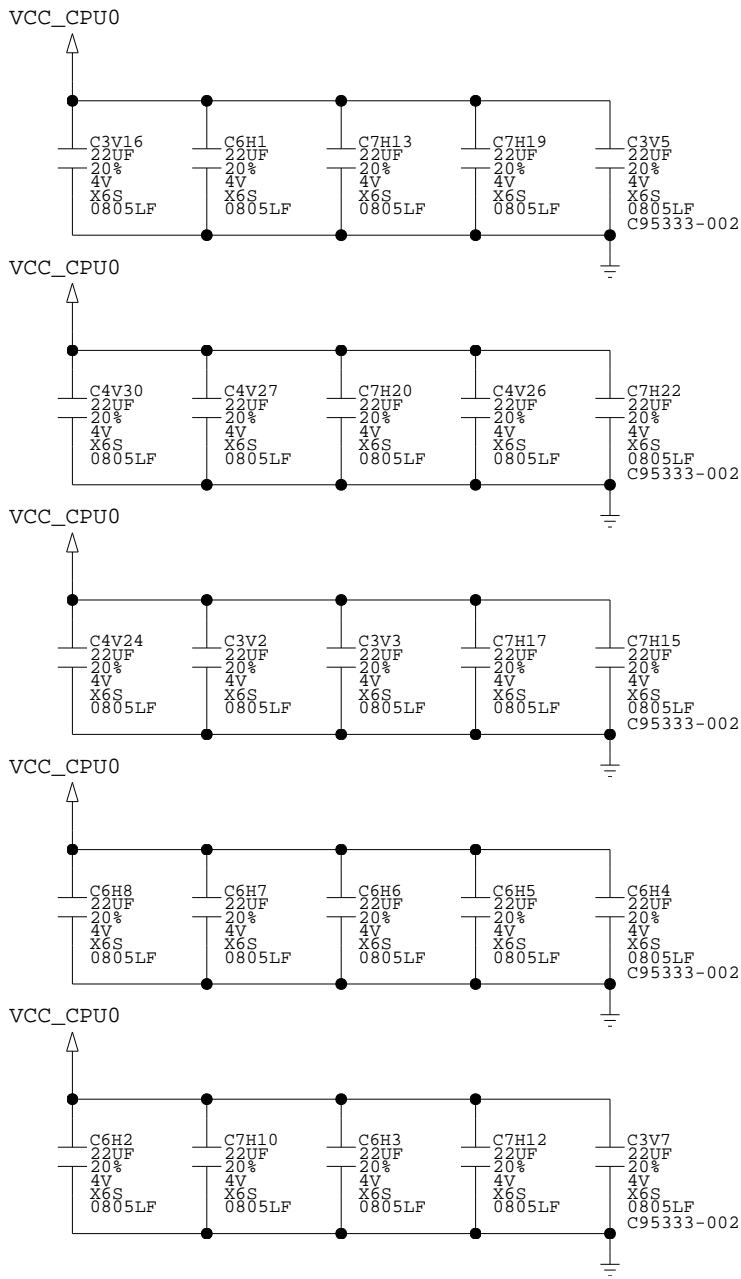
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SANDYBRIDGE SKT R  
DECOUPLING CAP



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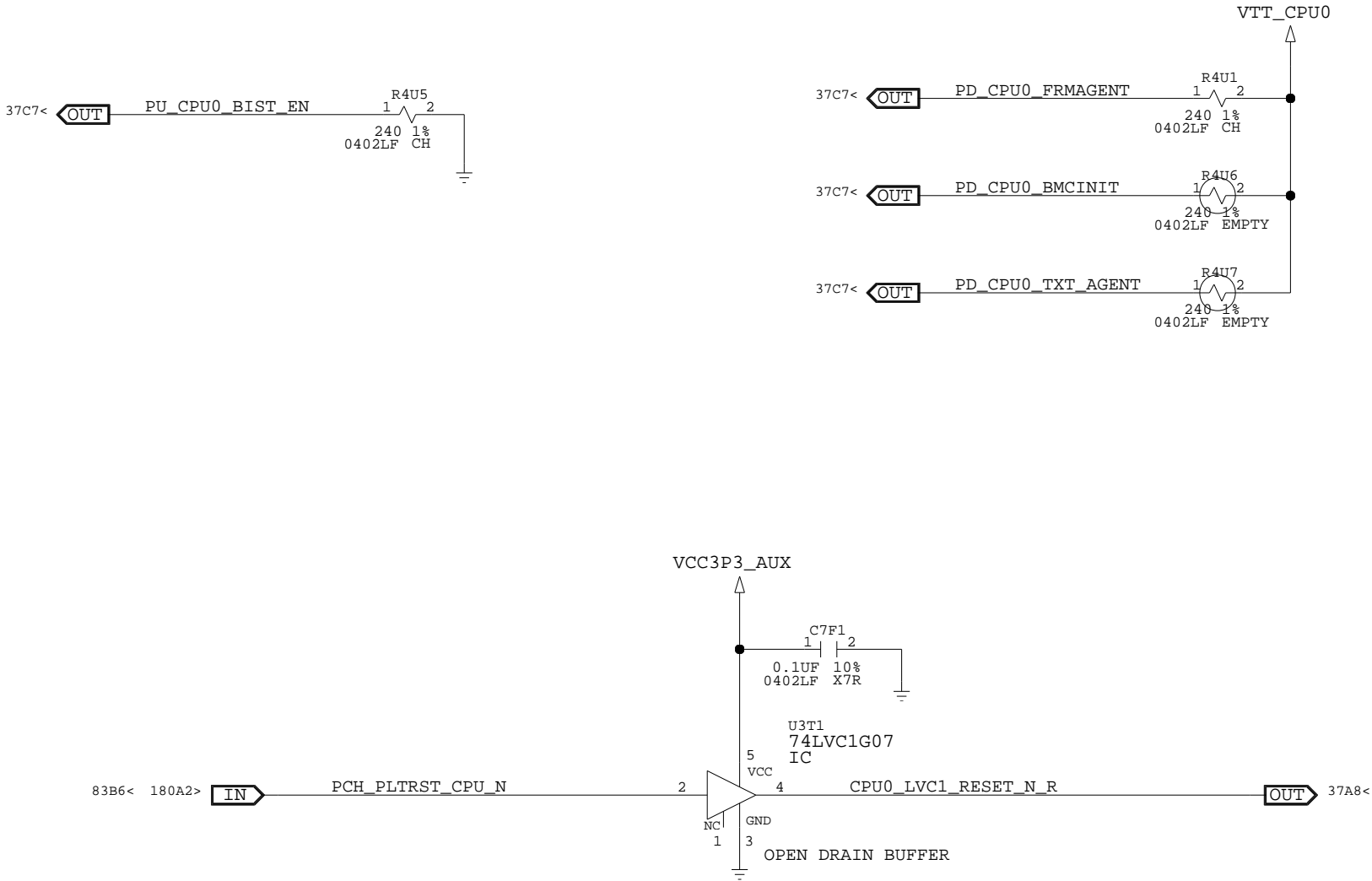
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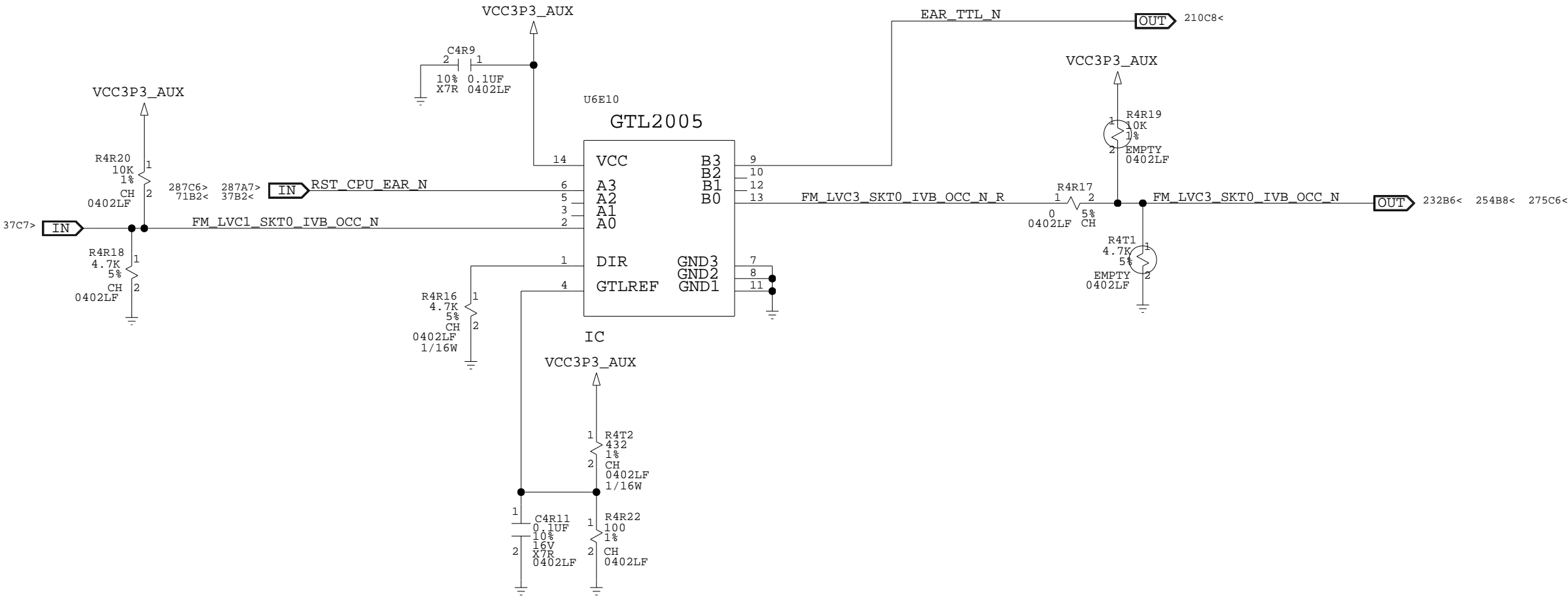
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CAD NOTE:  
PLACE U3T1 CLOSE TO U8D1 (P.83)  
NEED MATCH LENGHT BETWEEN  
CPU0\_LVC1\_RESET\_N\_R AND CPU1\_LVC1\_RESET\_N\_R

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## CPU0 DIMM CHANNELS

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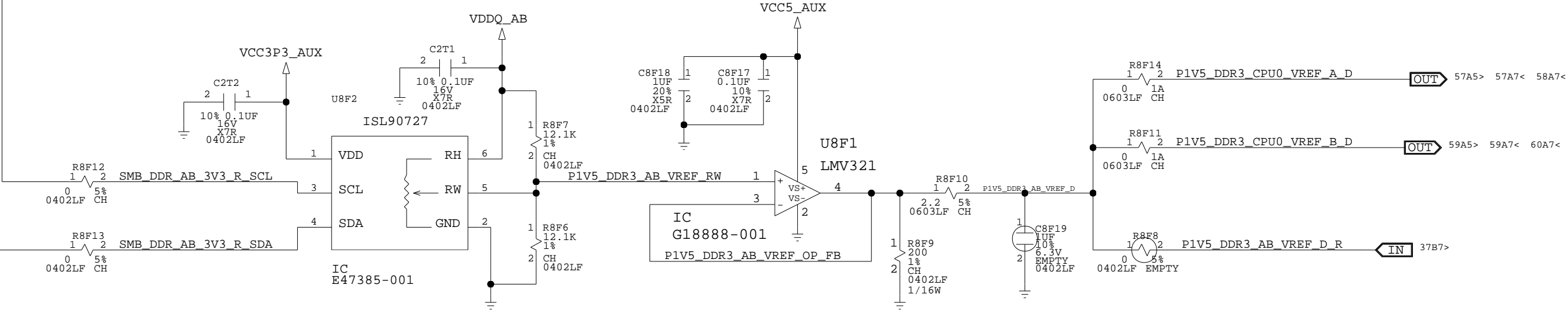
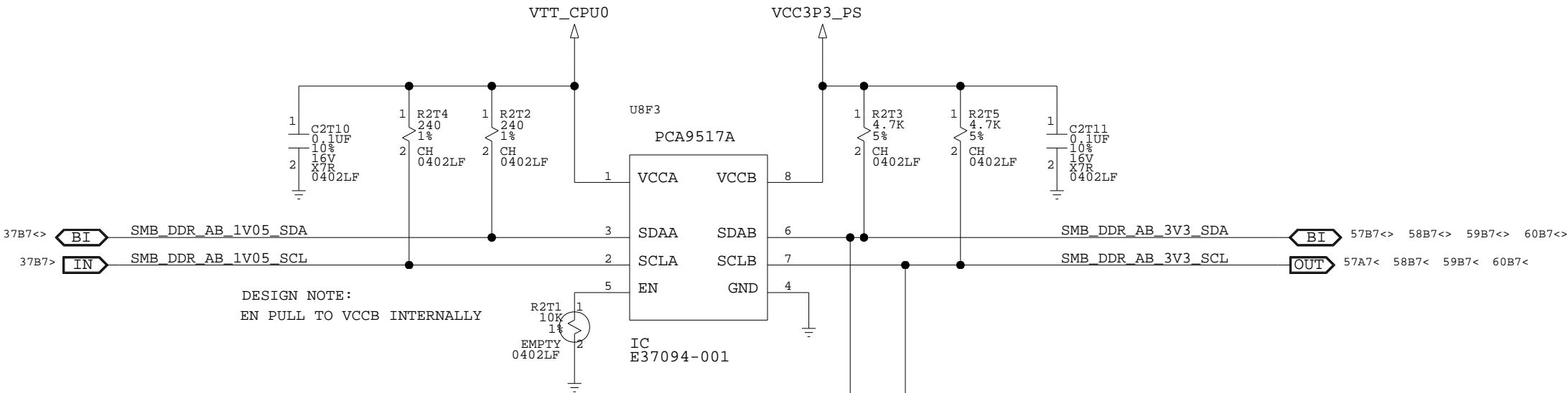
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SEC - CPU0 DIMM CHANNELS  
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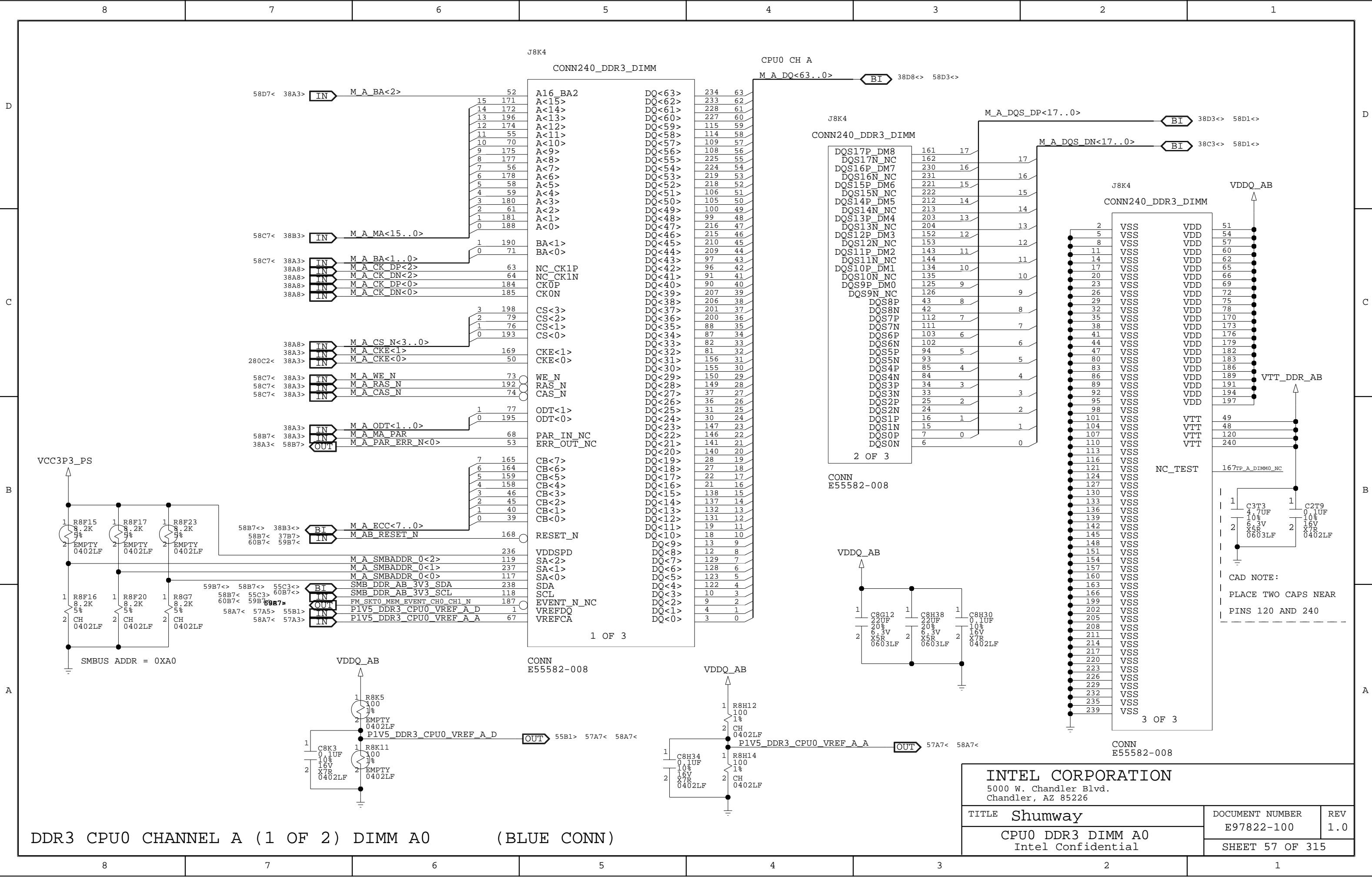
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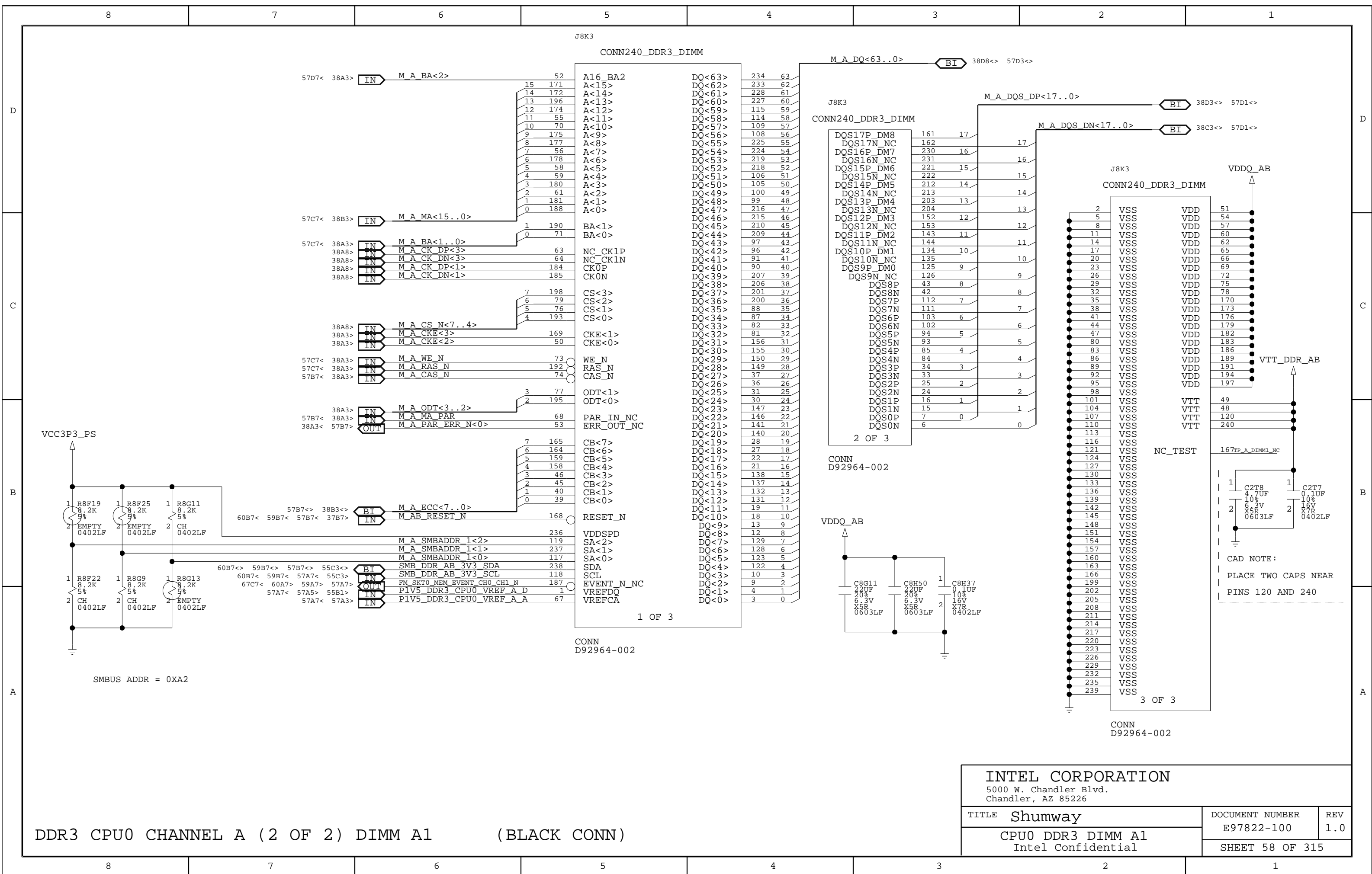
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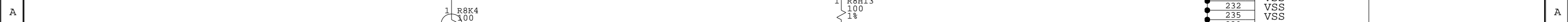
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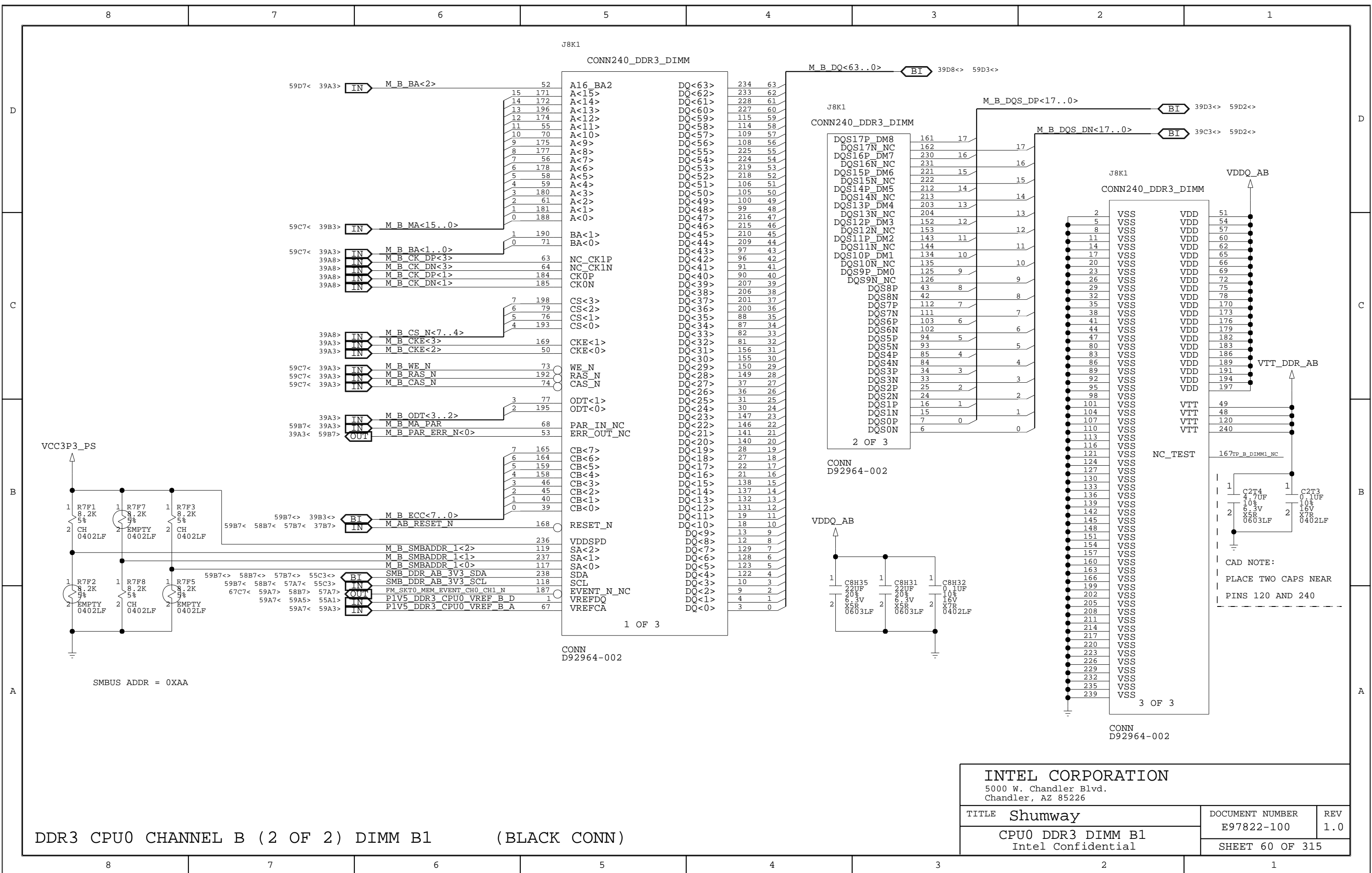
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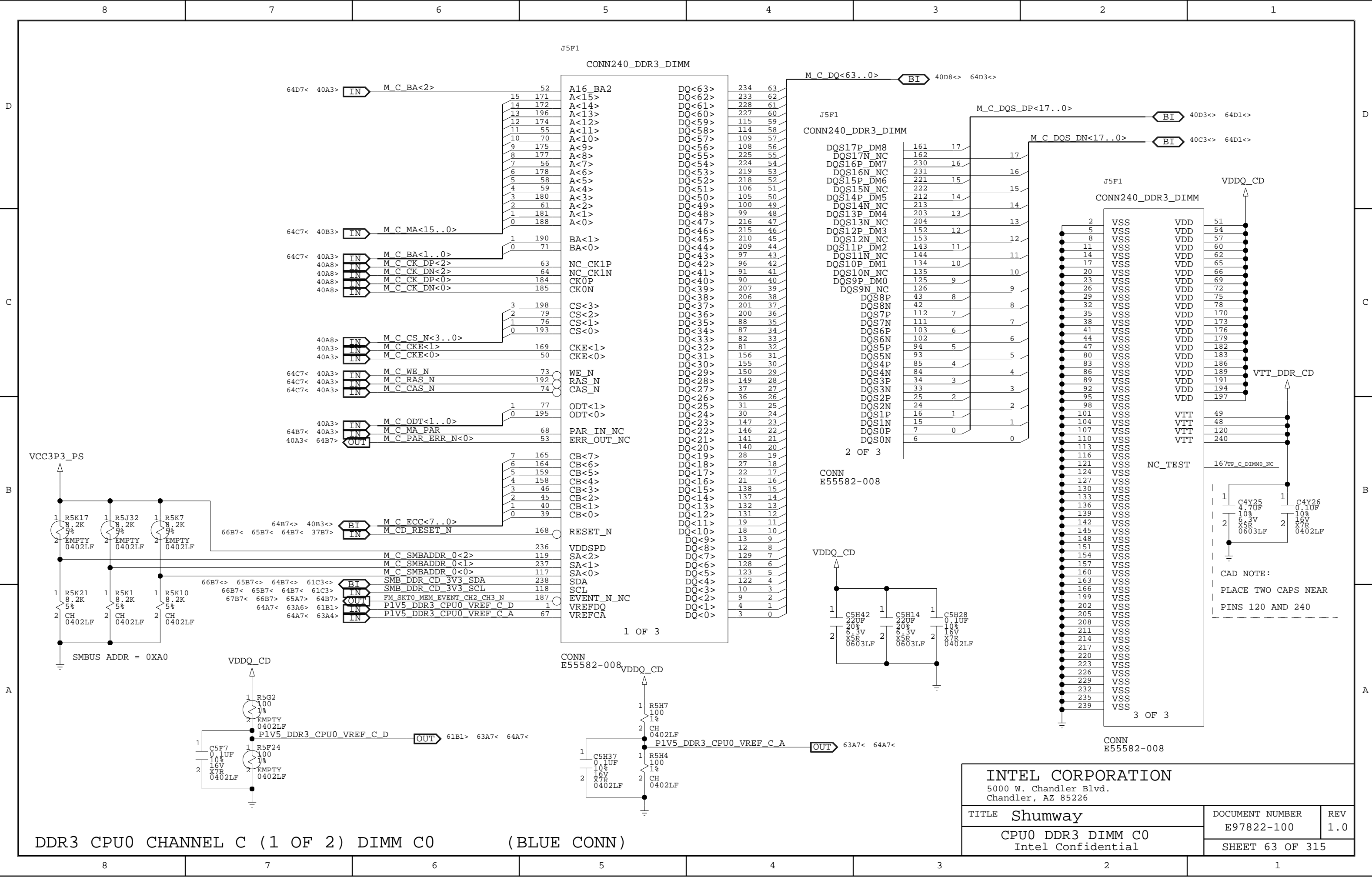


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A							
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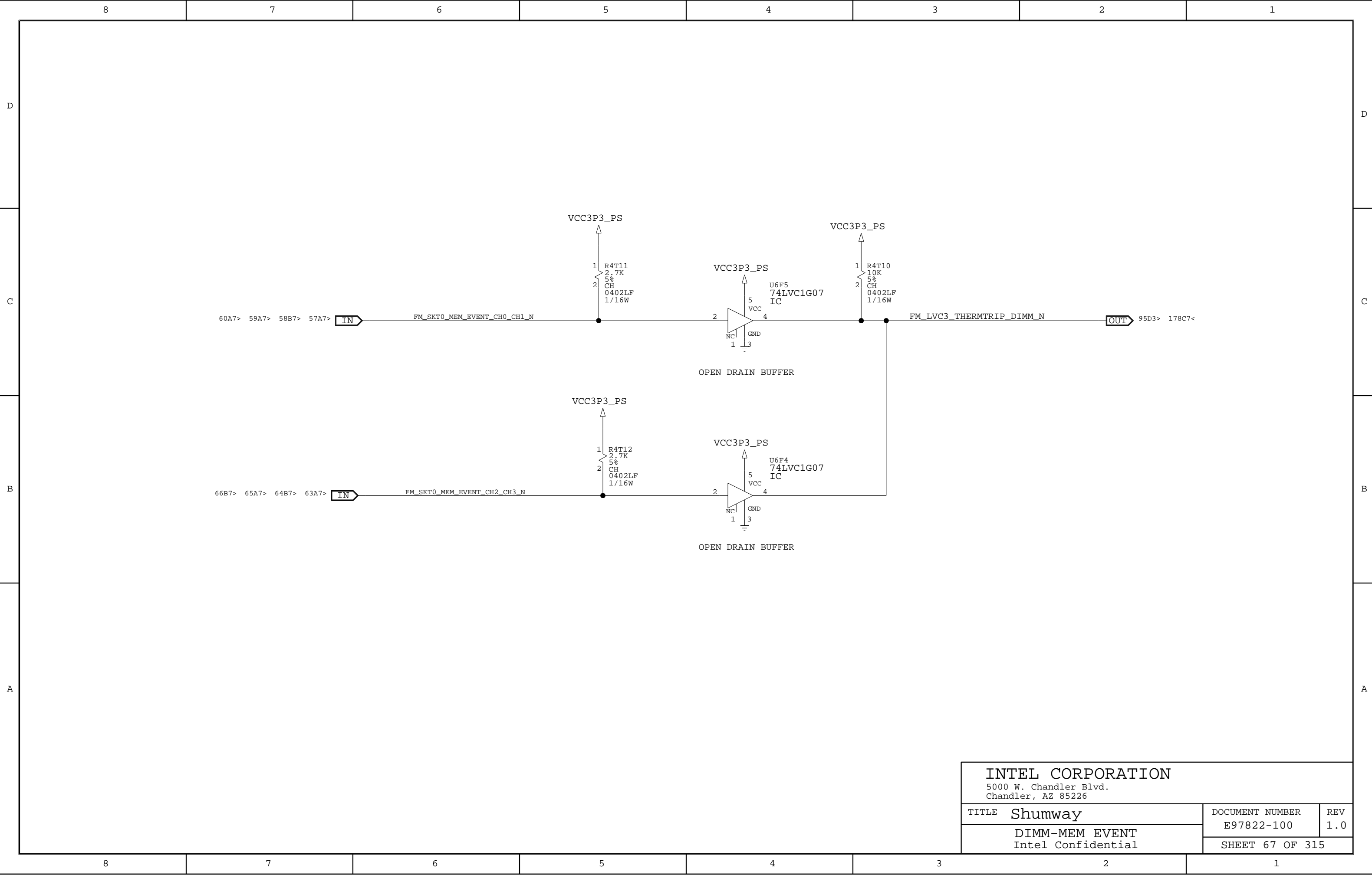




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TITLE	Shumway	DOCUMENT NUMBER	REV
CPU0 DDR3 DIMM D1		E97822-100	1.0
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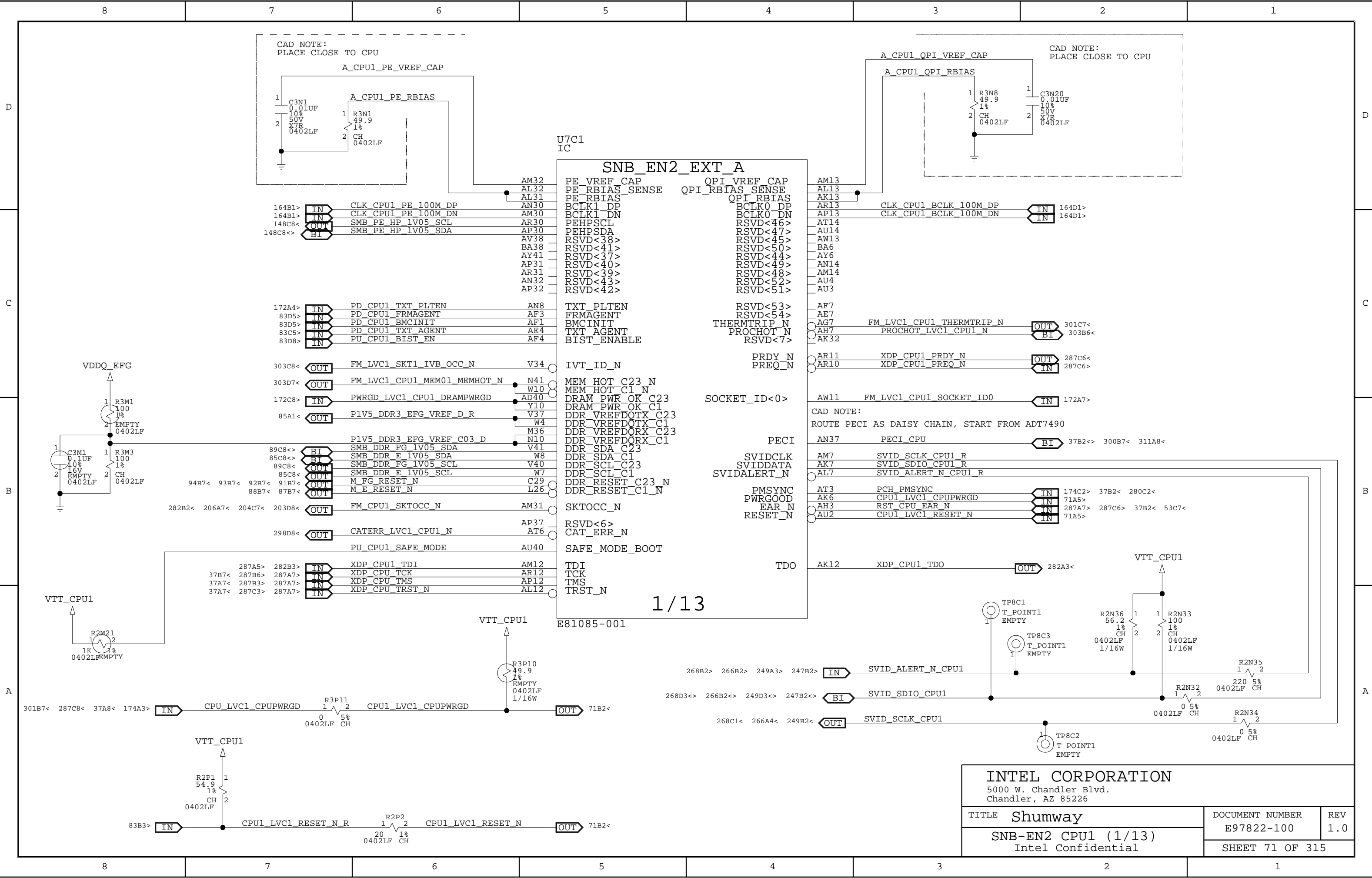
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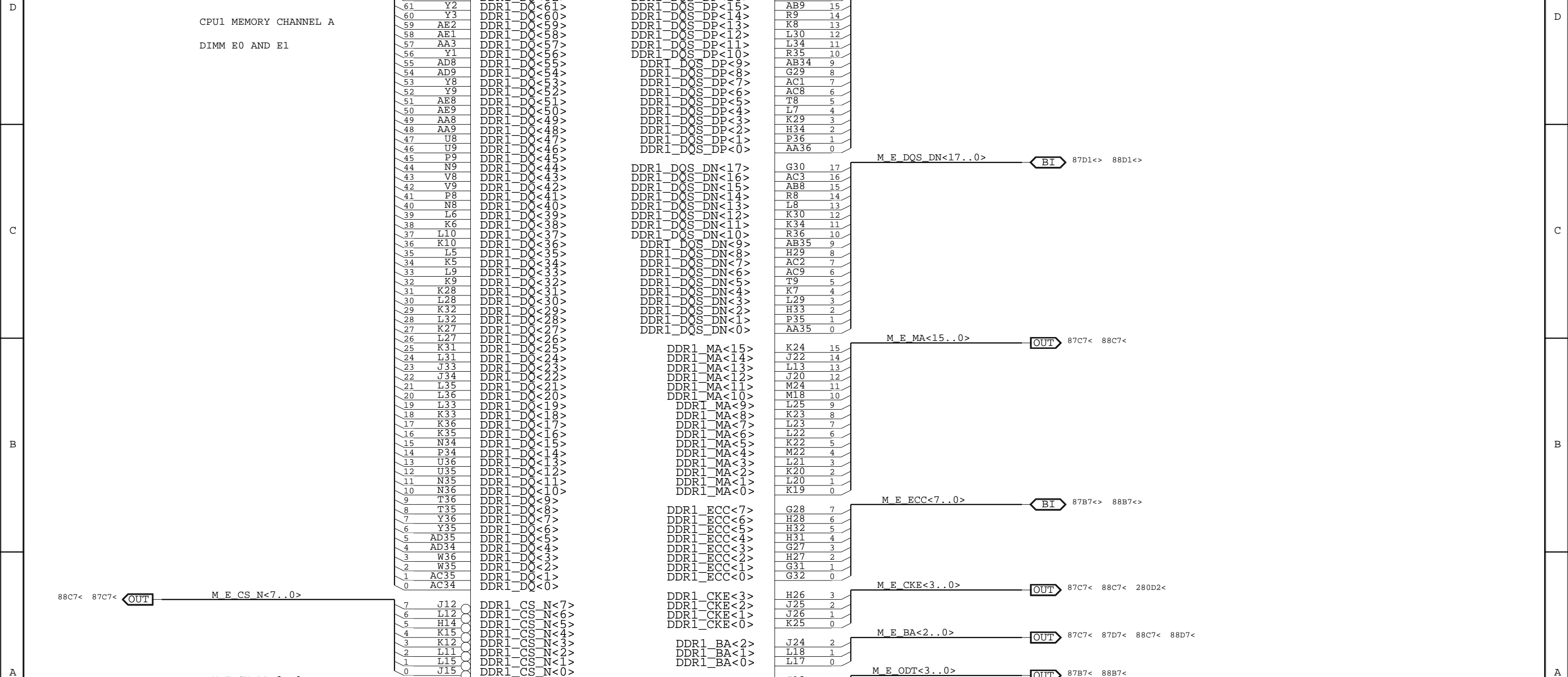
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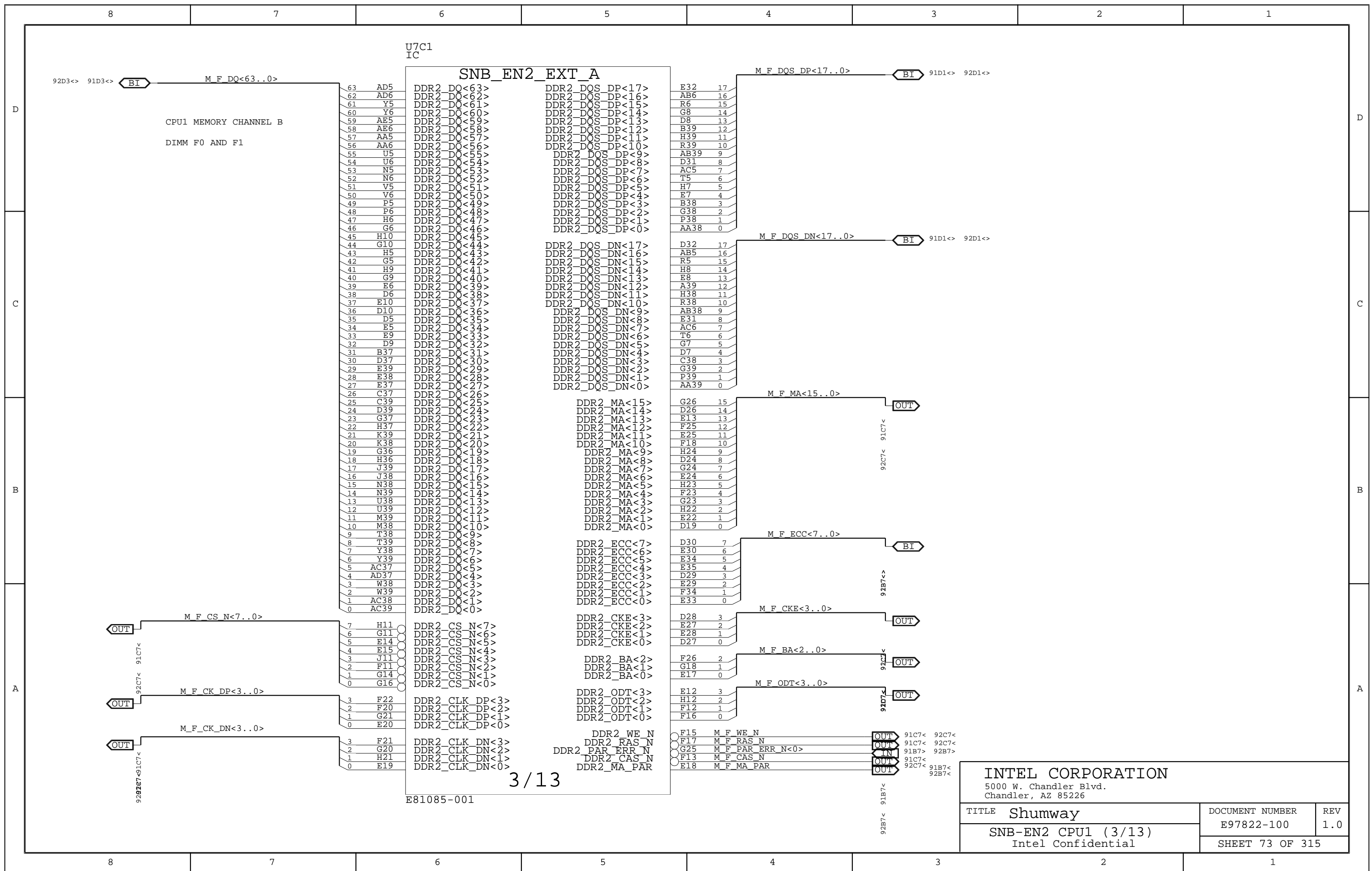
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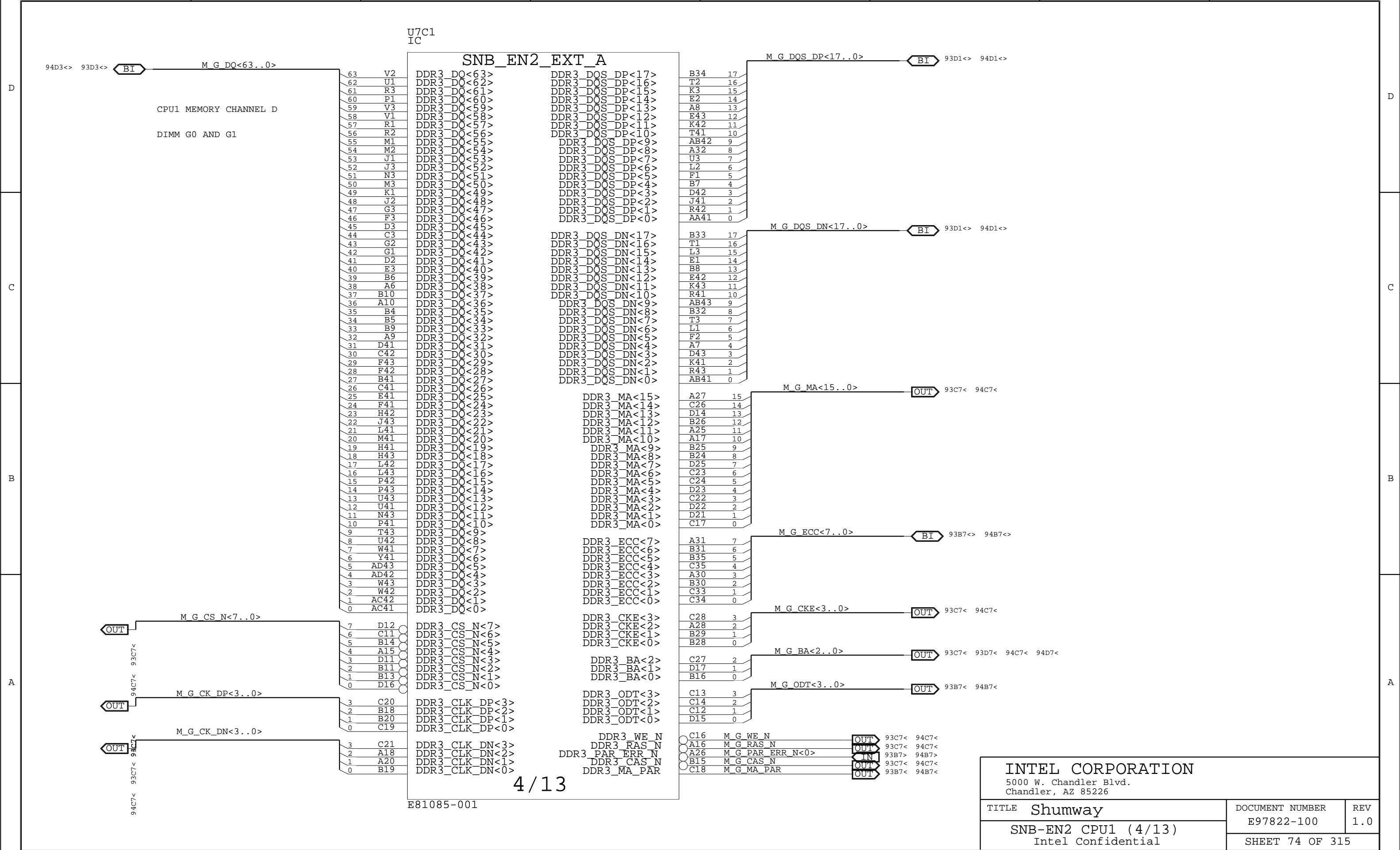
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SANDYBRIDGE SKT B2							
CPU 1							
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SEC - SNB-EN2 CPU1 Intel Confidential						SHEET 70 OF 315	
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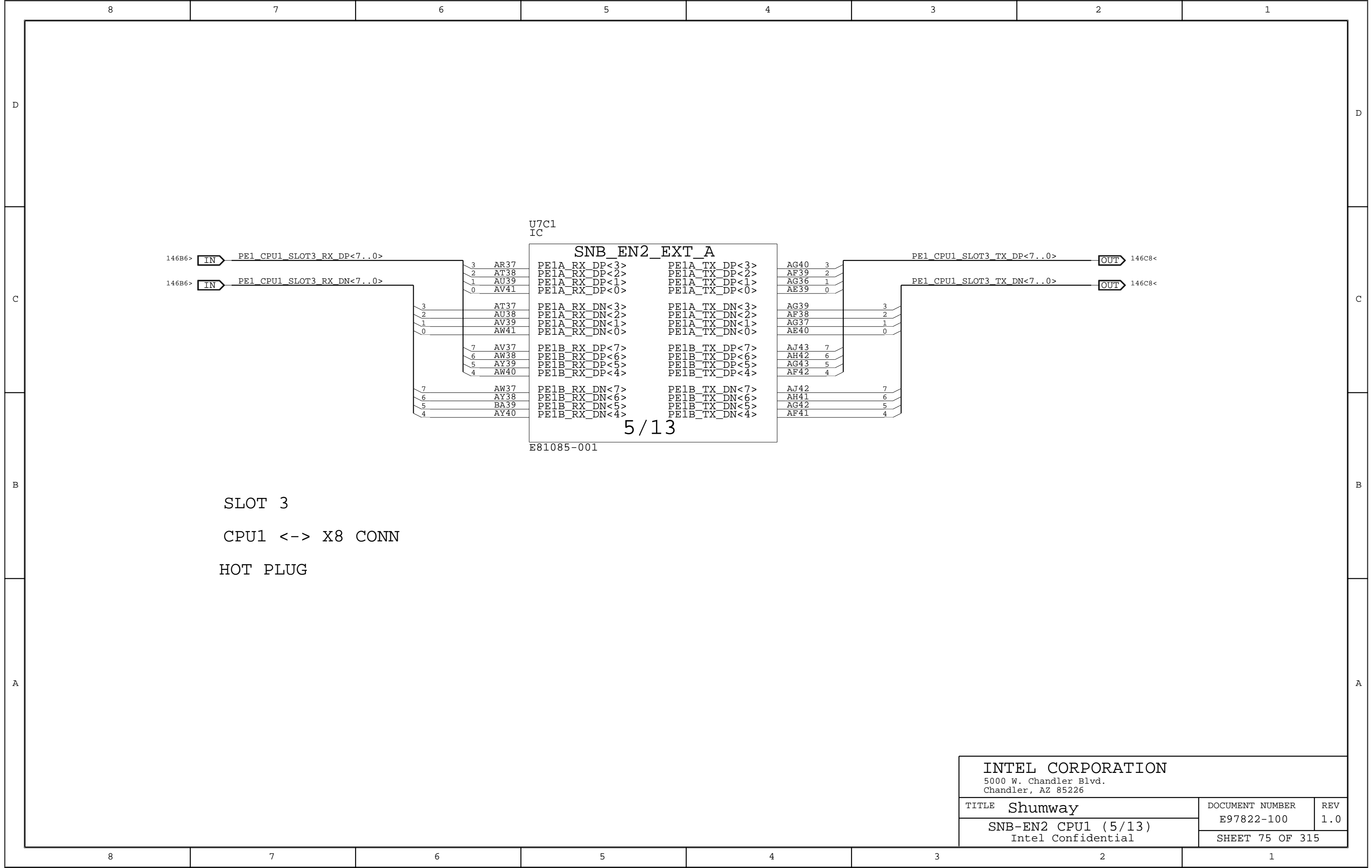


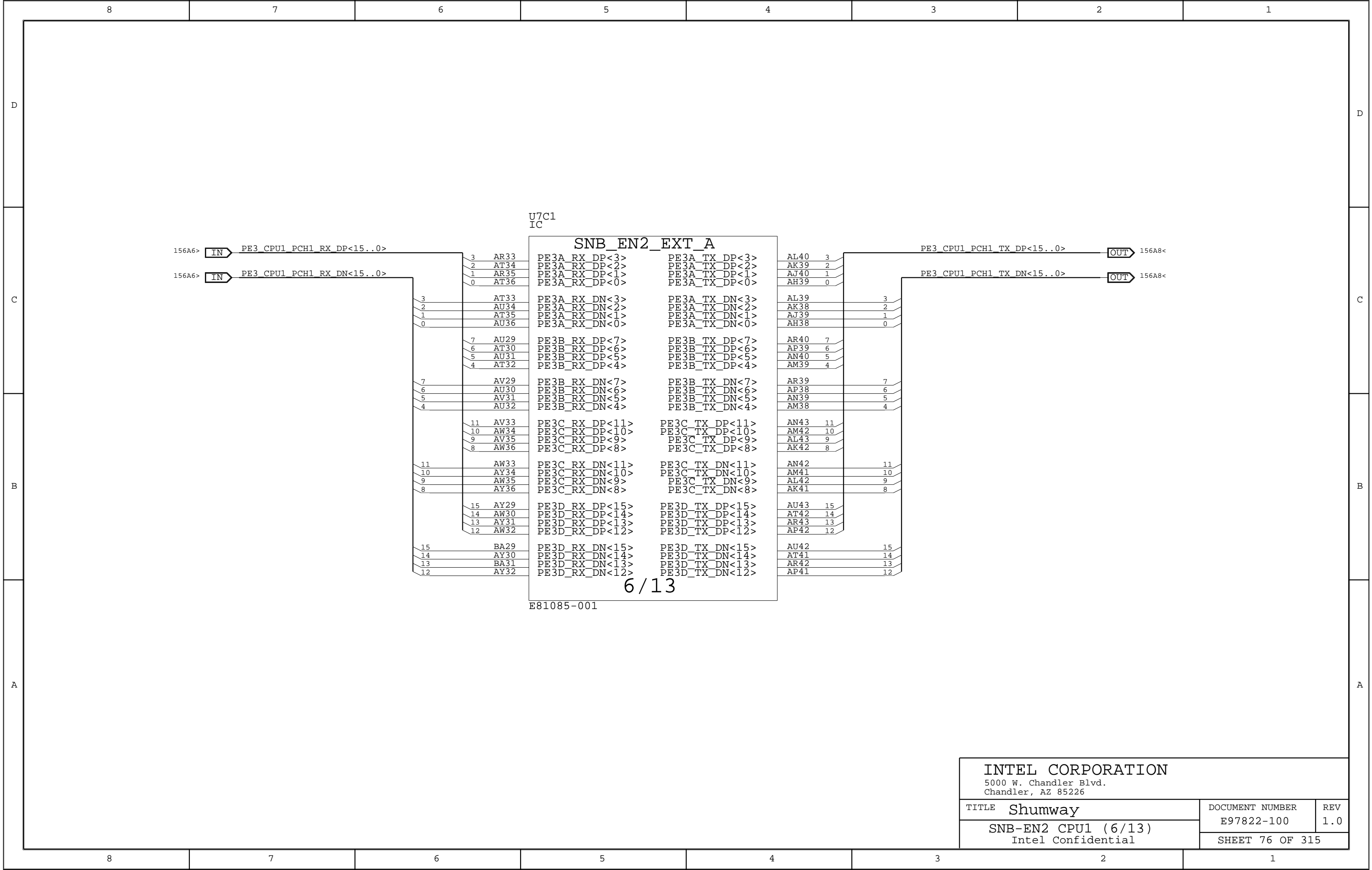


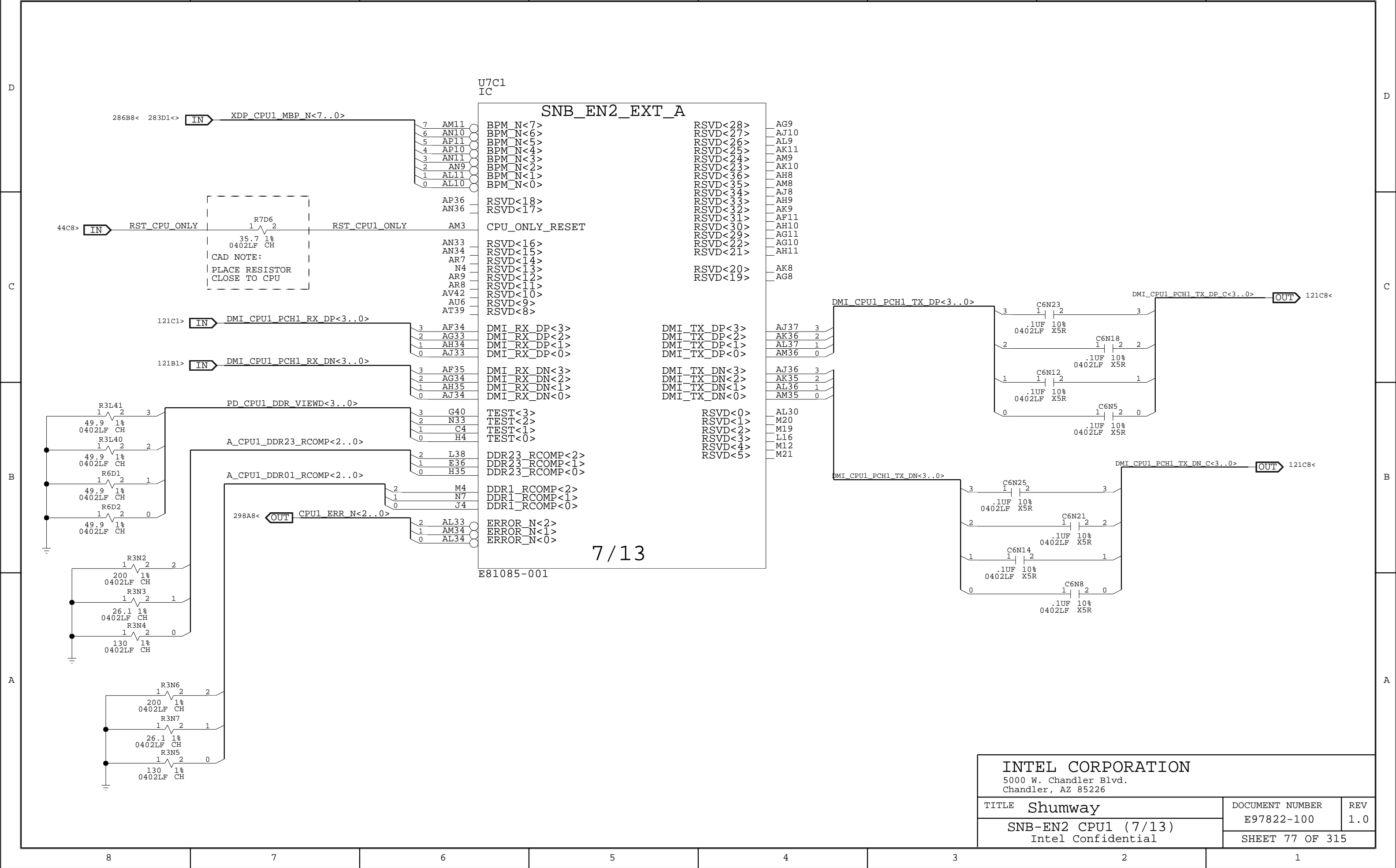


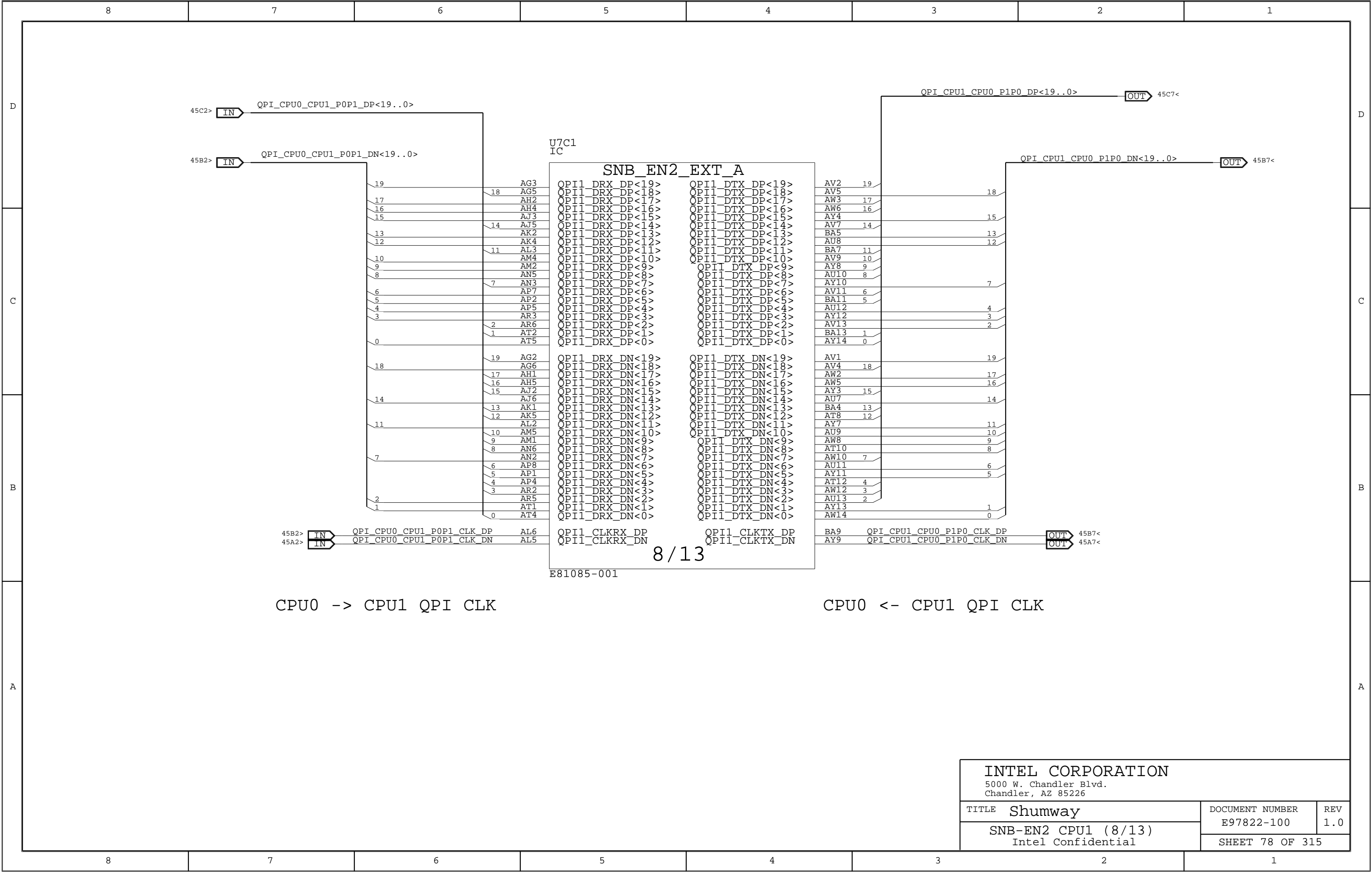




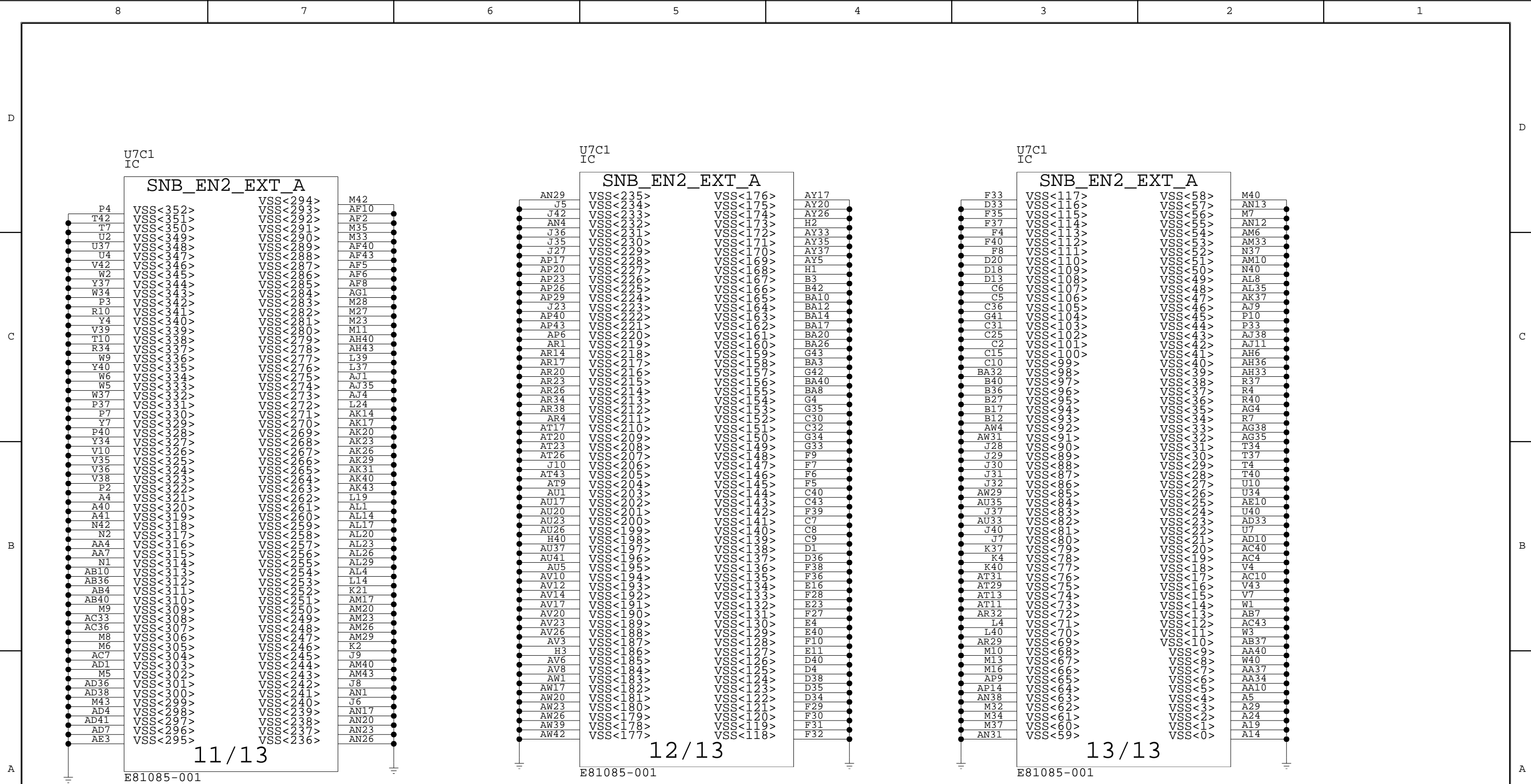




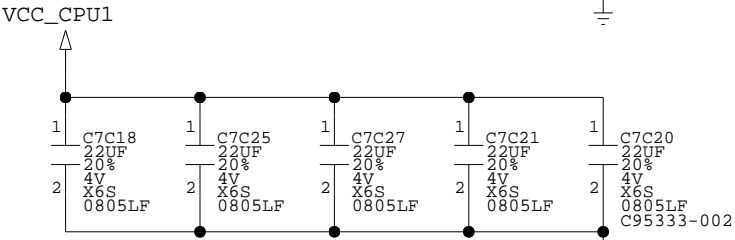
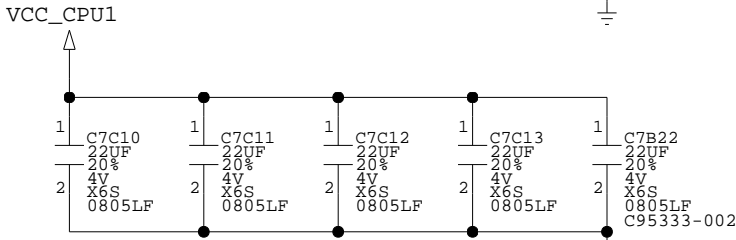
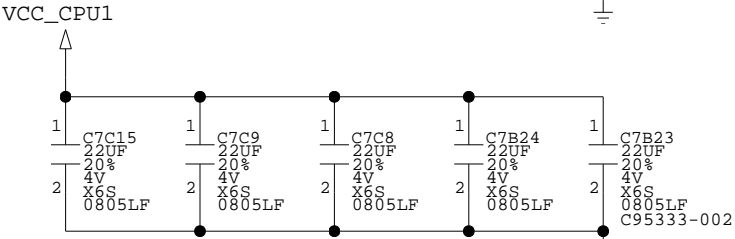
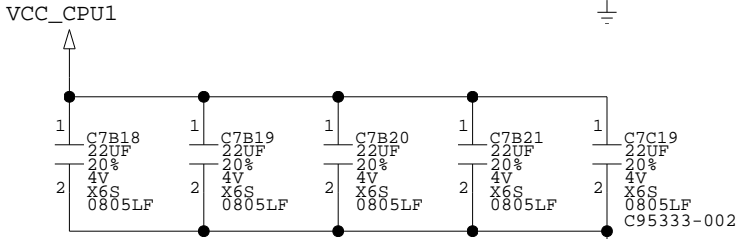
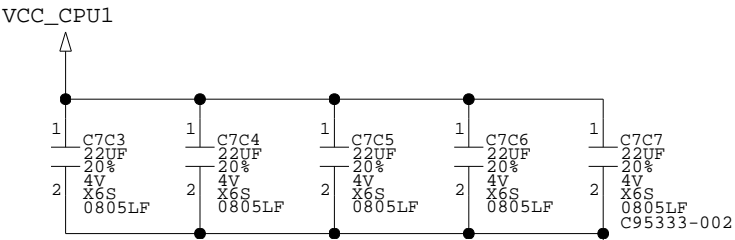
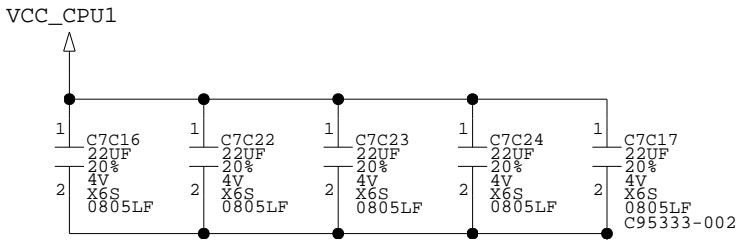




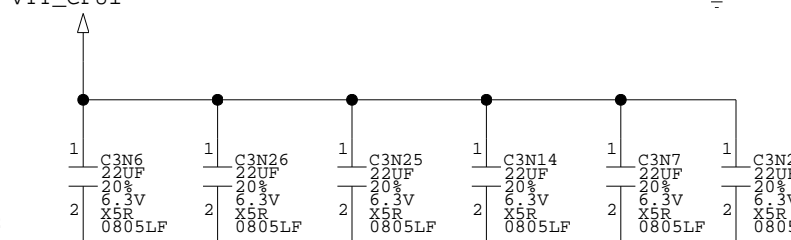
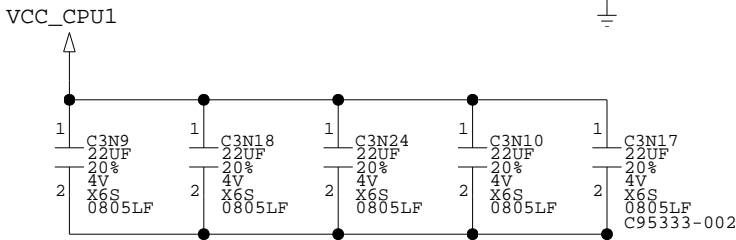
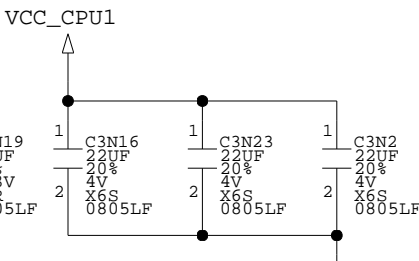
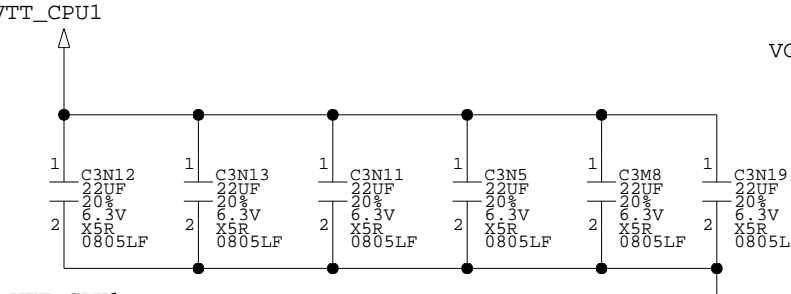
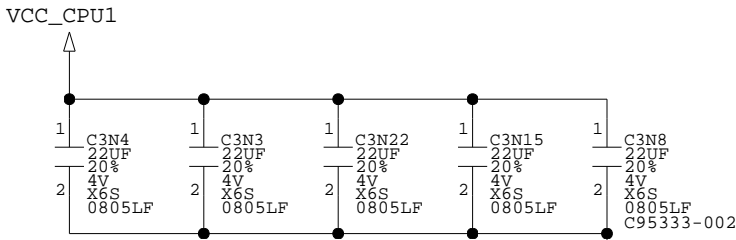
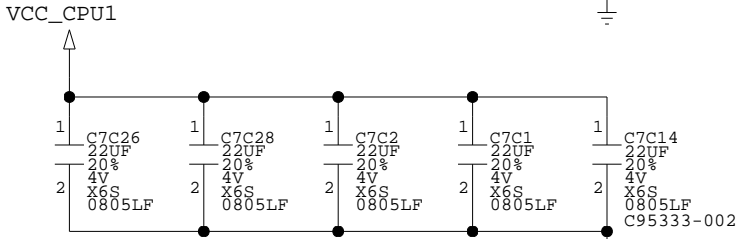




SANDYBRIDGE SKT B2 DECOUPLING CAP



CAD NOTE:  
PLACE CAPS IN/OR OPPOSITE CAVITY



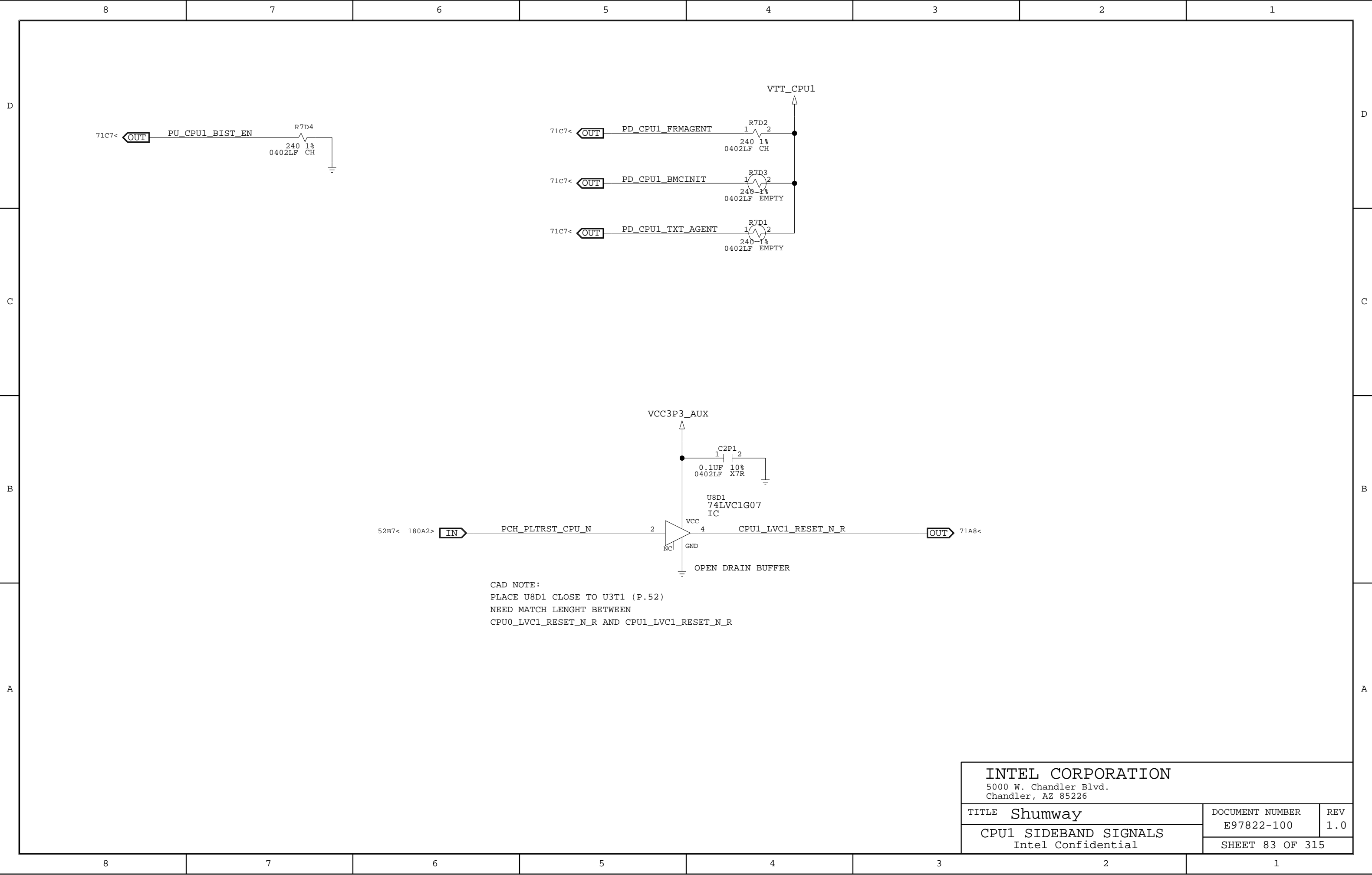
CAD NOTE:  
PLACE CAPS IN/OR OPPOSITE CAVITY

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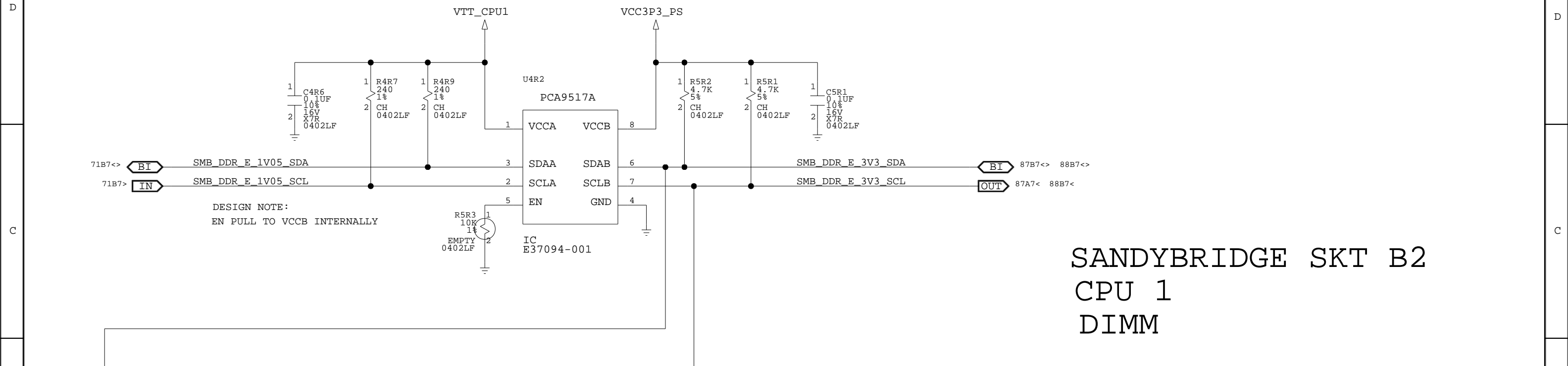
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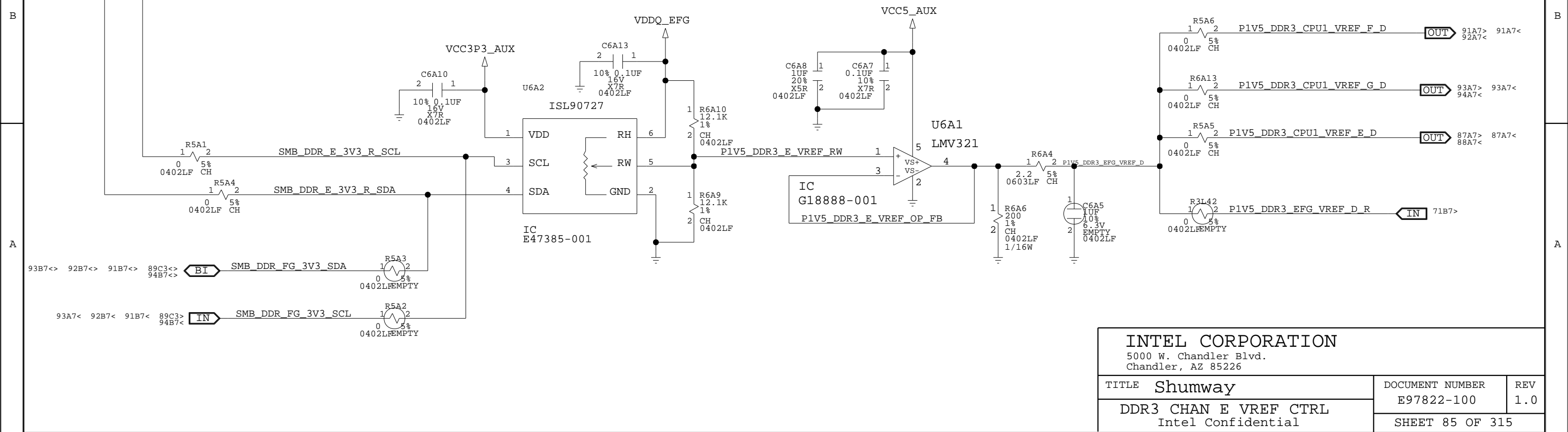
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SANDYBRIDGE SKT B2  
CPU 1  
DIMM



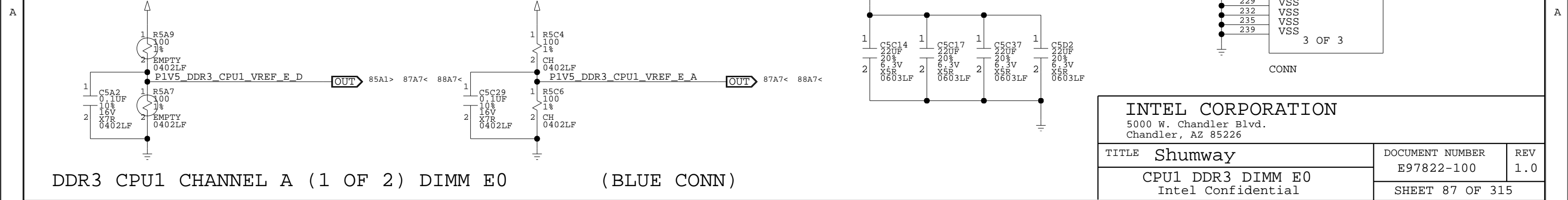
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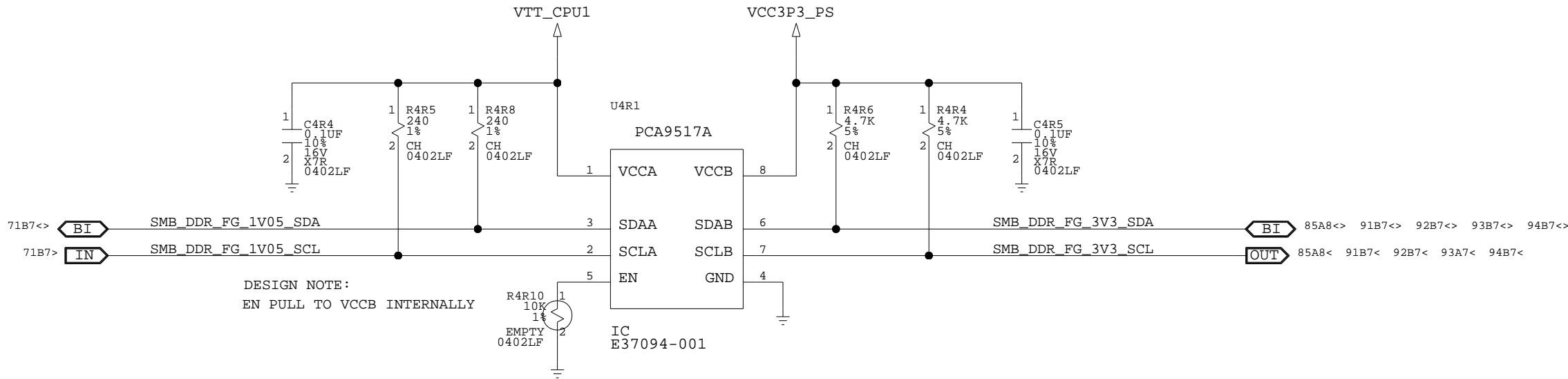
DDR3 CHAN E VREF CTRL  
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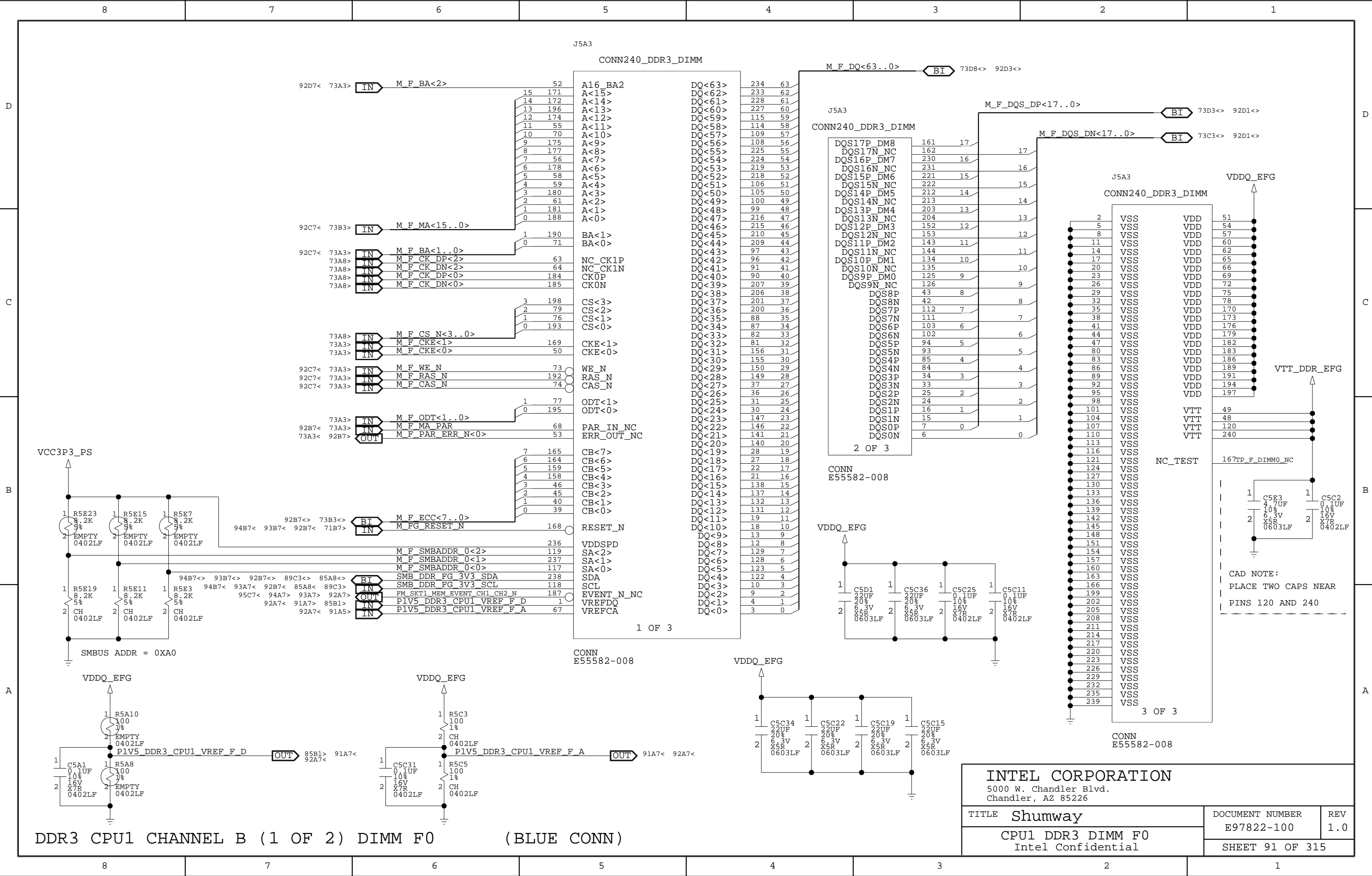


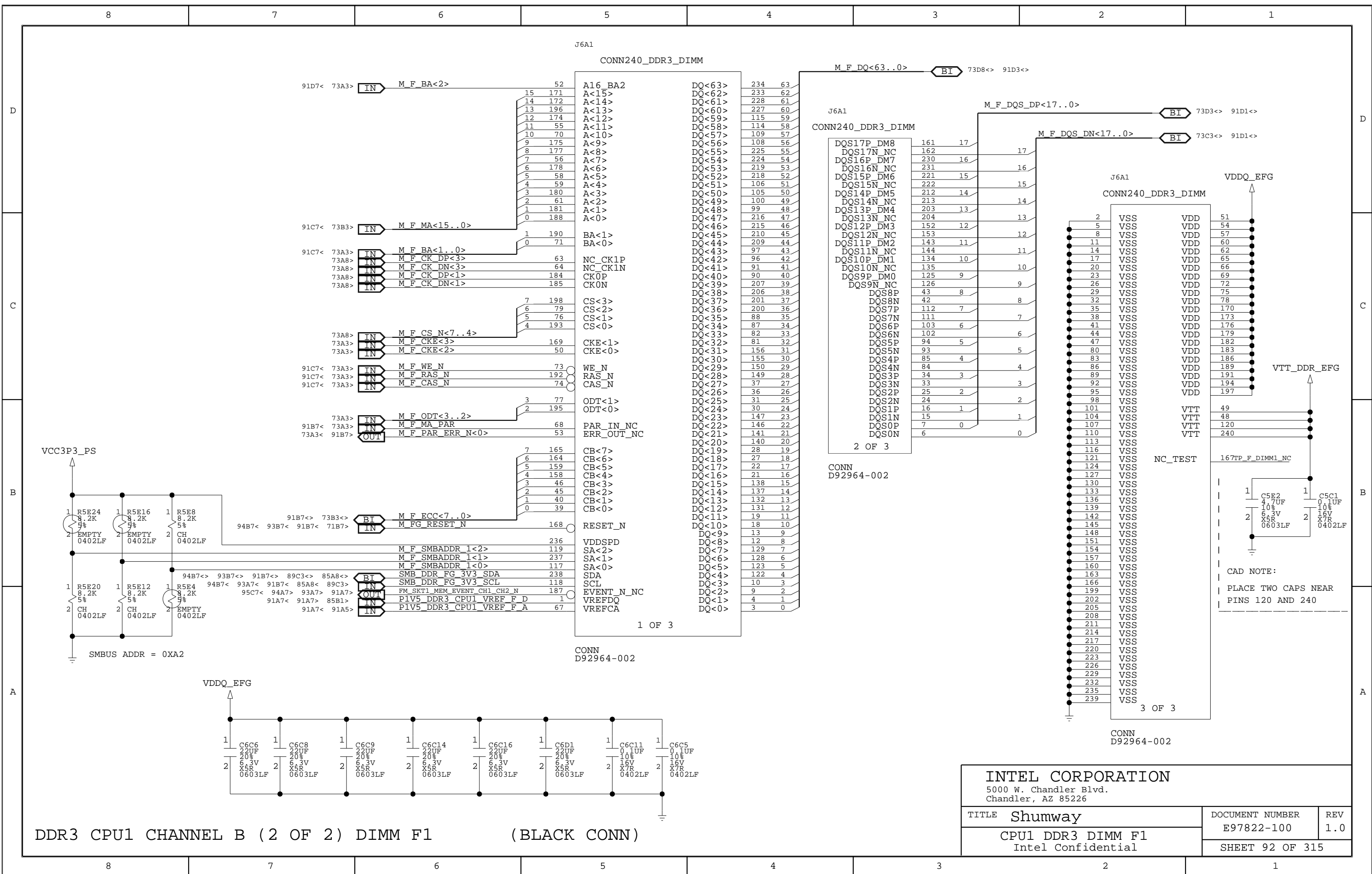


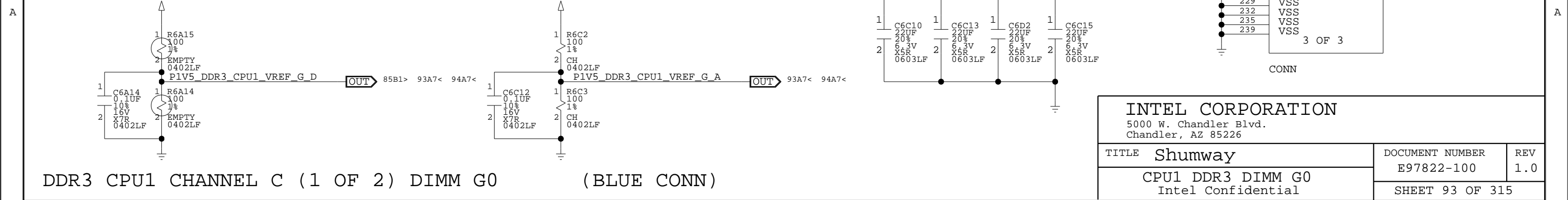
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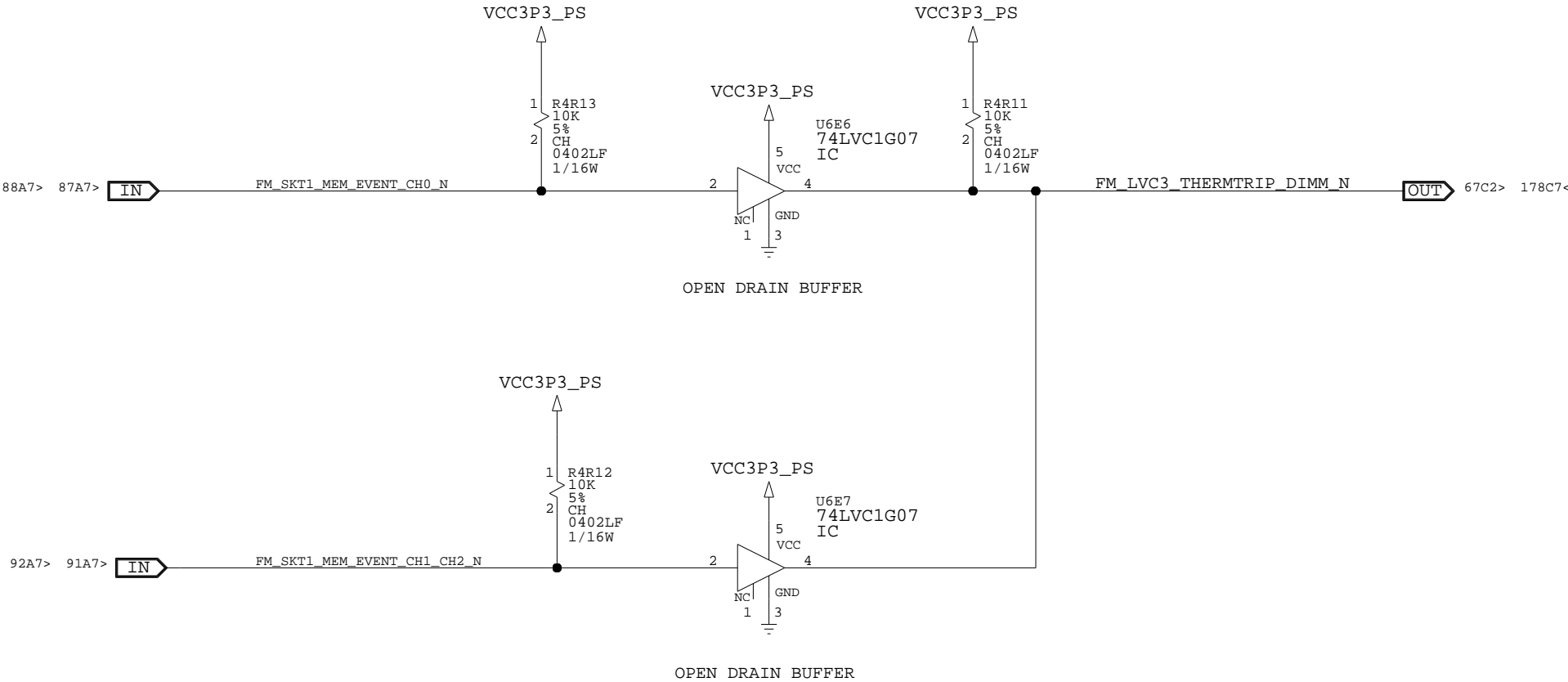
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DIMM: SKT1\_MEM\_EVENT  
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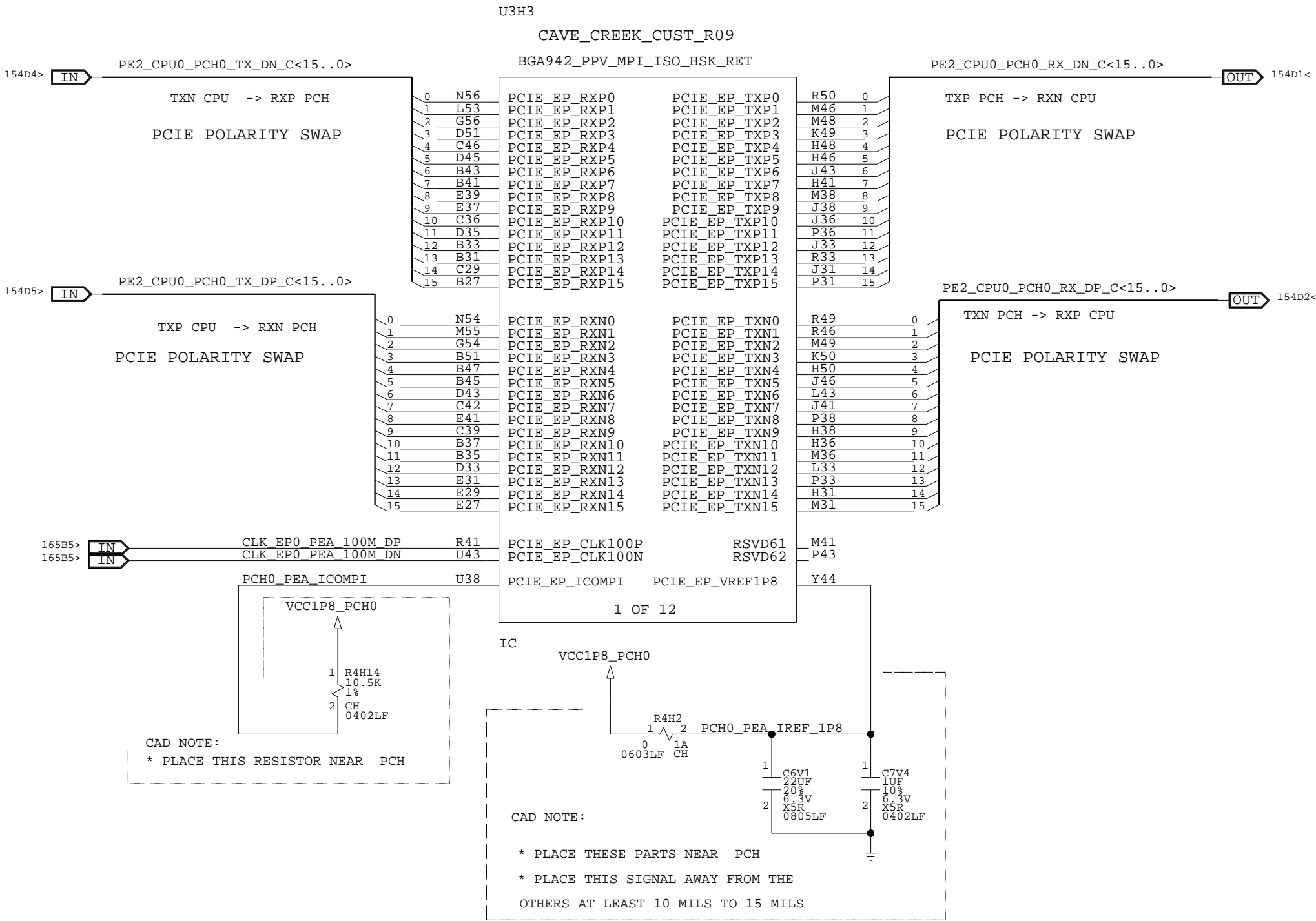
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CCK0 (PCIE X16)  
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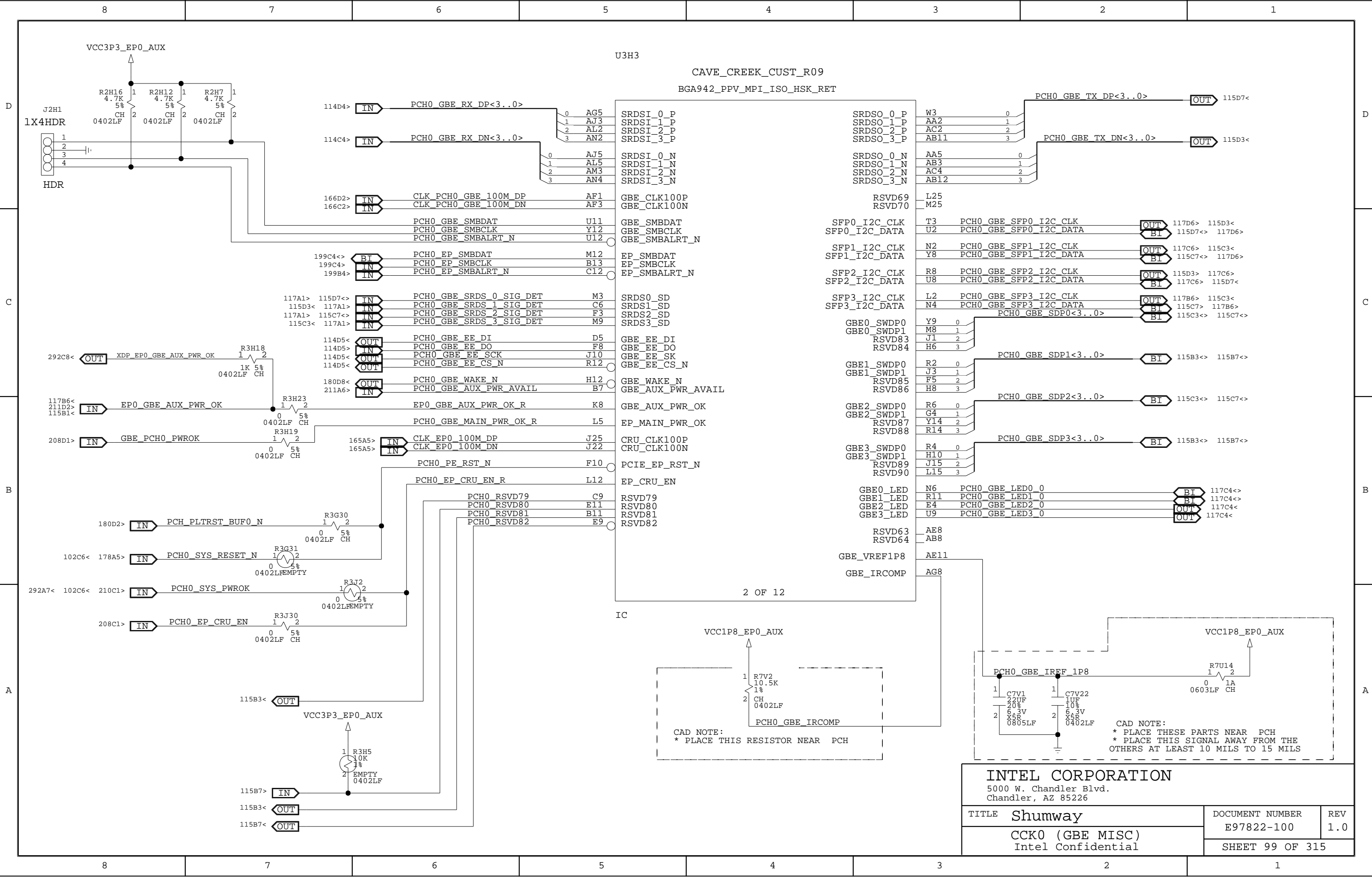
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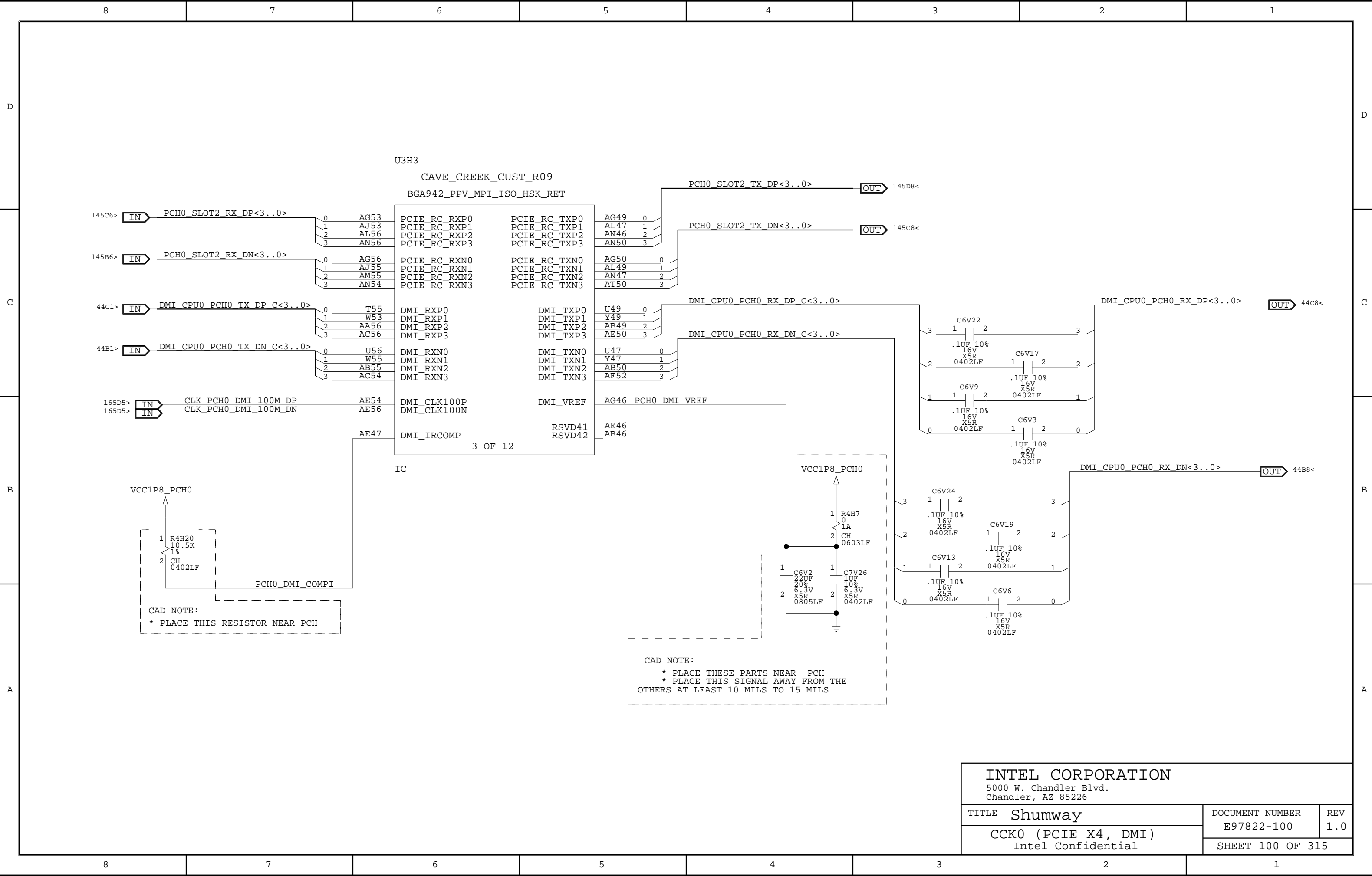
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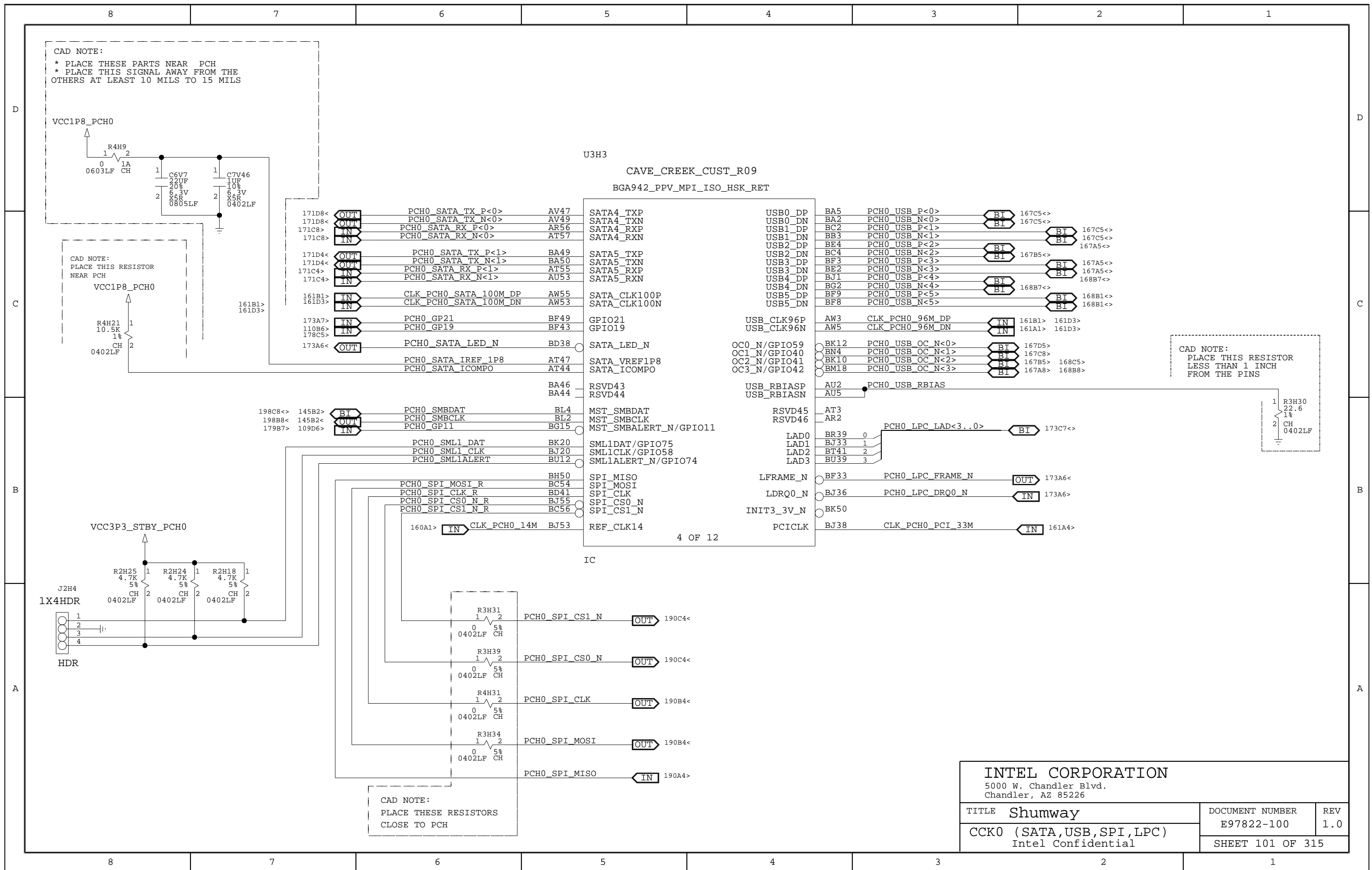
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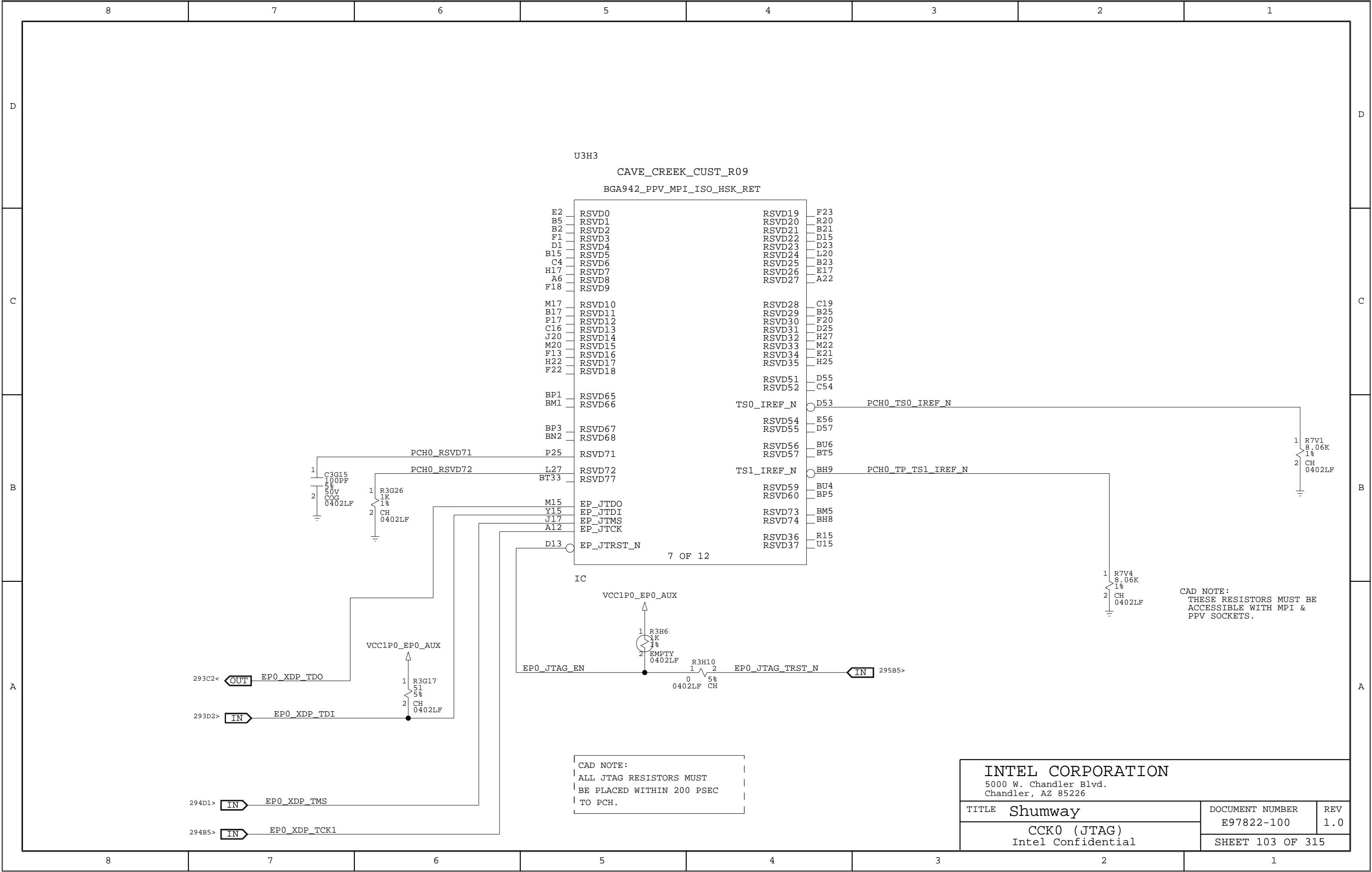


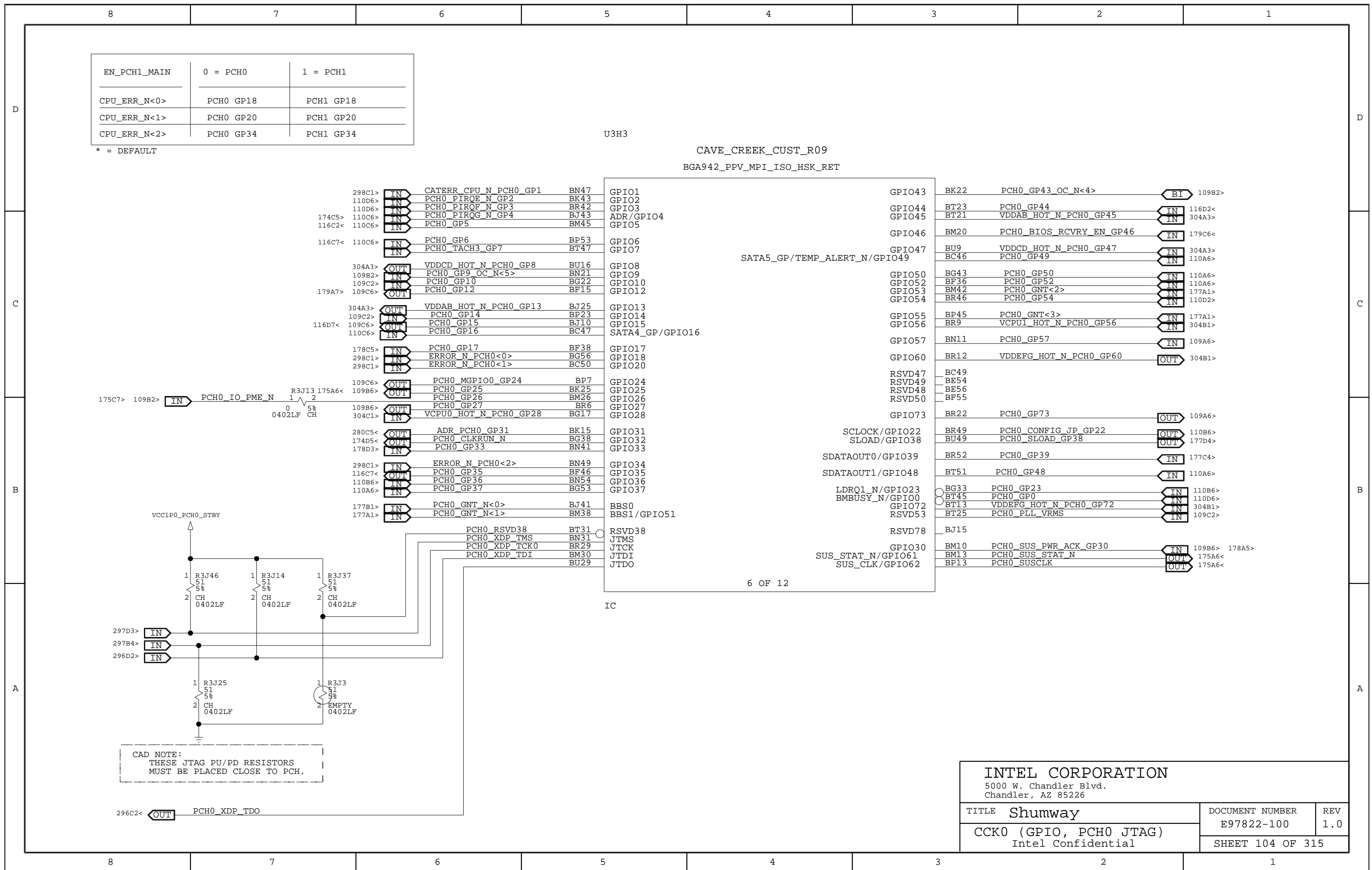








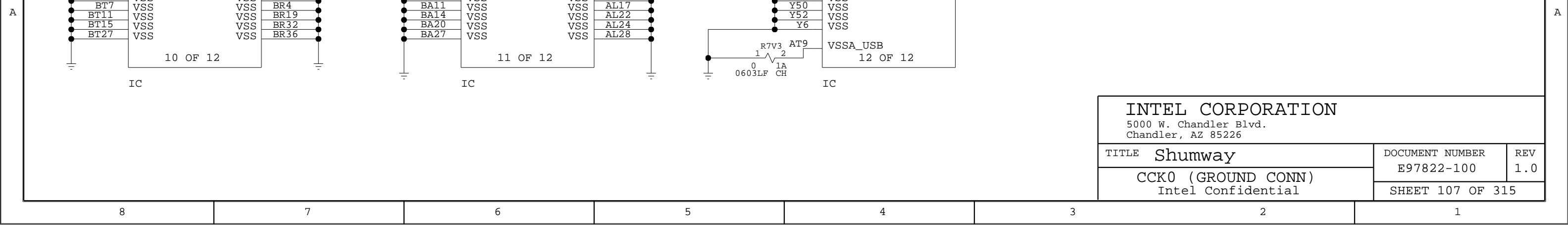












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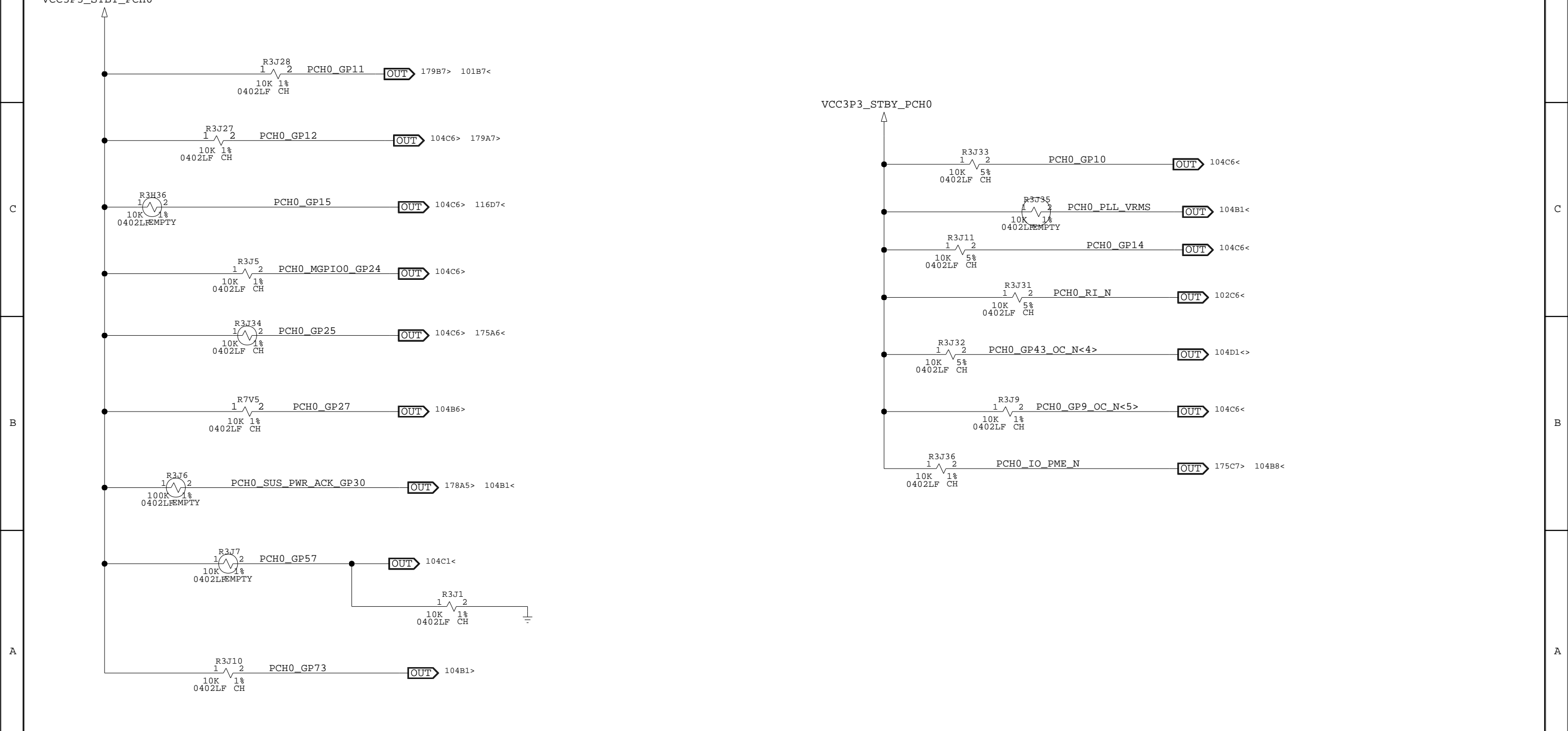
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PCH0 GPIO STBY TERM Intel Confidential		REV
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GPIO (MAIN VOLTAGE LEVEL) TERMINATION

VCC3P3\_PCH0

R3J17  
10K 1%  
0402LFEEMPTY

PCH0\_GP0

OUT

104B1<

R3J42  
10K 5%  
0402LF CH

PCH0\_PIRQE\_N\_GP2

OUT

104D6<

R3J15  
10K 5%  
0402LF CH

PCH0\_PIRQF\_N\_GP3

OUT

104C6<

R3J41  
10K 1%  
0402LFEEMPTY

PCH0\_PIRQG\_N\_GP4

OUT

174C5> 104C6<

R3J16  
10K 5%  
0402LF CH

PCH0\_GP5

OUT

104C6< 116C2<

R3J22  
10K 5%  
0402LF CH

PCH0\_GP6

OUT

104C6< 116C7<

R3J19  
10K 5%  
0402LF CH

PCH0\_GP7

OUT

R4H38  
10K 5%  
0402LF CH

PCH0\_GP16

OUT

104C6<

R3J44  
10K 5%  
0402LF CH

PCH0\_GP19

OUT

178C5> 101C7<

R3J20  
10K 5%  
0402LF CH

PCH0\_CONFIG\_JP\_GP22

OUT

104B1>

R3J39  
10K 5%  
0402LF CH

PCH0\_GP23

OUT

104B1<

R3J23  
10K 5%  
0402LF CH

PCH0\_GP36

OUT

104B6<

R4H43  
10K 5%  
0402LFEEMPTY

PCH0\_GP37

OUT

104B6<

R3J21  
10K 5%  
0402LF CH

PCH0\_GP48

OUT

104B1<

R4H34  
10K 5%  
0402LF CH

PCH0\_GP49

OUT

104C1<

R3J43  
10K 5%  
0402LF CH

PCH0\_GP50

OUT

104C1<

R3J40  
10K 1%  
0402LFEEMPTY

PCH0\_GP52

OUT

104C1<

VCC3P3\_PCH0

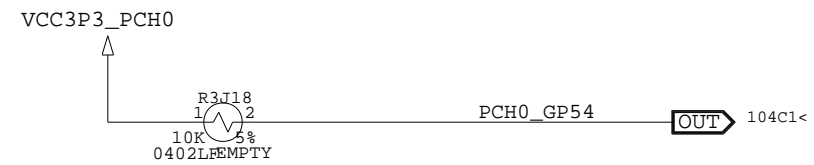
R3J18  
10K 5%  
0402LFEEMPTY

PCH0\_GP54

OUT

104C1<

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PHY CONN 0 &lt;-&gt; PCH0

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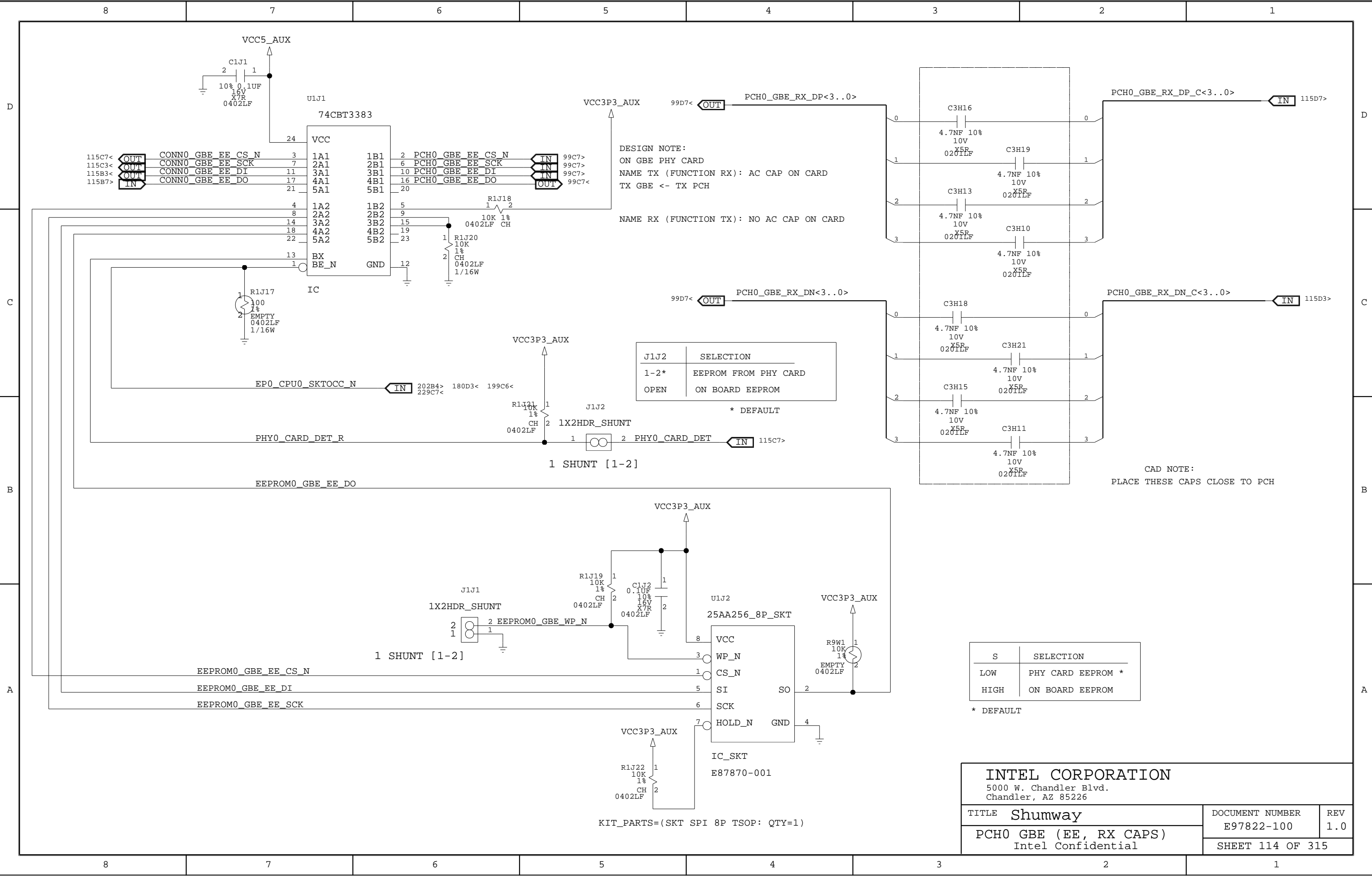
TITLE	Shumway
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SEC - PCH0 GBE PHY CONN  
Intel Confidential

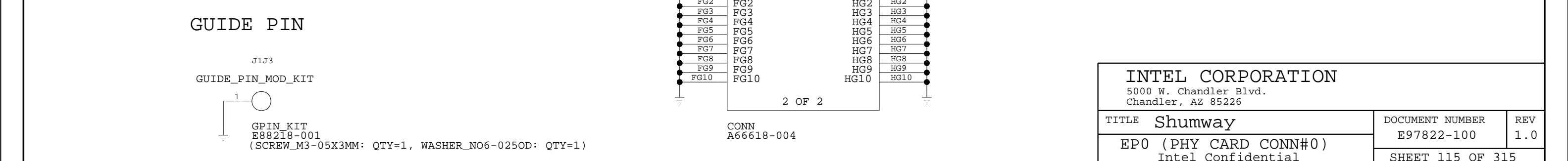
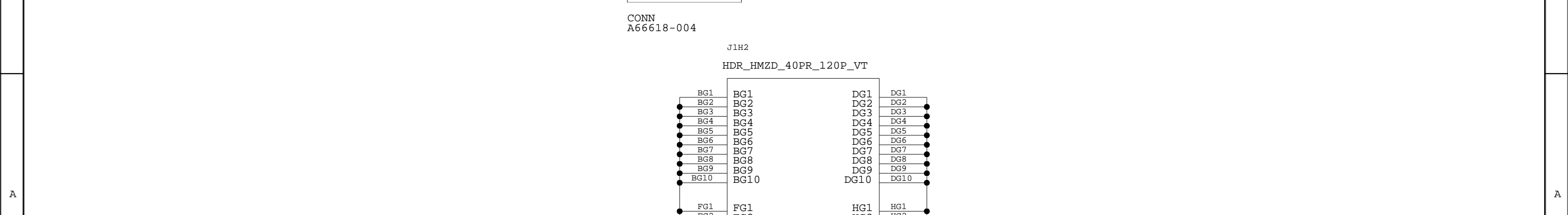
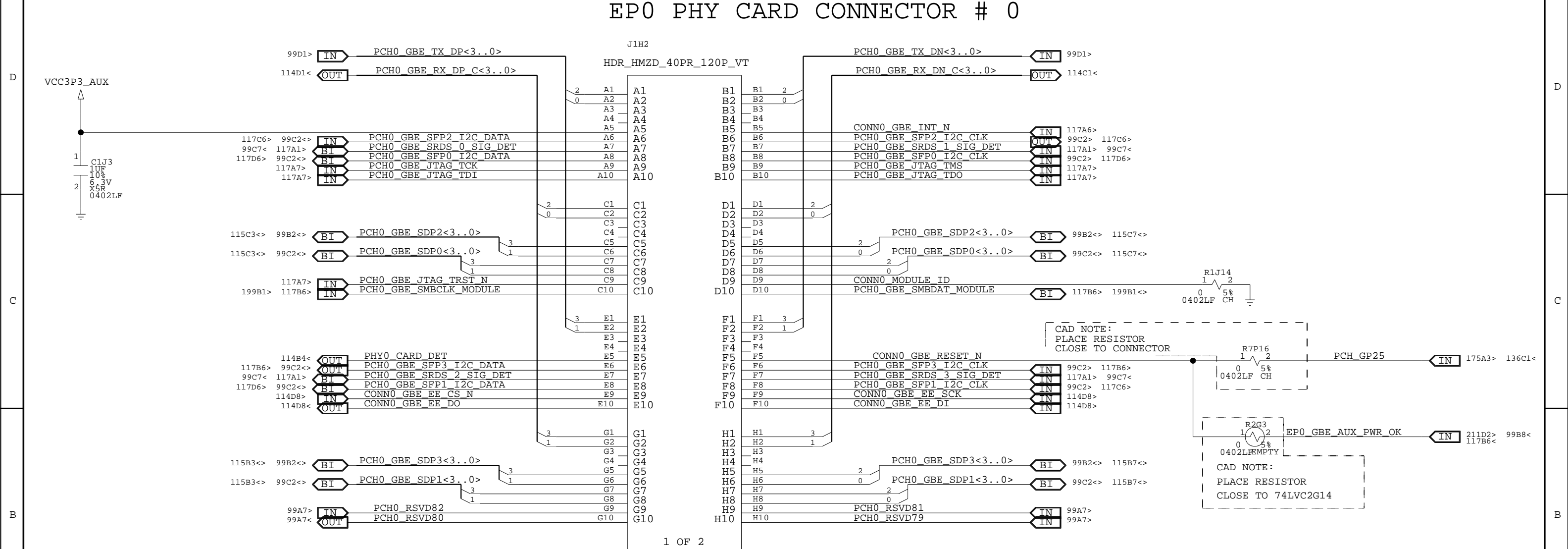
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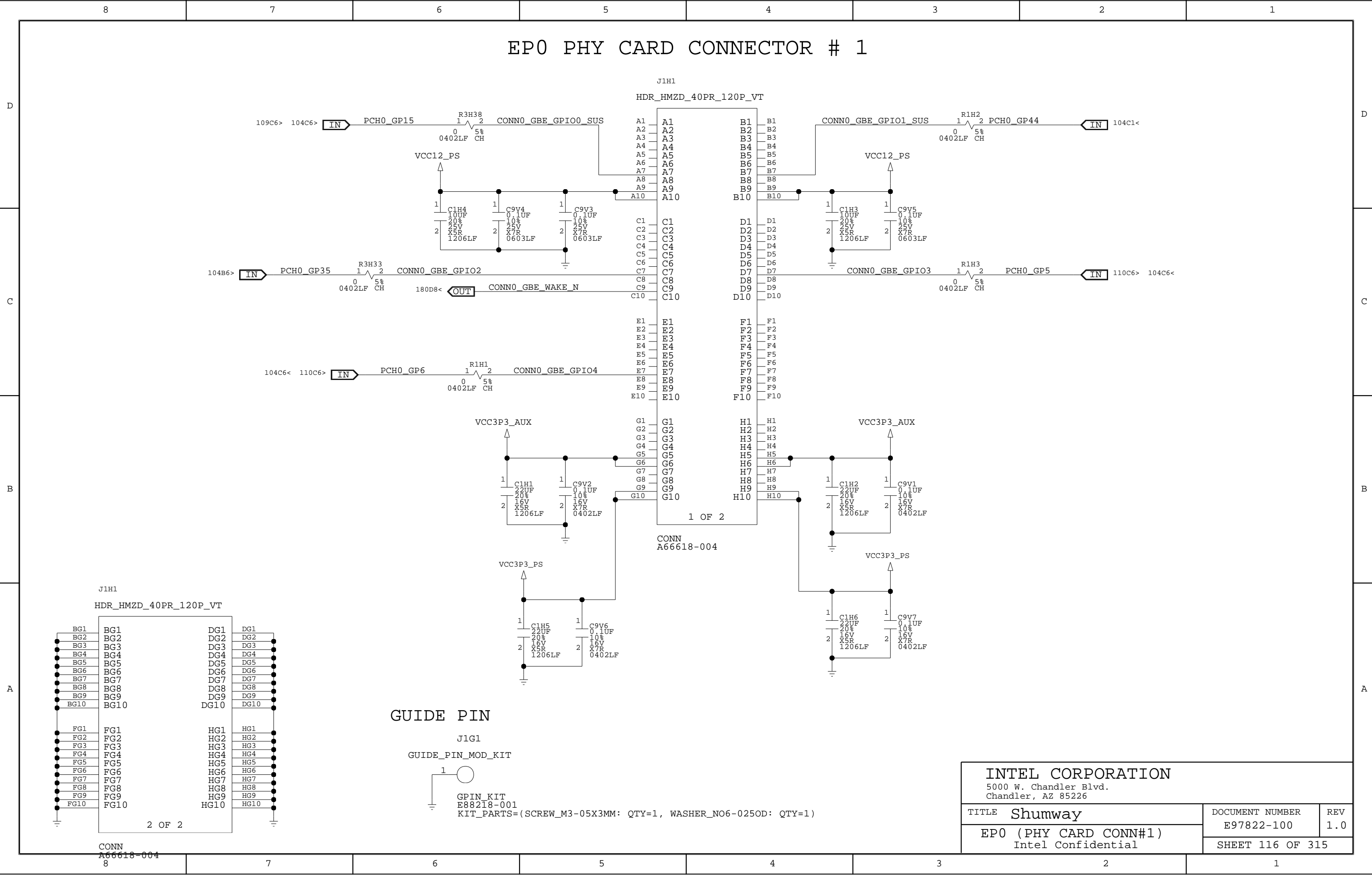
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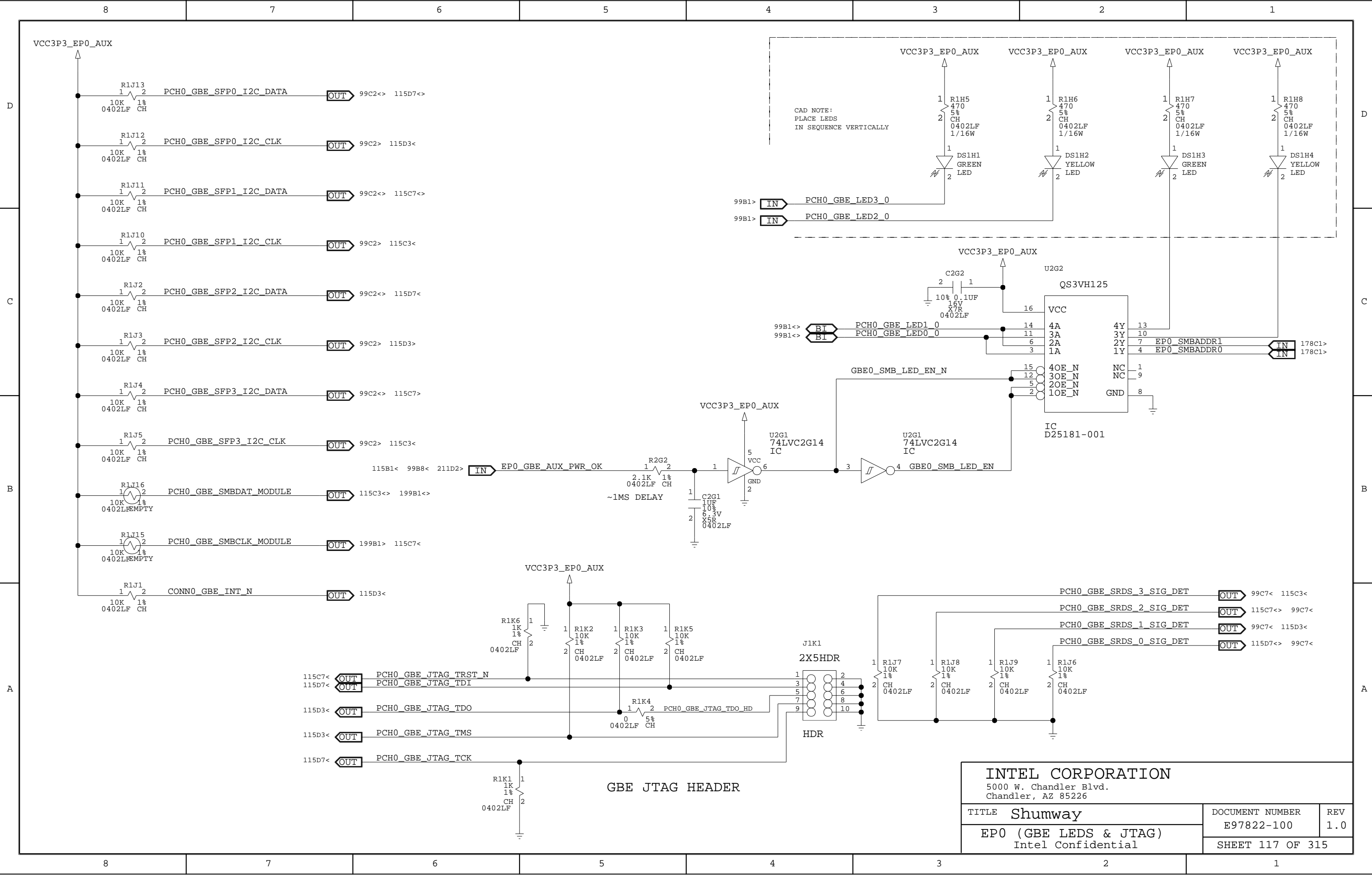
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EP0 (PHY CARD CONN#0) Intel Confidential	E97822-100	1.0
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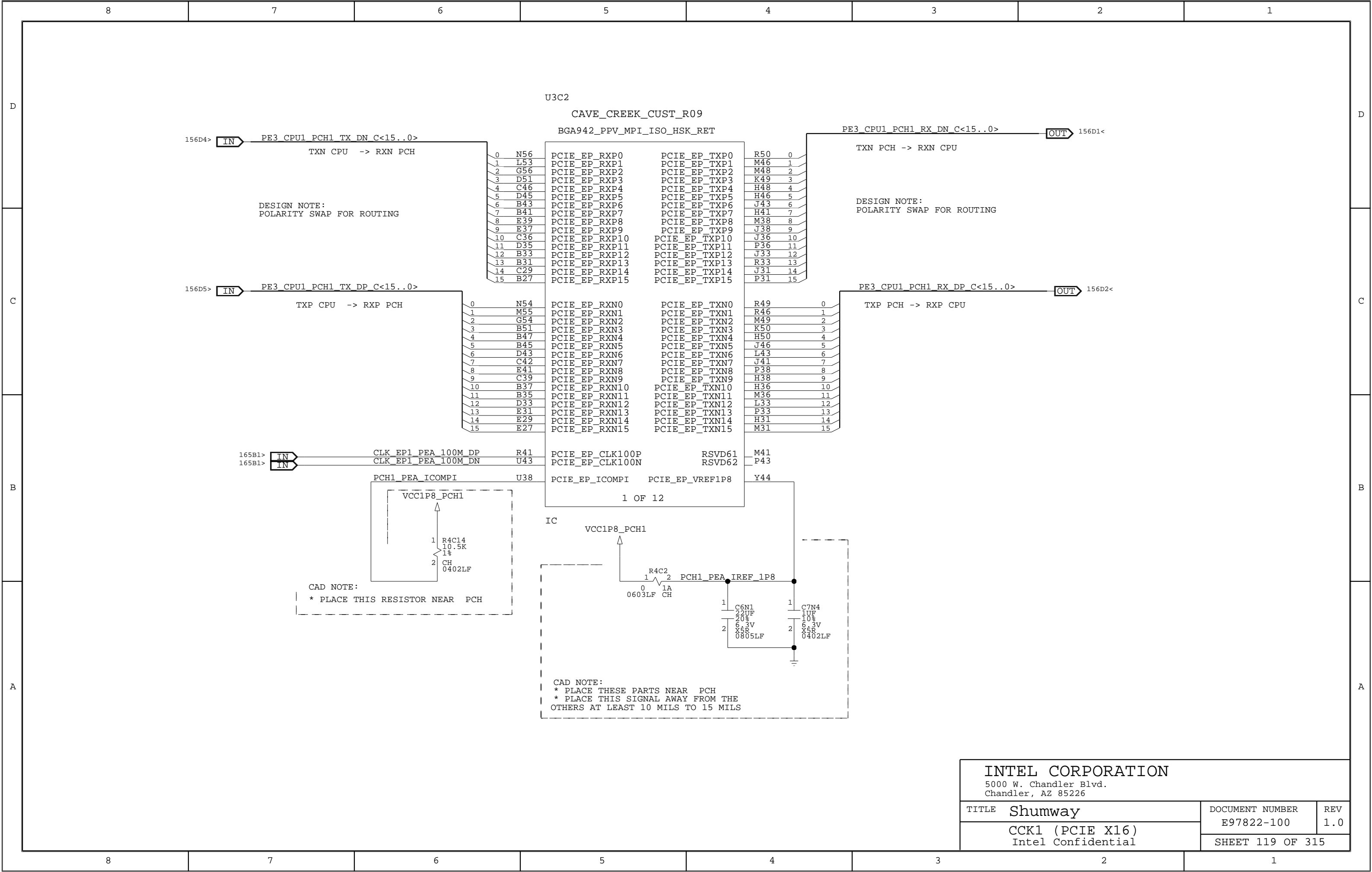
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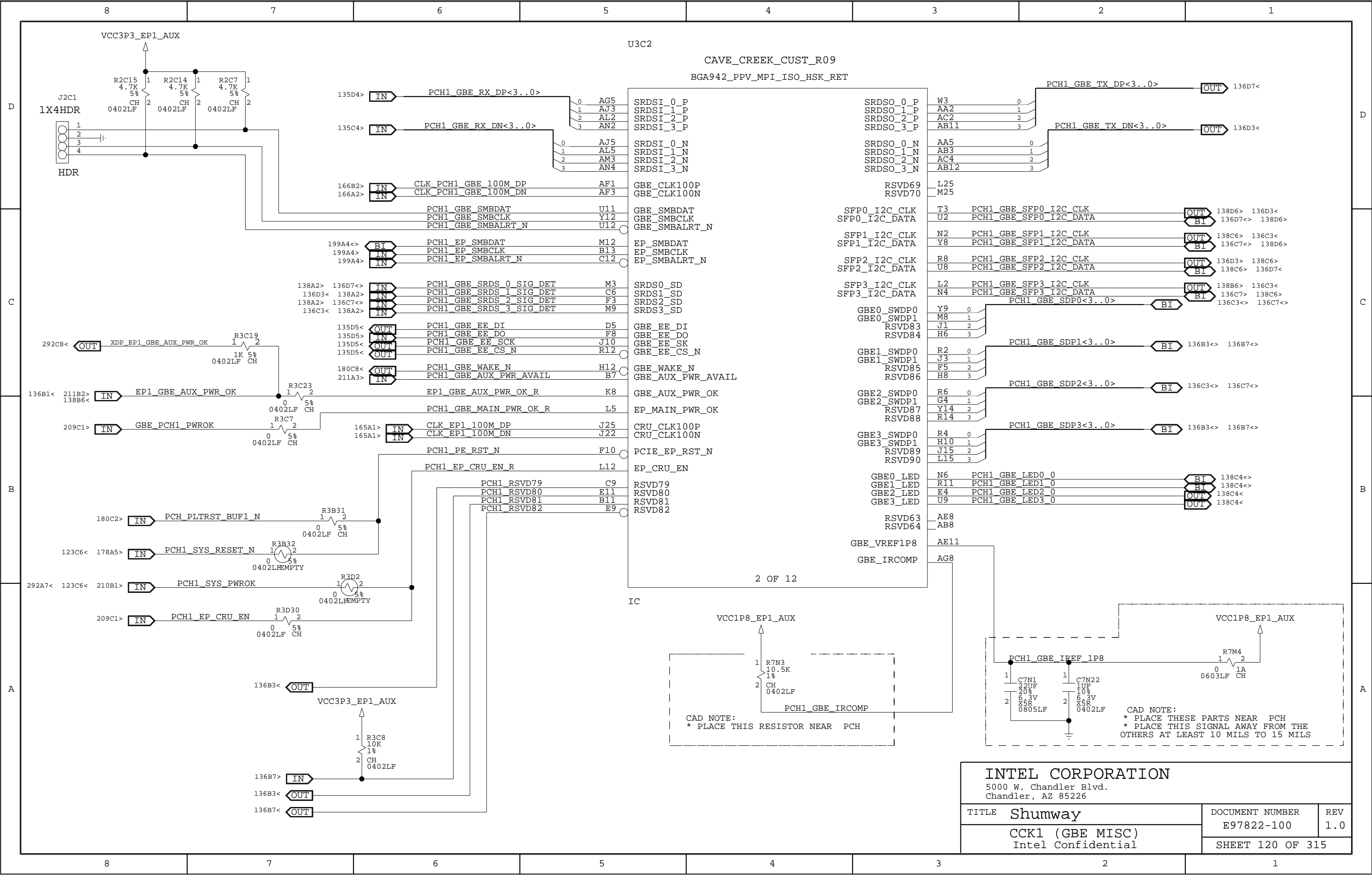
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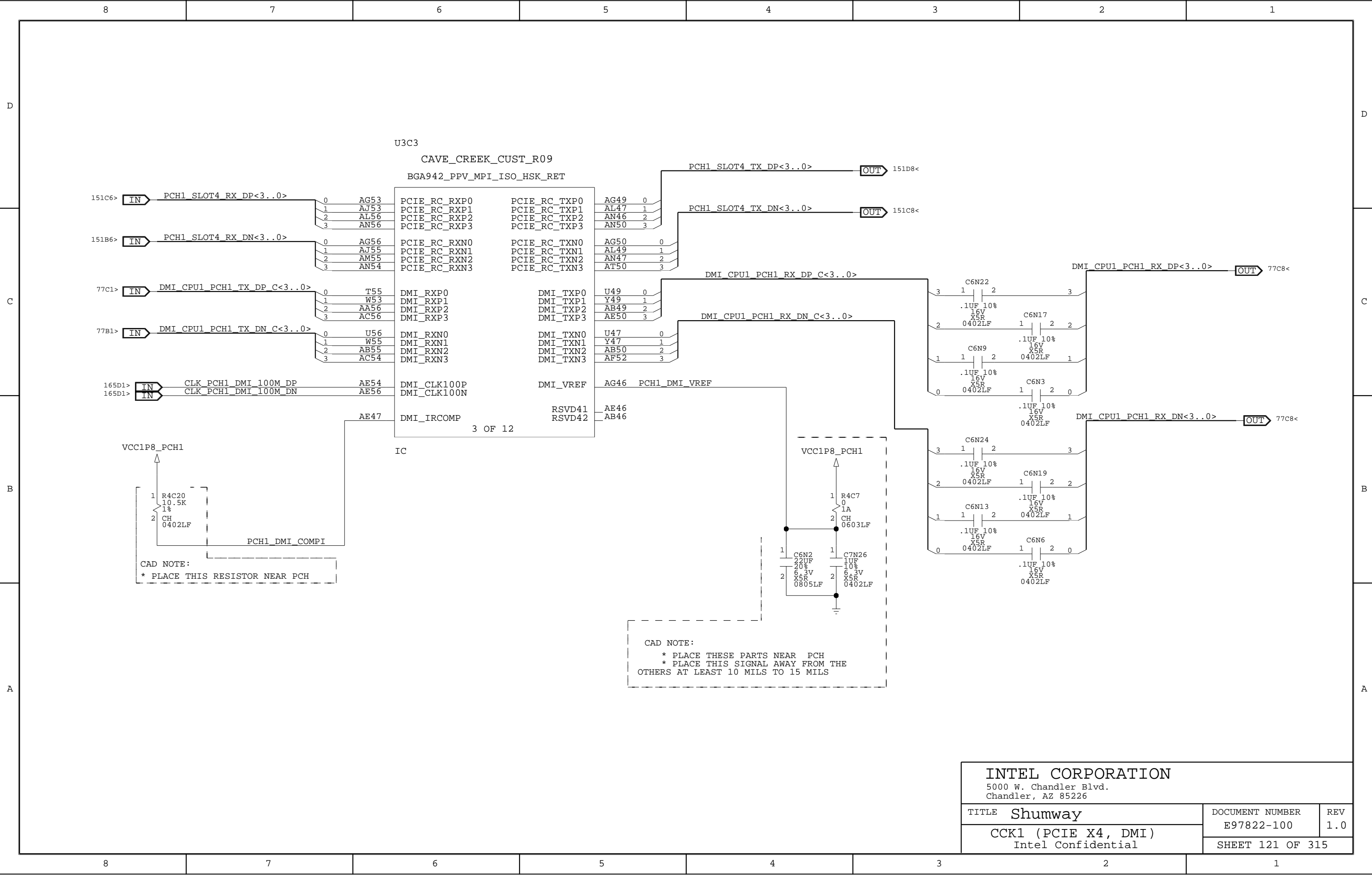
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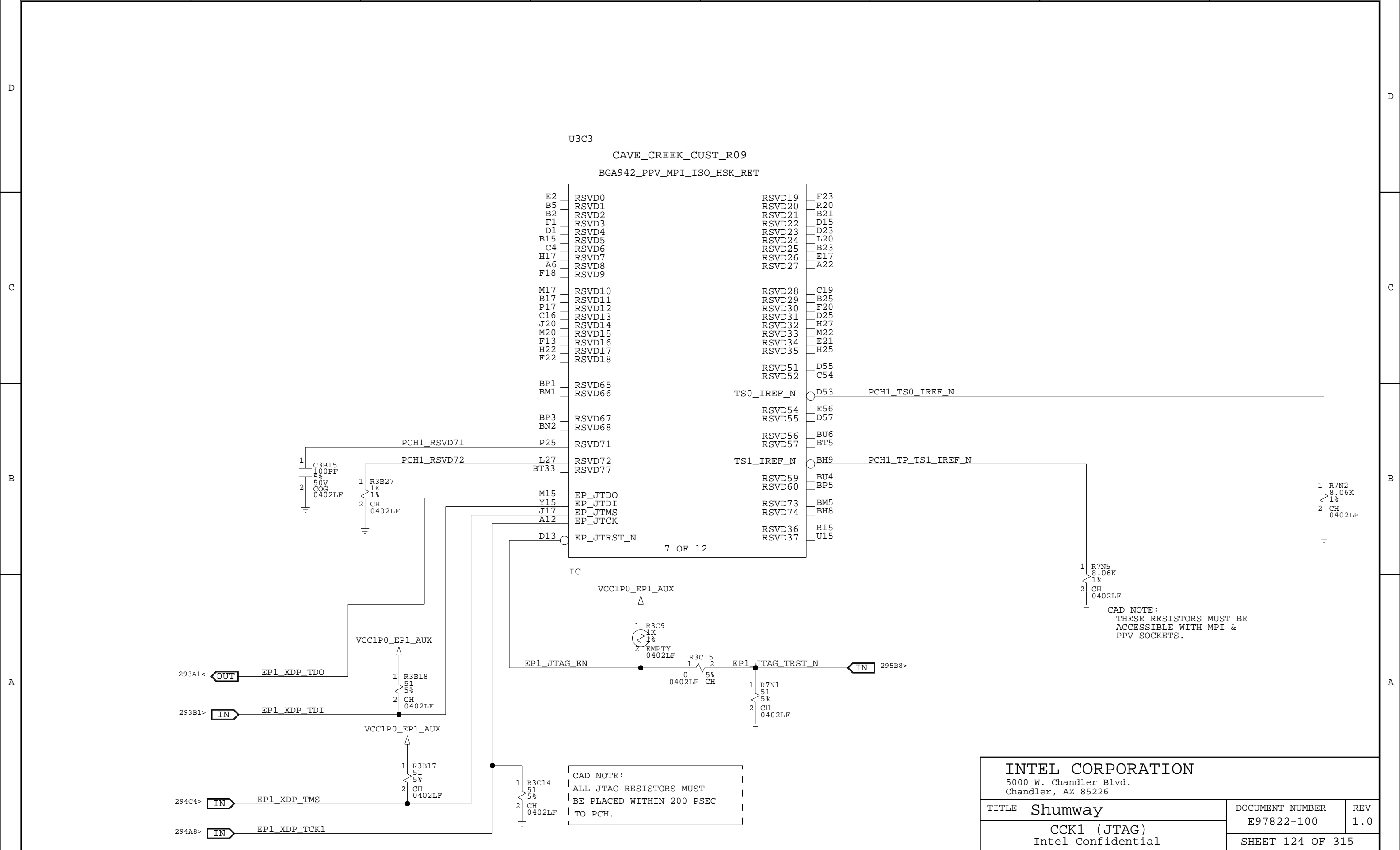


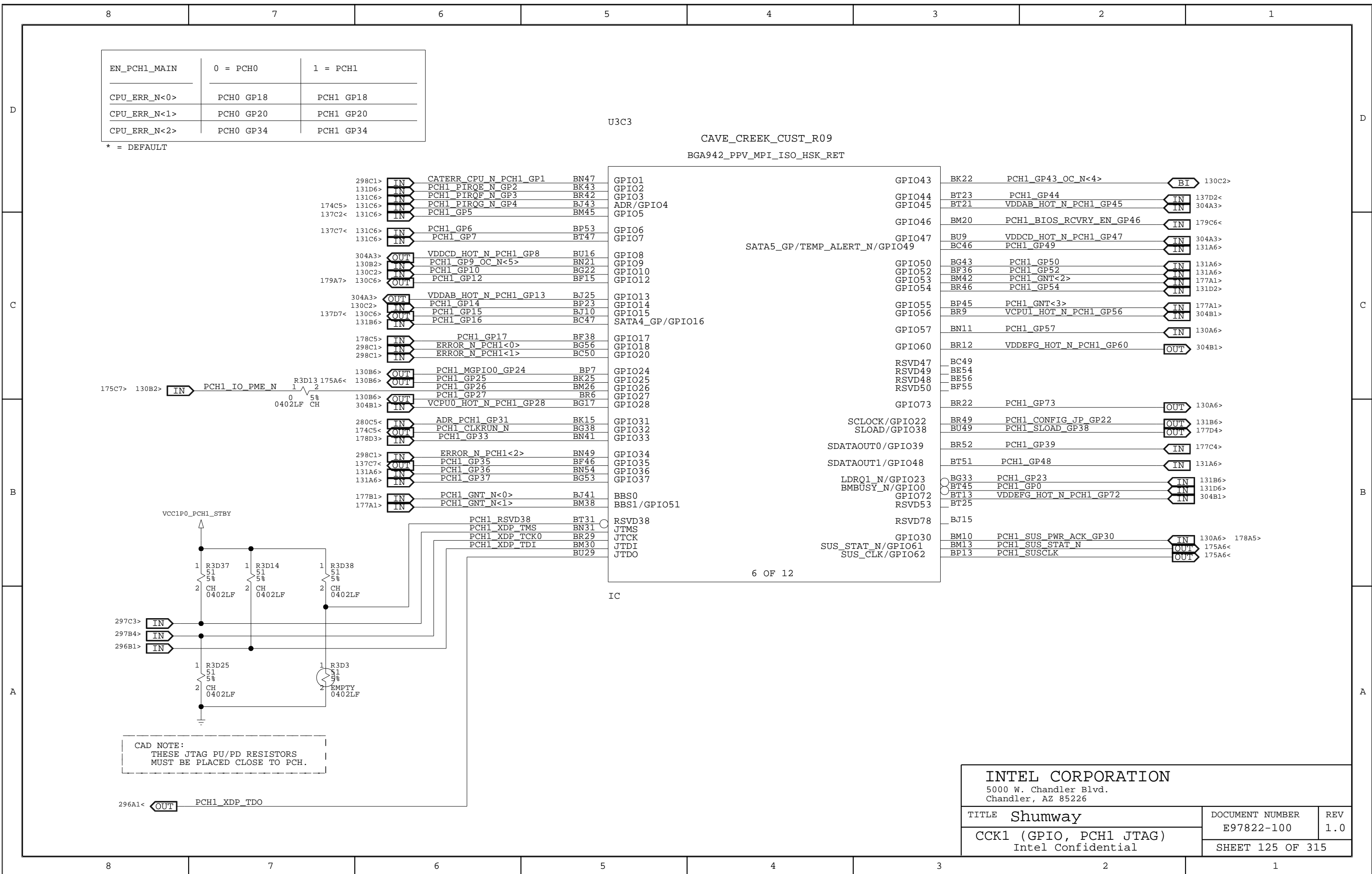


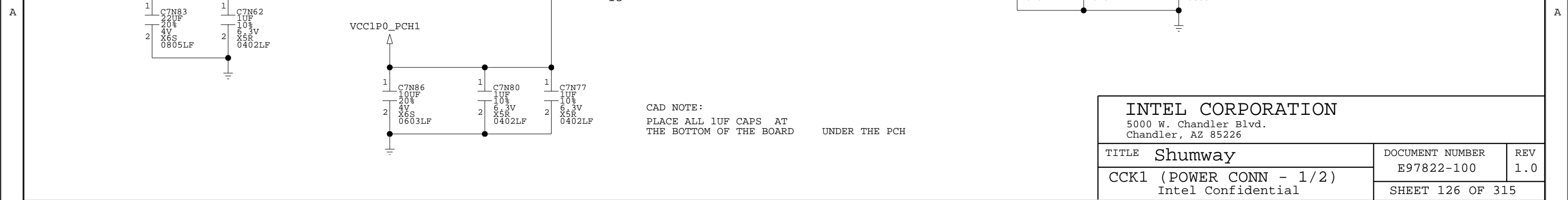






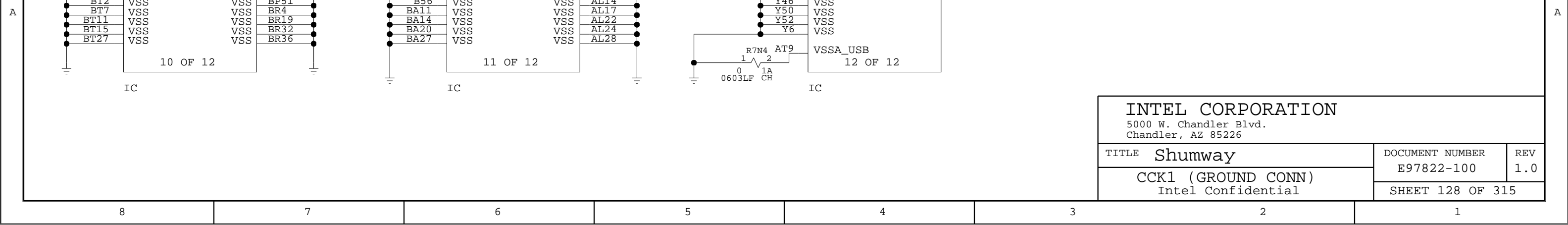






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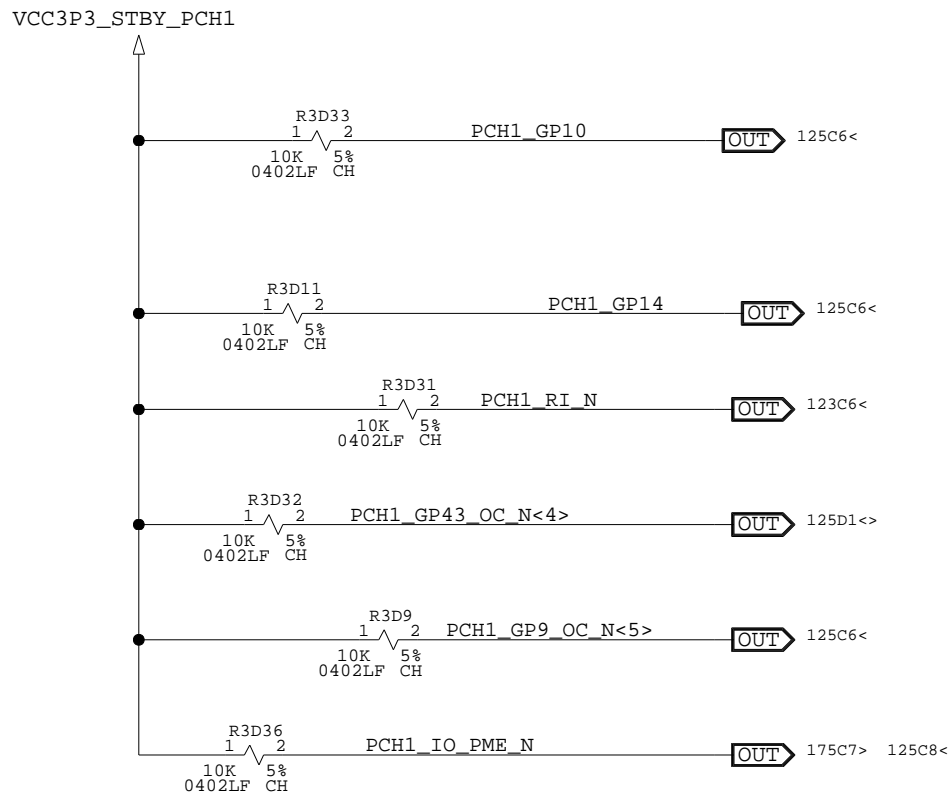
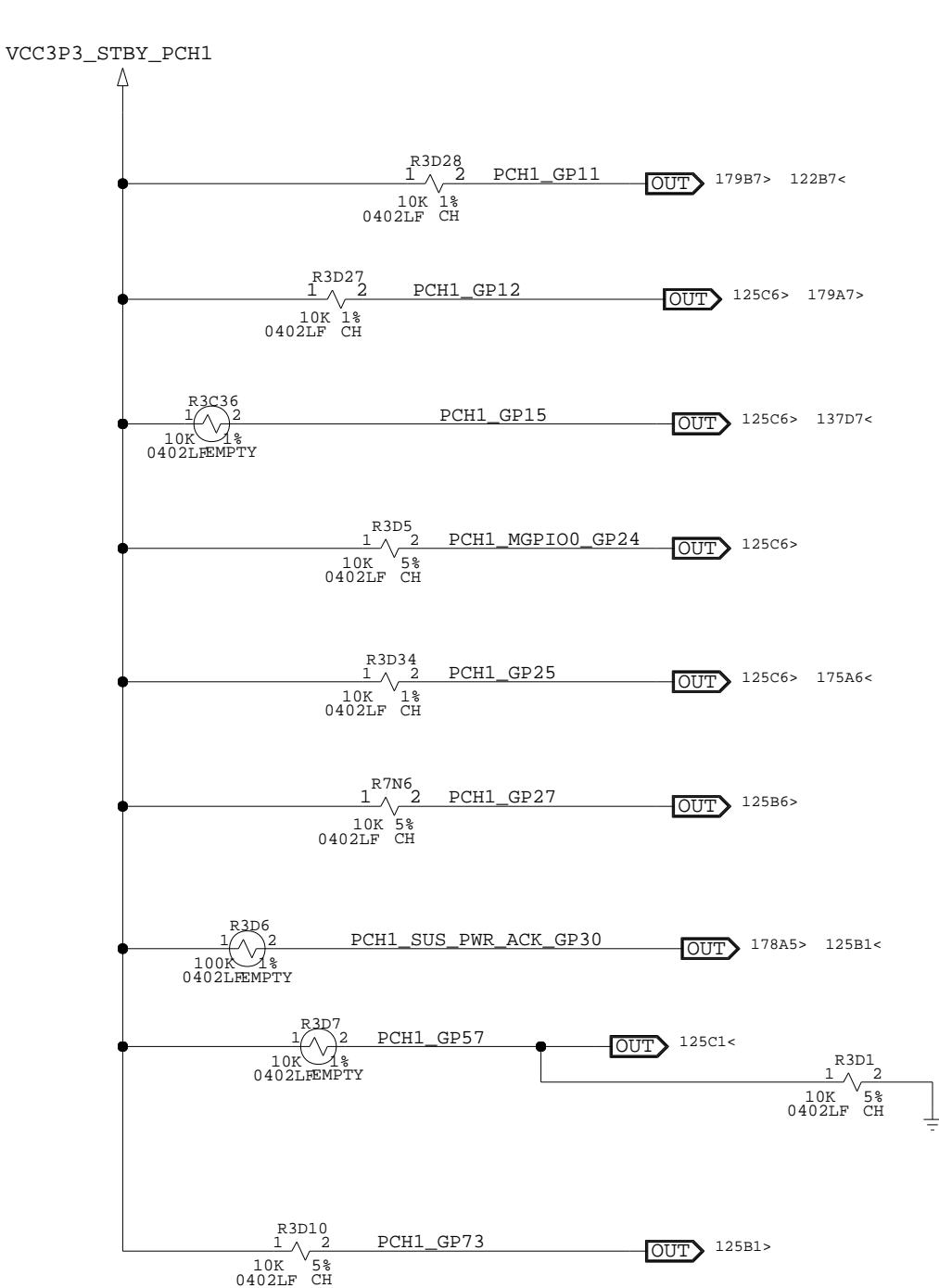
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GPIO (RESUME VOLTAGE LEVEL) TERMINATION



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PCH1 GPIO STBY TERM Intel Confidential	SHEET 130 OF 315	



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GPIO (MAIN VOLTAGE LEVEL) TERMINATION

VCC3P3\_PCH1

R3D17  
10K 1%  
0402L FEMPTY

PCH1\_GP0

OUT

125B1<

R3D43  
10K 1%  
0402L F CH

PCH1\_PIRQE\_N\_GP2

OUT

125D6<

R3D15  
10K 1%  
0402L F CH

PCH1\_PIRQF\_N\_GP3

OUT

125D6<

R3D42  
10K 1%  
0402L FEMPTY

PCH1\_PIRQG\_N\_GP4

OUT

174C5> 125C6<

R3D16  
10K 1%  
0402L F CH

PCH1\_GP5

OUT

125C6< 137C2<

R3D22  
10K 1%  
0402L F CH

PCH1\_GP6

OUT

125C6< 137C7<

R3D19  
10K 1%  
0402L F CH

PCH1\_GP7

OUT

125C6<

R4C49  
10K 1%  
0402L F CH

PCH1\_GP16

OUT

125C6<

R3D45  
10K 1%  
0402L F CH

PCH1\_GP19

OUT

178C5> 122C7<

R3D20  
10K 1%  
0402L F CH

PCH1\_CONFIG\_JP\_GP22

OUT

125B1>

R3D40  
10K 1%  
0402L F CH

PCH1\_GP23

OUT

125B1<

R3D23  
10K 1%  
0402L F CH

PCH1\_GP36

OUT

125B6<

R4C53  
10K 1%  
0402L FEMPTY

PCH1\_GP37

OUT

125B6<

R3D21  
10K 1%  
0402L F CH

PCH1\_GP48

OUT

125B1<

R4C45  
10K 1%  
0402L F CH

PCH1\_GP49

OUT

125C1<

R3D44  
10K 1%  
0402L F CH

PCH1\_GP50

OUT

125C1<

R3D41  
10K 1%  
0402L FEMPTY

PCH1\_GP52

OUT

125C1<

VCC3P3\_PCH1

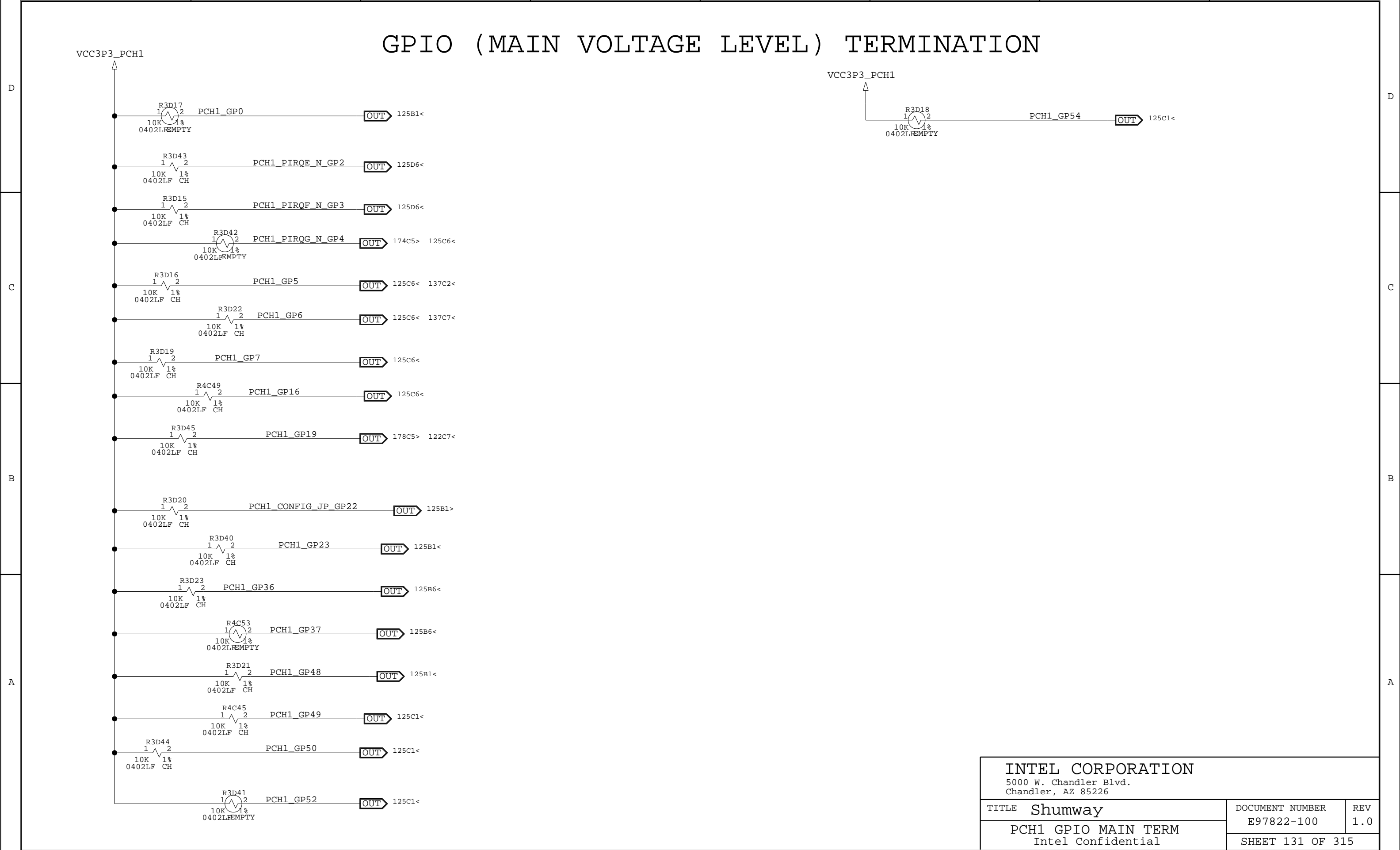
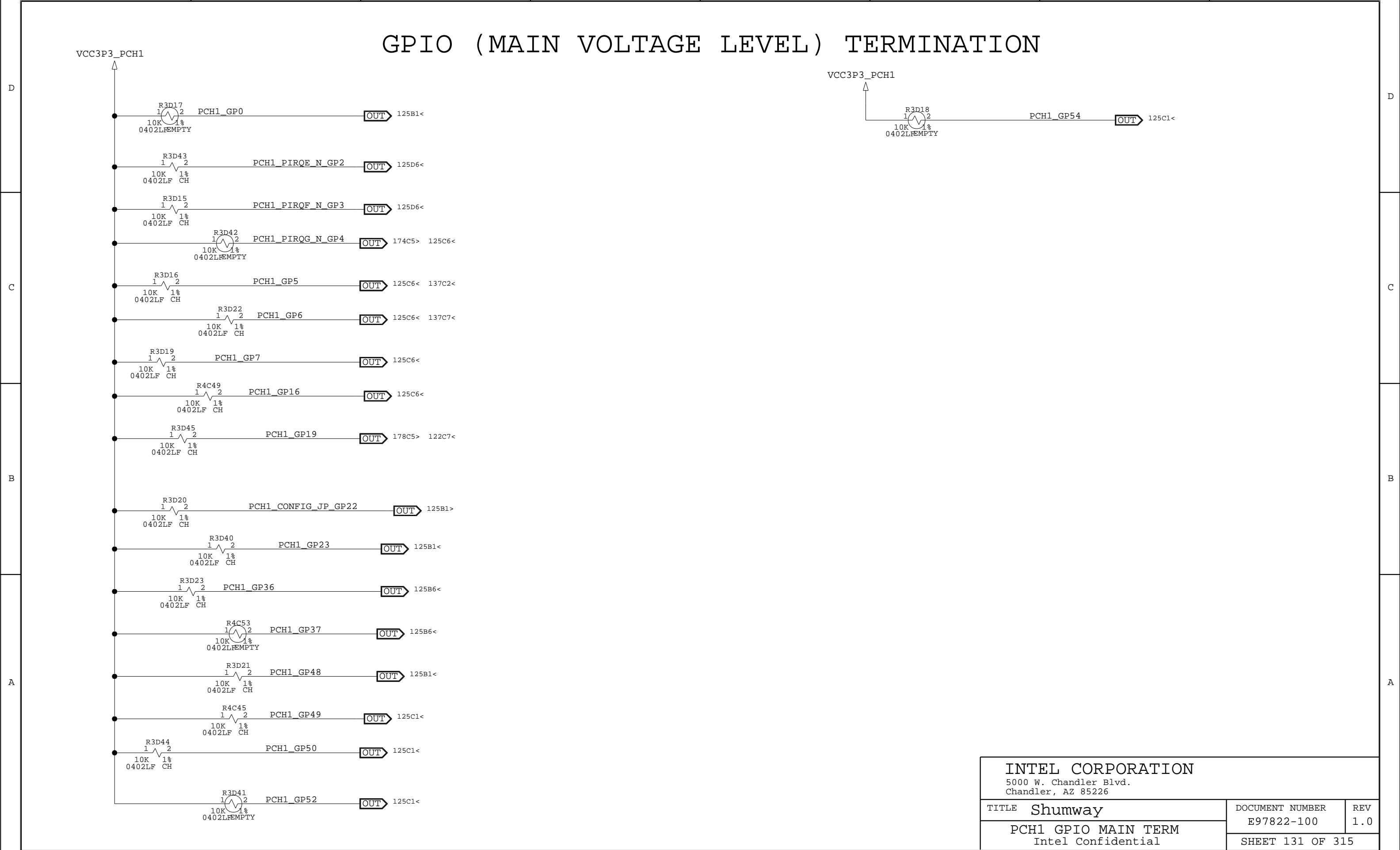
R3D18  
10K 1%  
0402L FEMPTY

PCH1\_GP54

OUT

125C1<

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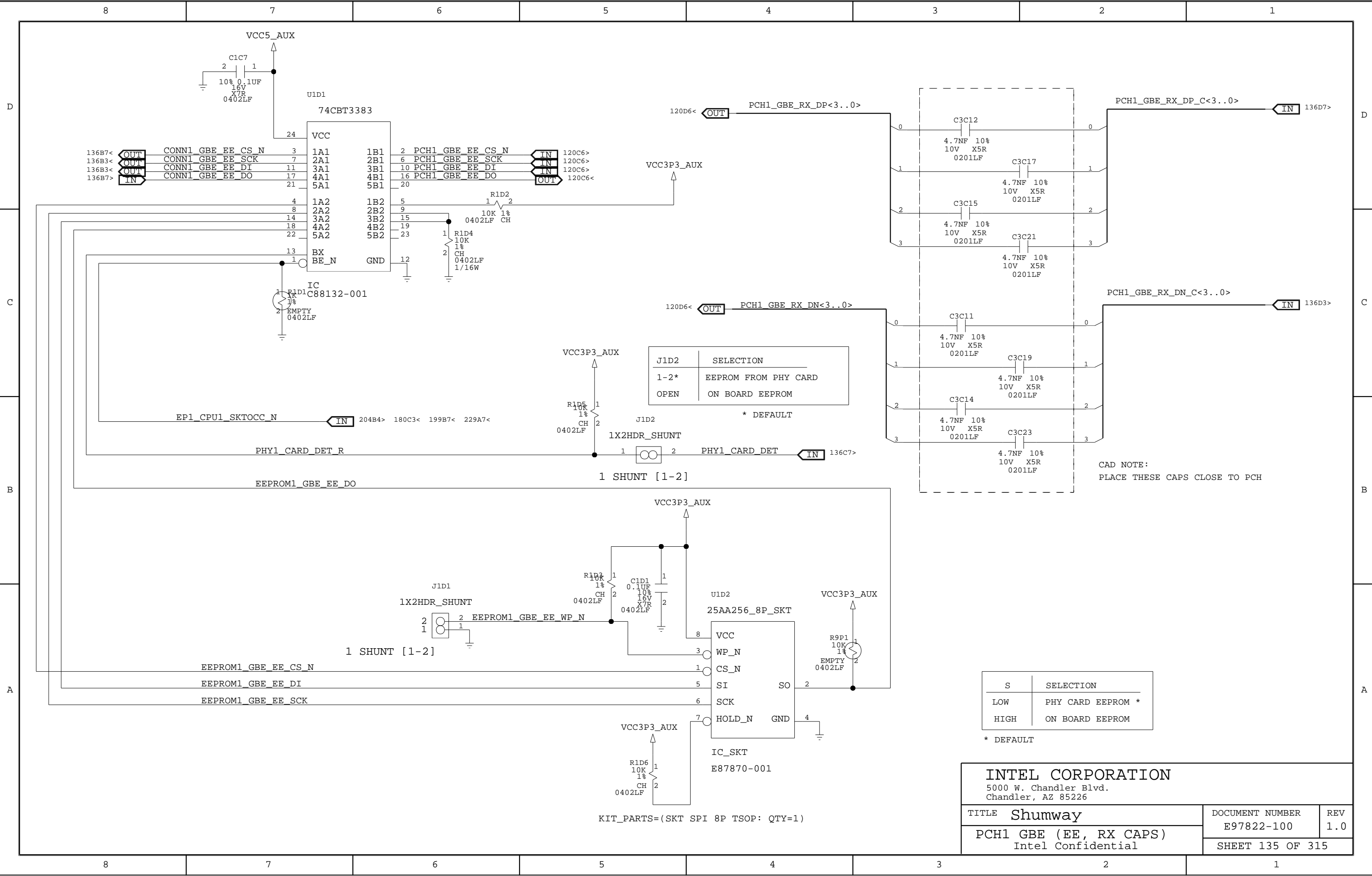
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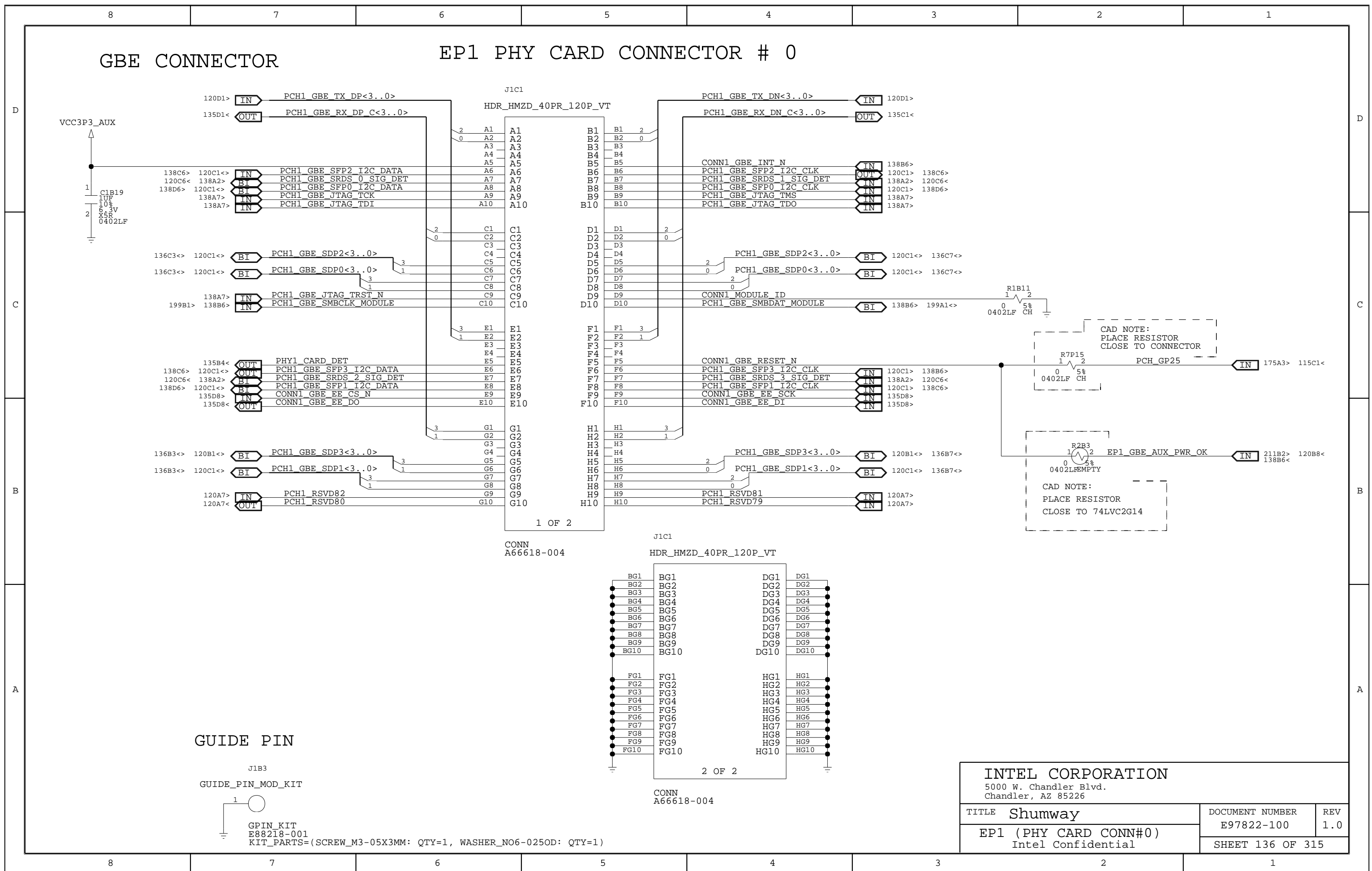
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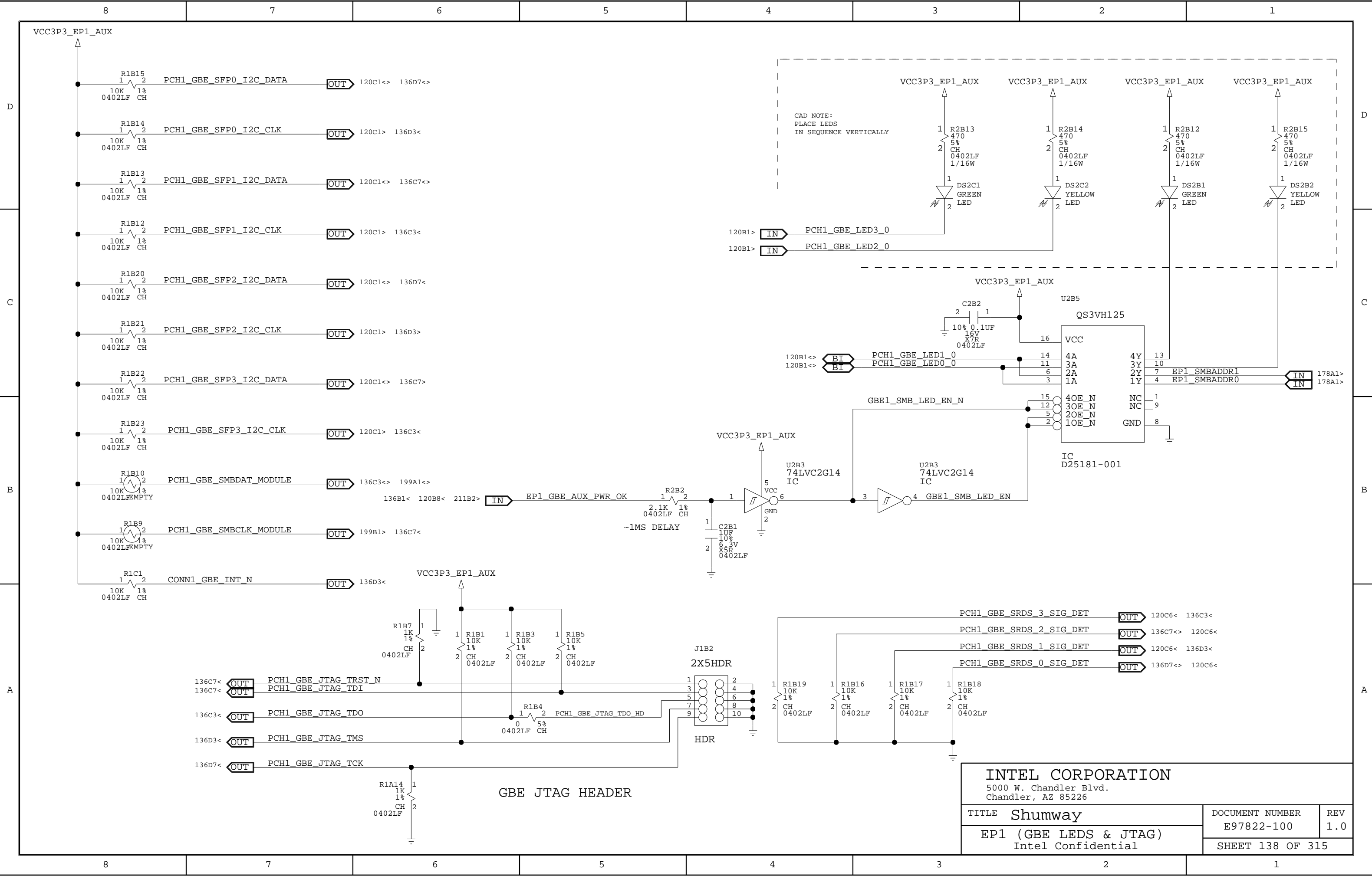
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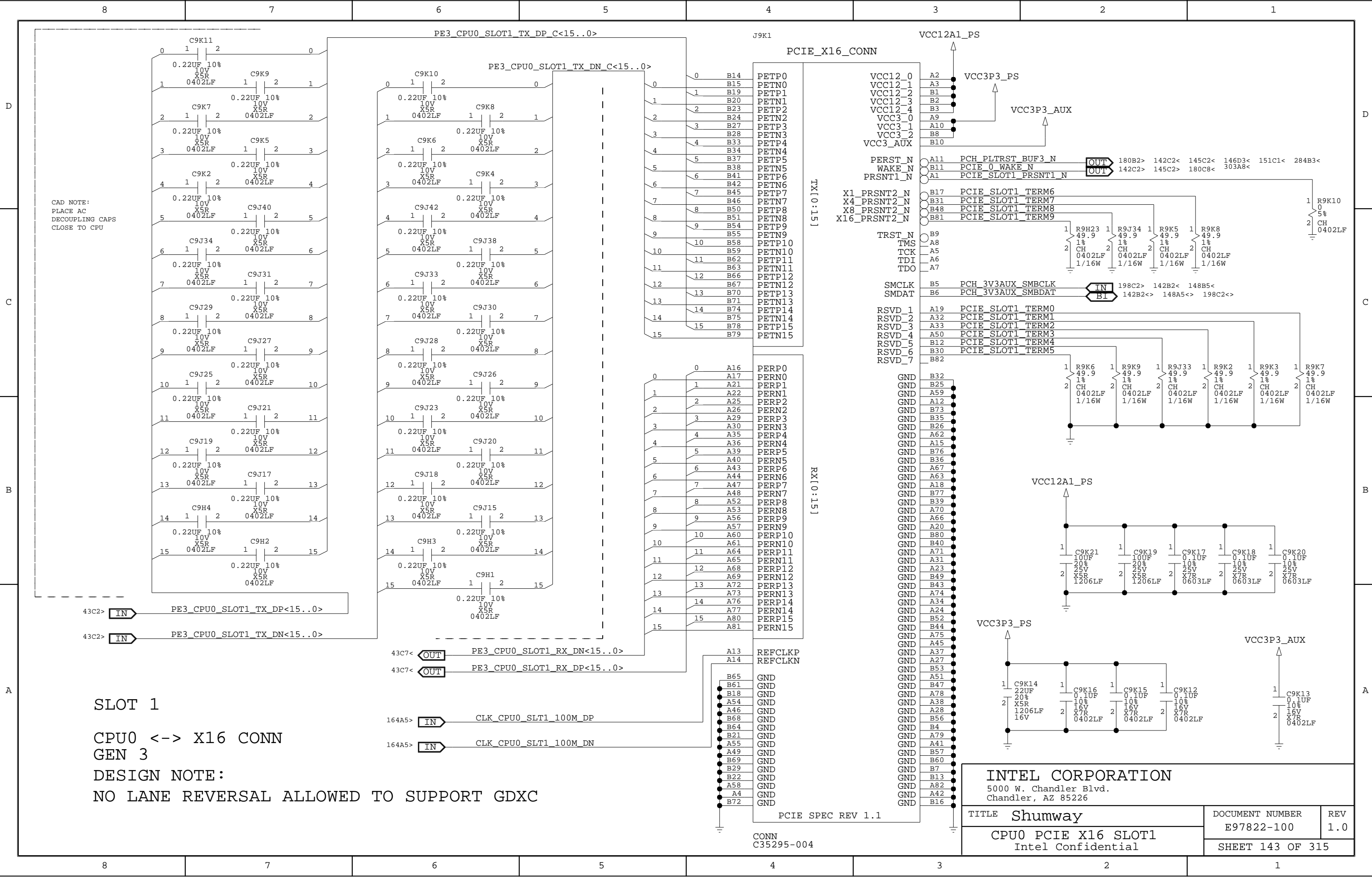
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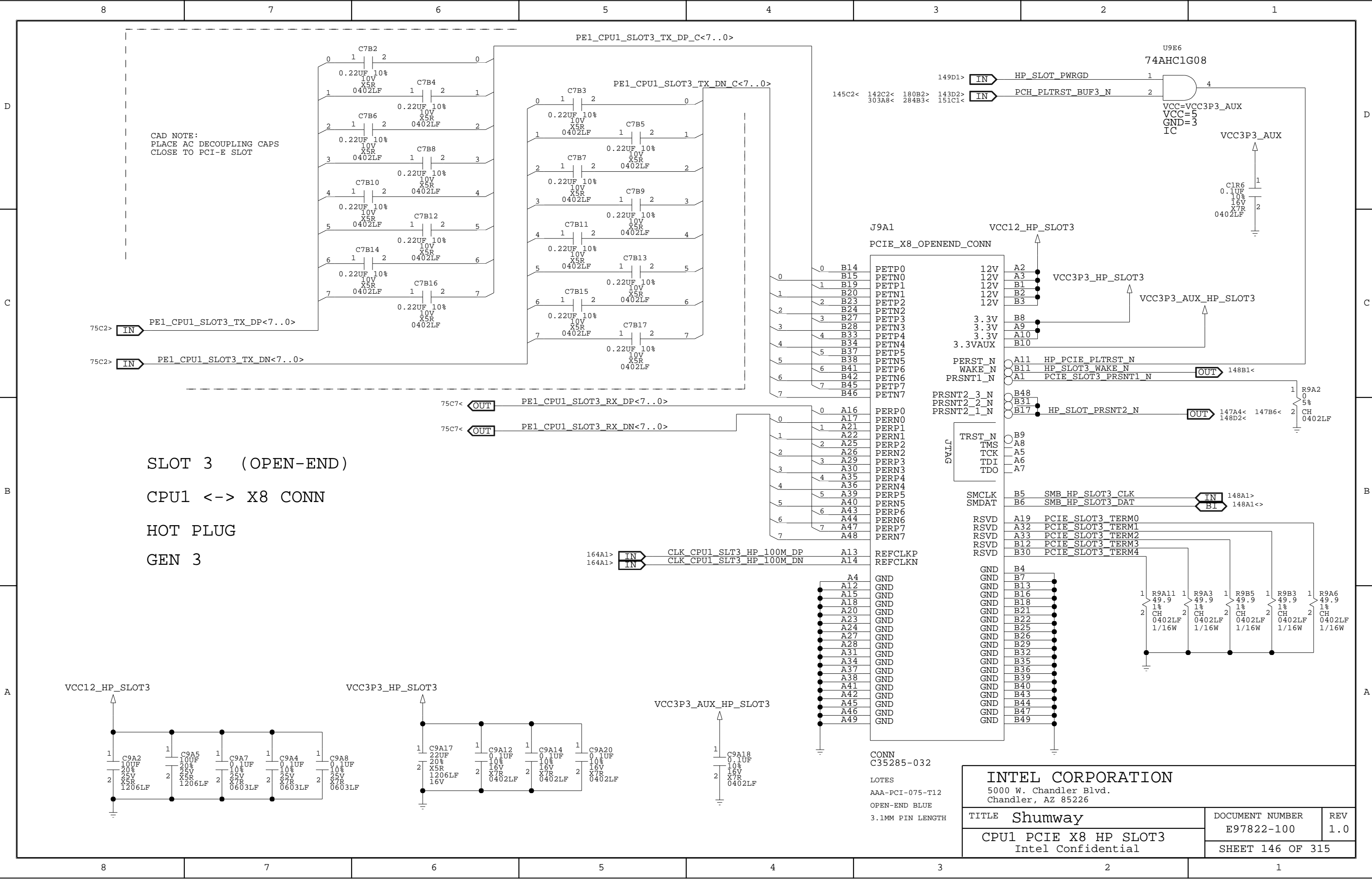
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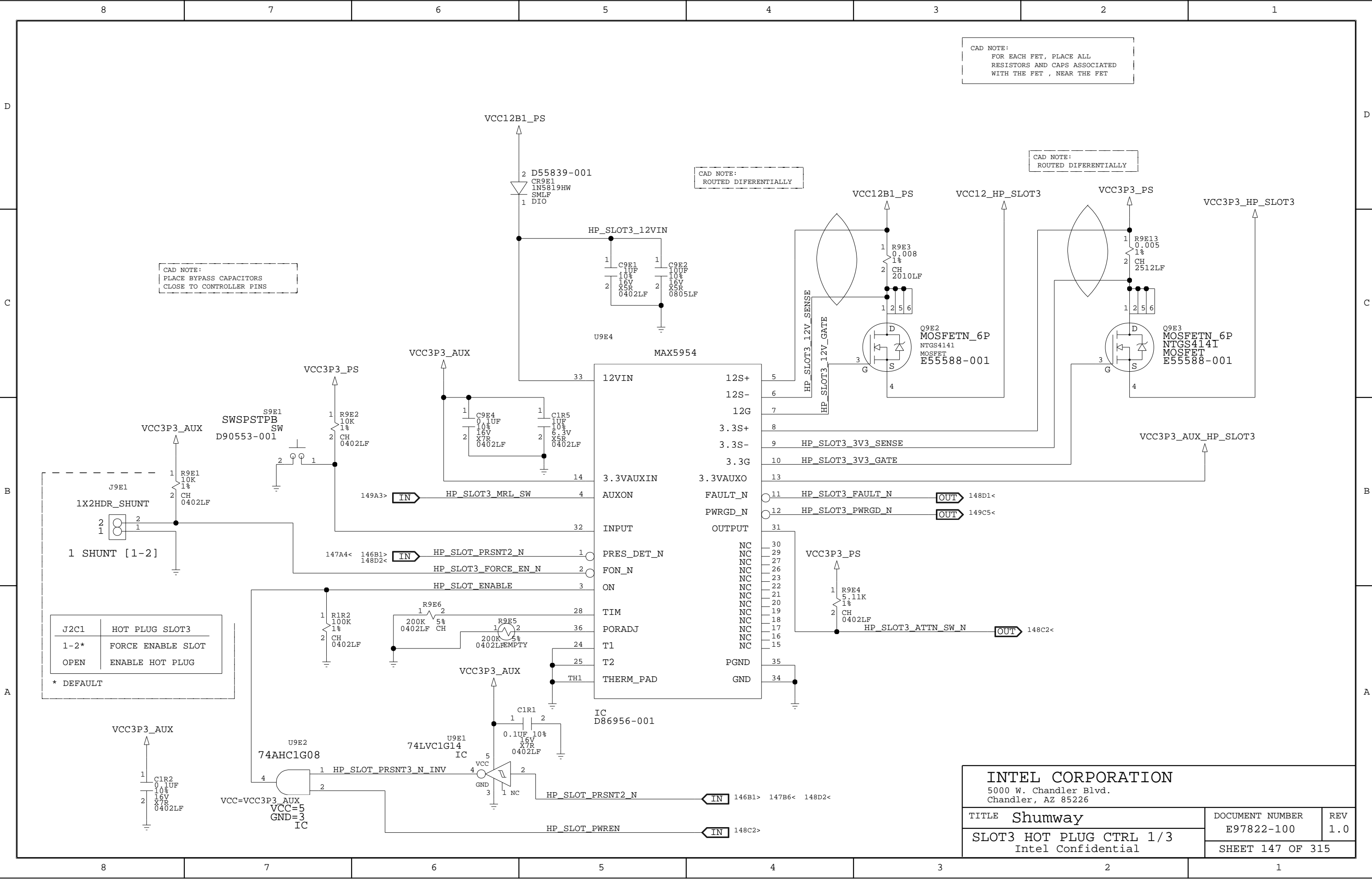
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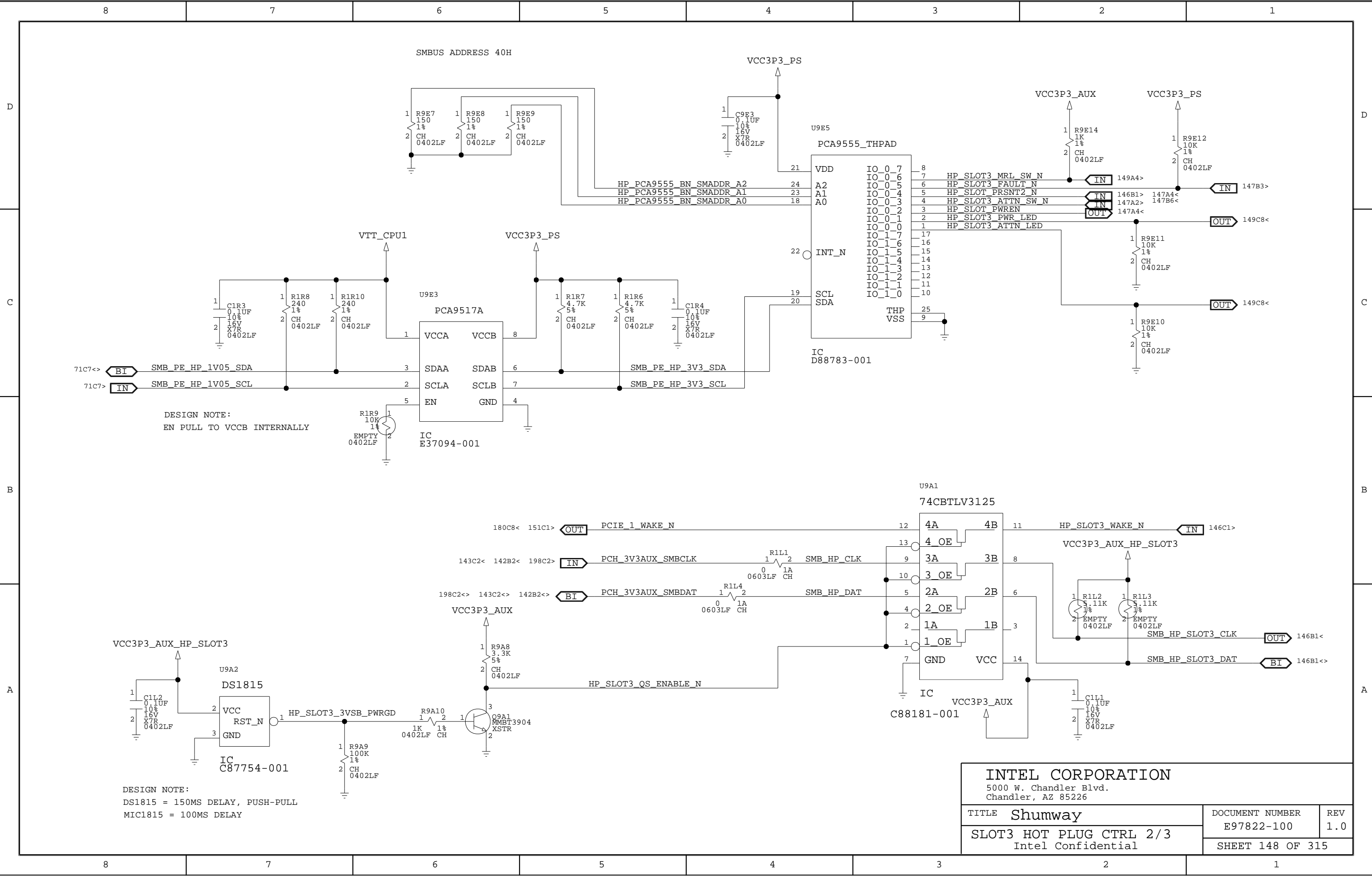
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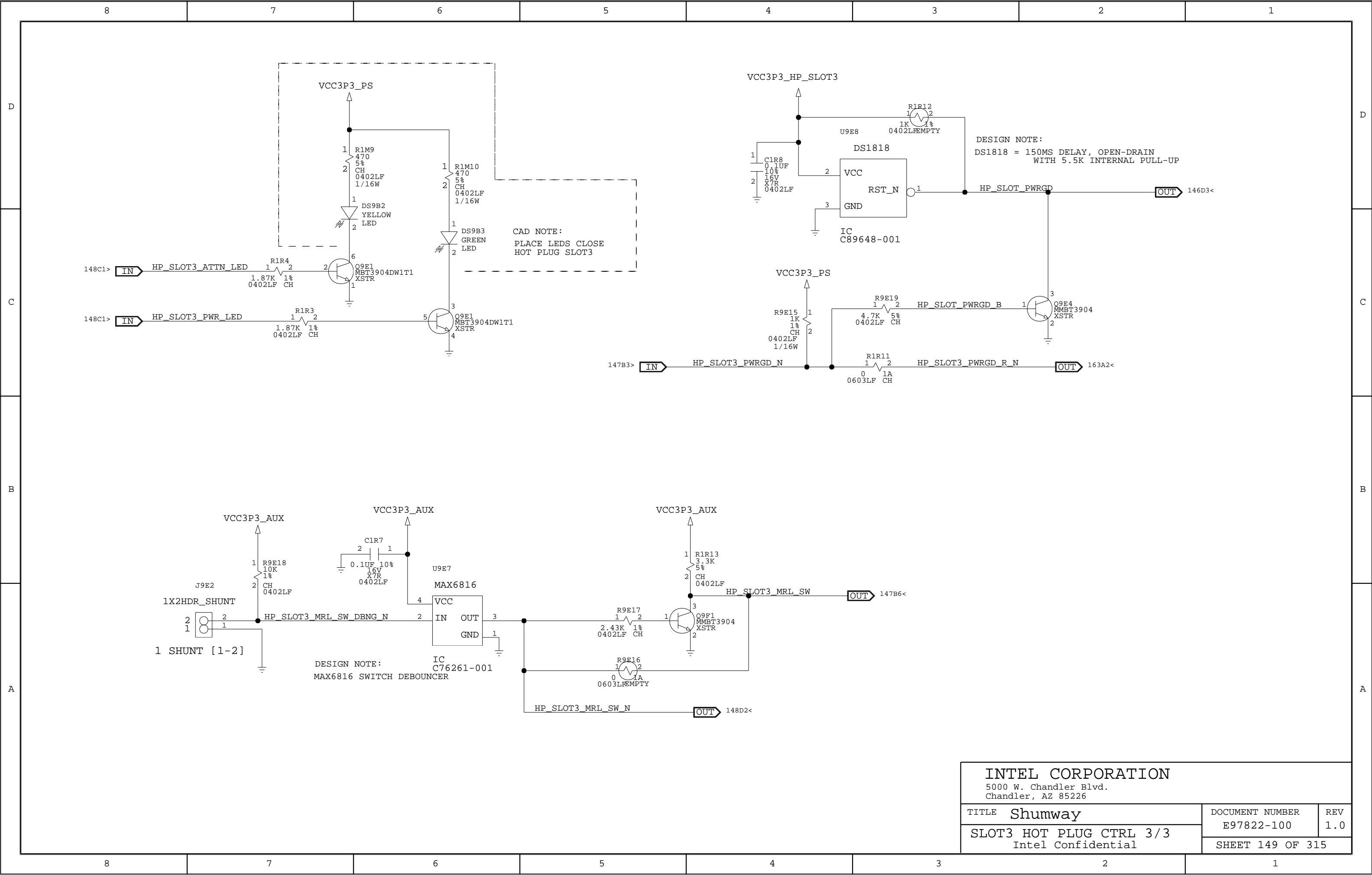












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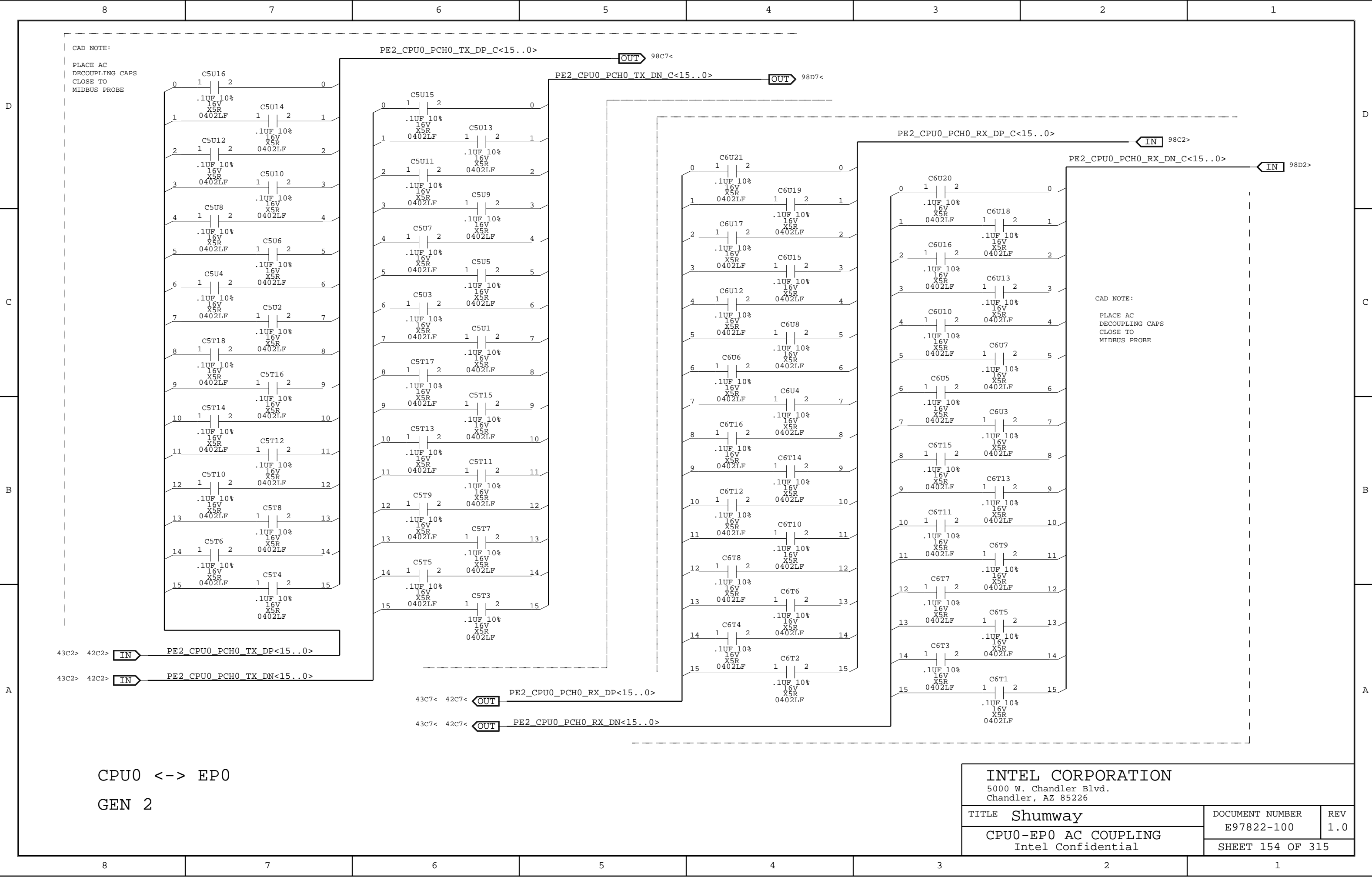
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8	7	6	5	4	3	2	1
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C							
B							
A							
8	7	6	5	4	3	2	1

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SEC - DMI AC COUPLING Intel Confidential	SHEET 152 OF 315	







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D							D
C							C
B							B
A							A
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CPU1-EP1 AC COUPLING			
Intel Confidential		SHEET 156 OF 315	

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D							D												
C							C												
B							B												
A							A												
						<table><tr><td colspan="3">INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226</td></tr><tr><td>TITLE</td><td>Shumway</td><td>DOCUMENT NUMBER E97822-100</td></tr><tr><td colspan="2">BLANK PAGE Intel Confidential</td><td>REV 1.0</td></tr><tr><td colspan="2"></td><td>SHEET 157 OF 315</td></tr></table>		INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226			TITLE	Shumway	DOCUMENT NUMBER E97822-100	BLANK PAGE Intel Confidential		REV 1.0			SHEET 157 OF 315
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## CLOCK GENERATORS

C

C

B

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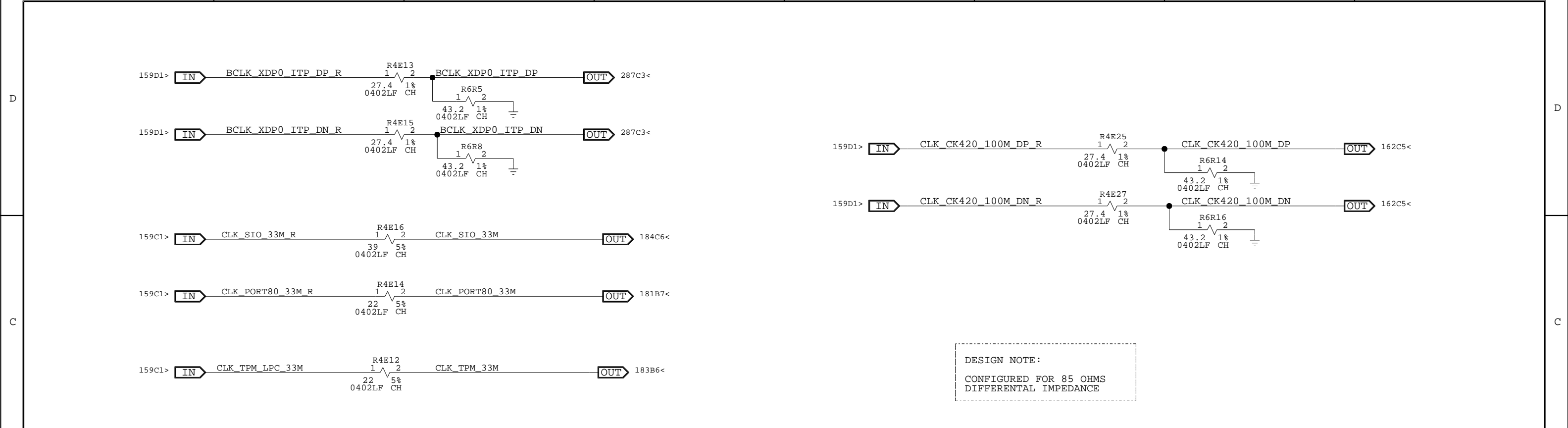
SEC - CLOCK GENERATORS  
Intel Confidential

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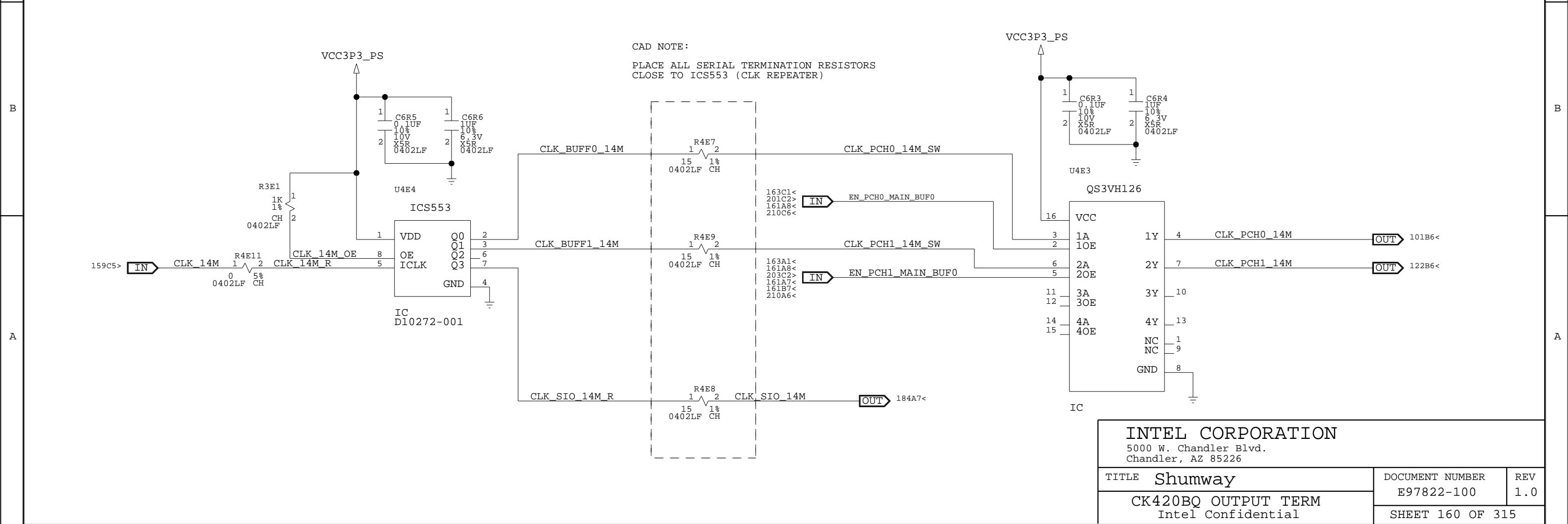
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DESIGN NOTE:  
CONFIGURED FOR 85 OHMS  
DIFFERENTIAL IMPEDANCE

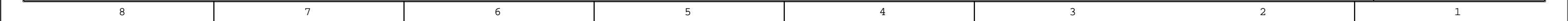


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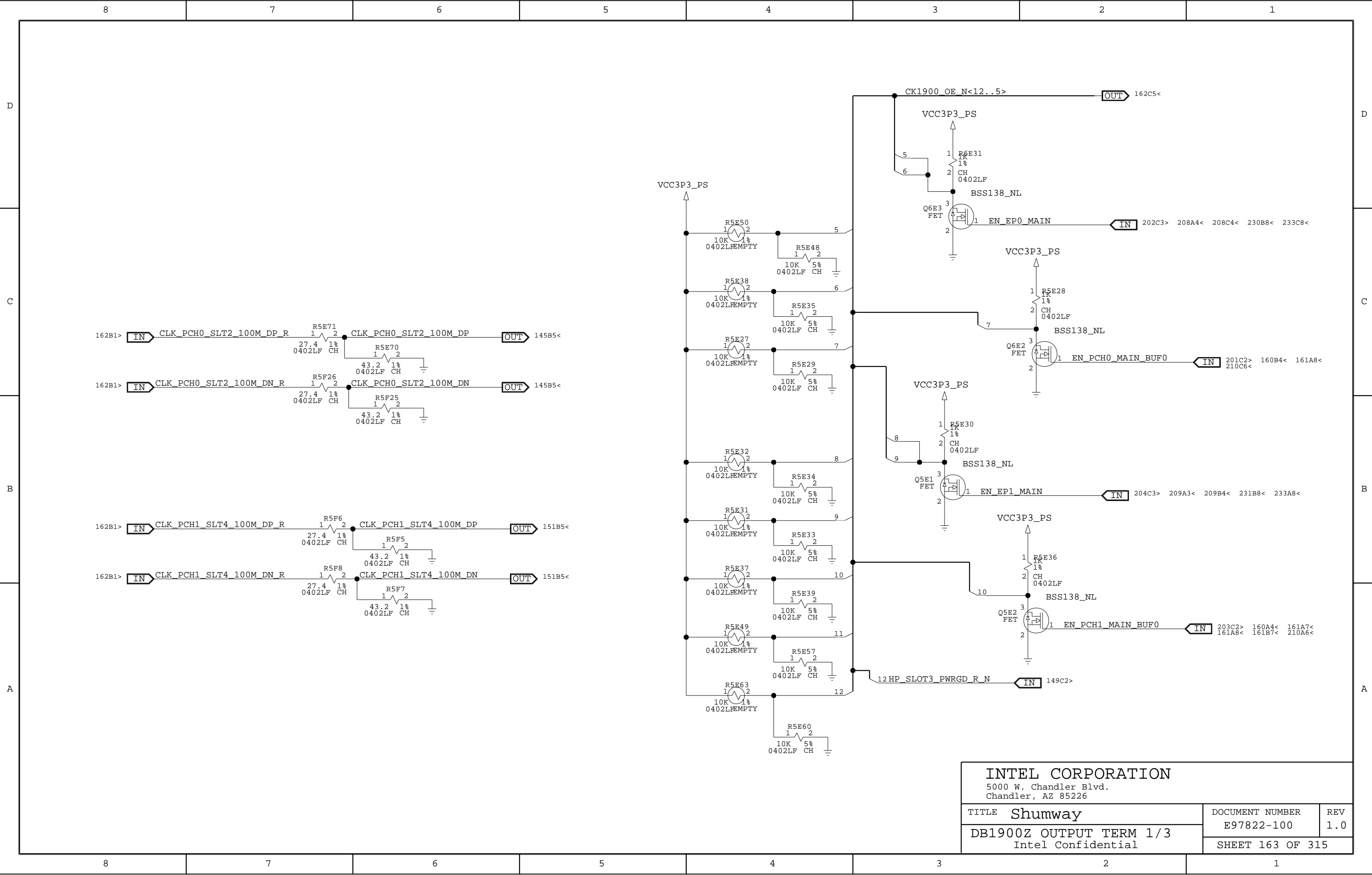
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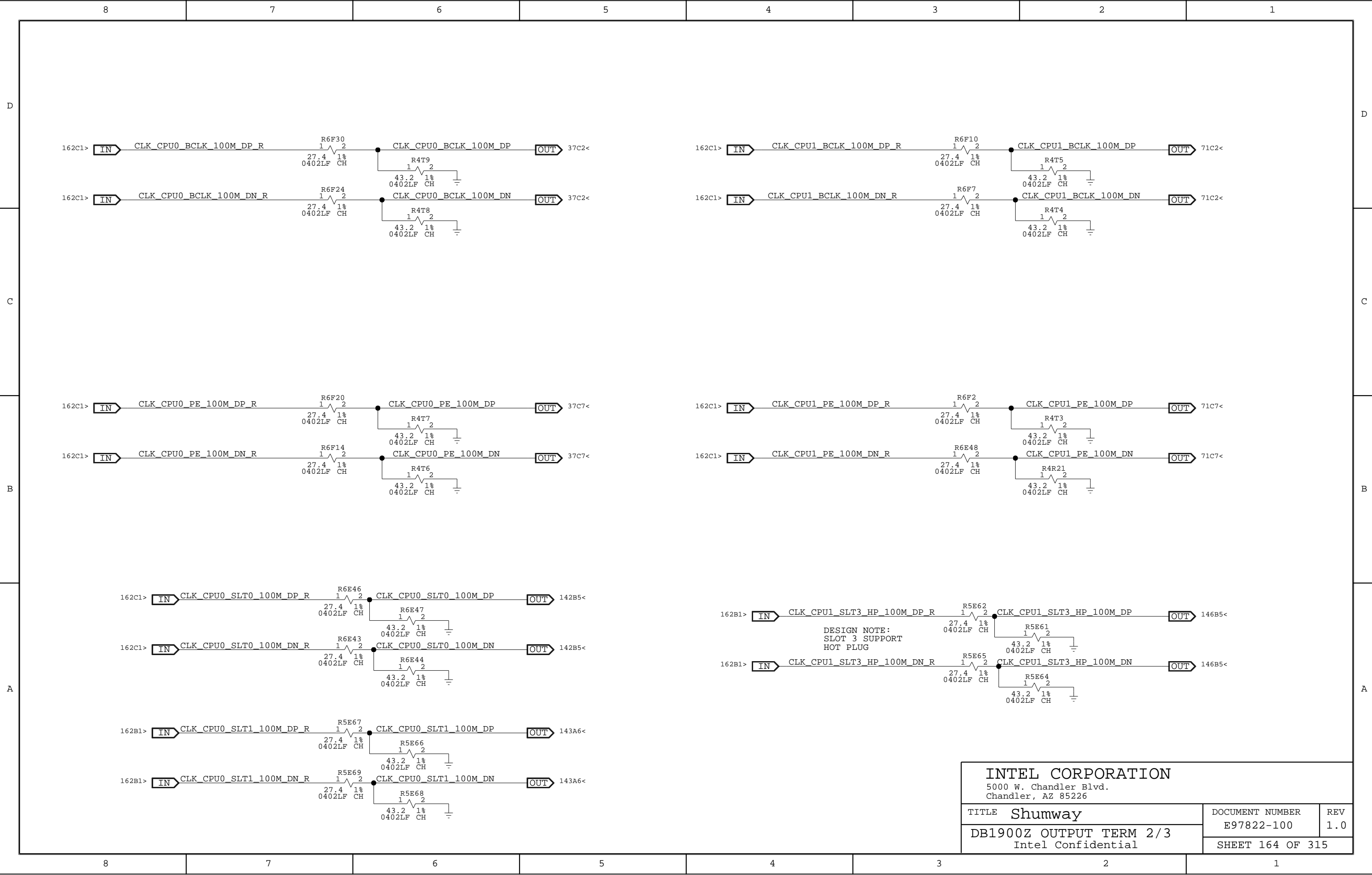
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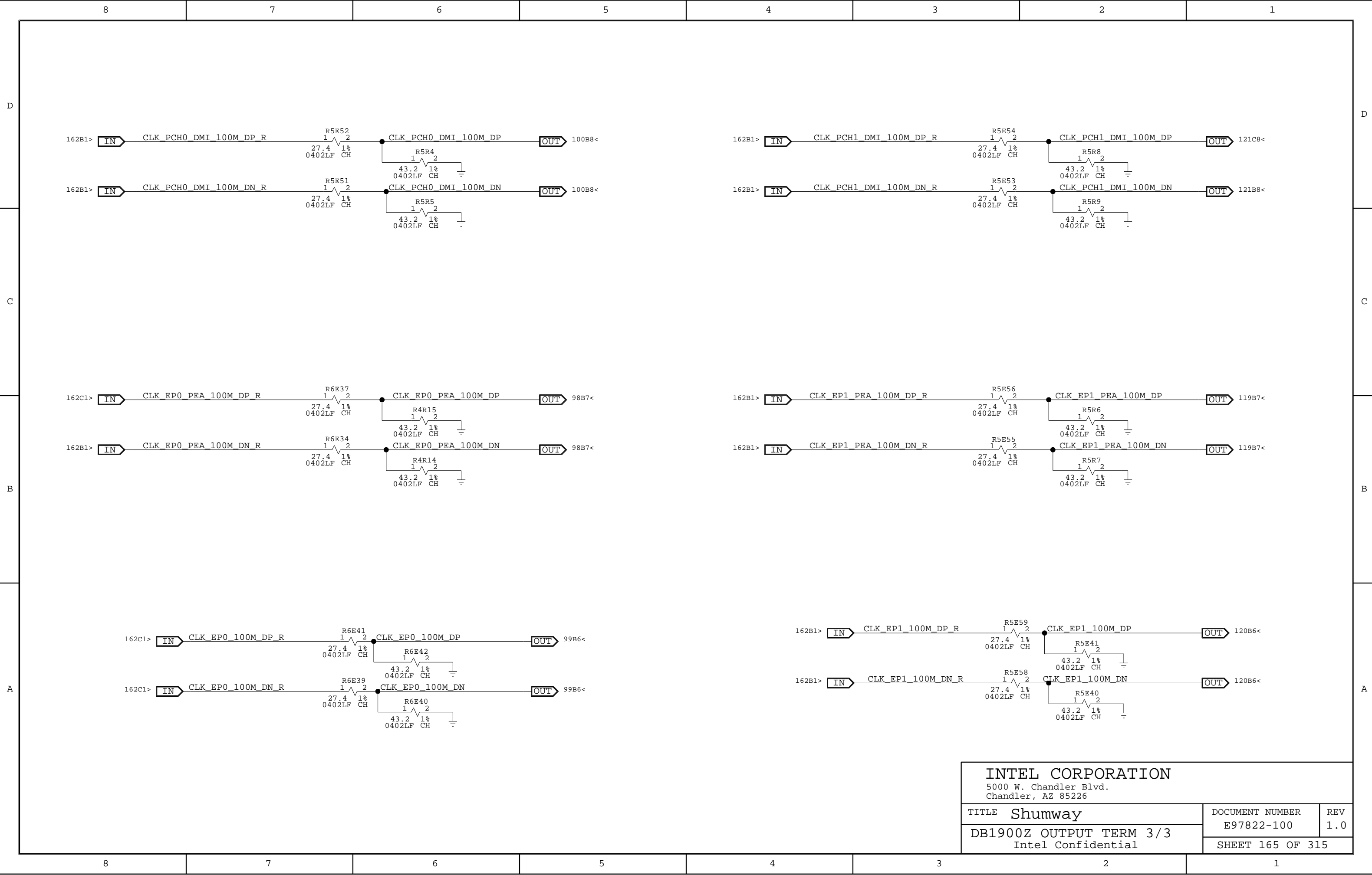












162B1>

IN

CLK\_PCH1\_DMI\_100M\_DP\_R

R5E54

1

2

27.4

0402LF

1%

CH

●

CLK\_PCH1\_DMI\_100M\_DP

OUT

121C8<

R5R8

1

2

43.2

0402LF

1%

CH

●

⏏

R5E53

1

2

27.4

0402LF

1%

CH

●

CLK\_PCH1\_DMI\_100M\_DN\_R

IN

●

CLK\_PCH1\_DMI\_100M\_DN

OUT

121B8<

R5R9

1

2

43.2

0402LF

1%

CH

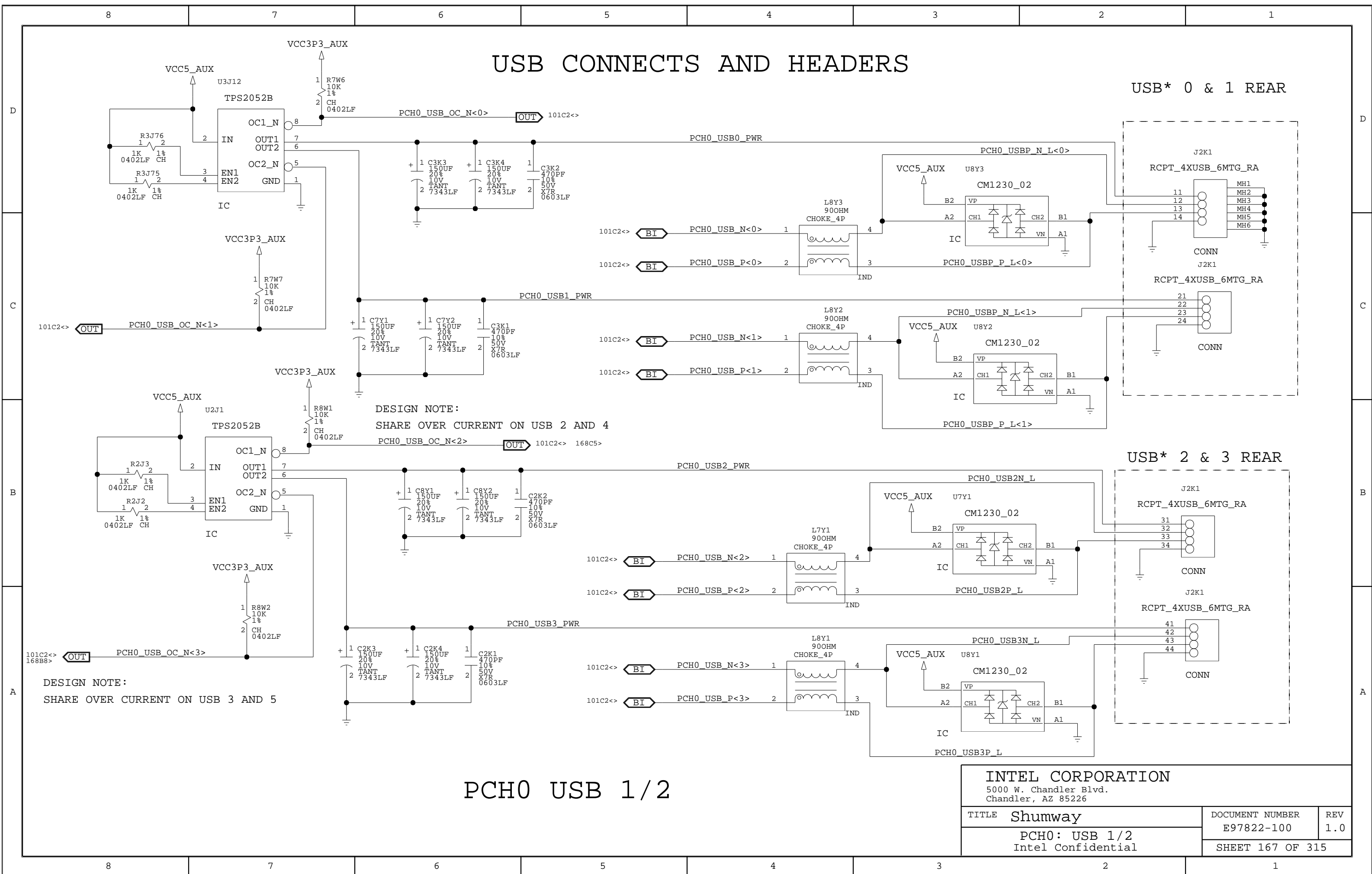
●

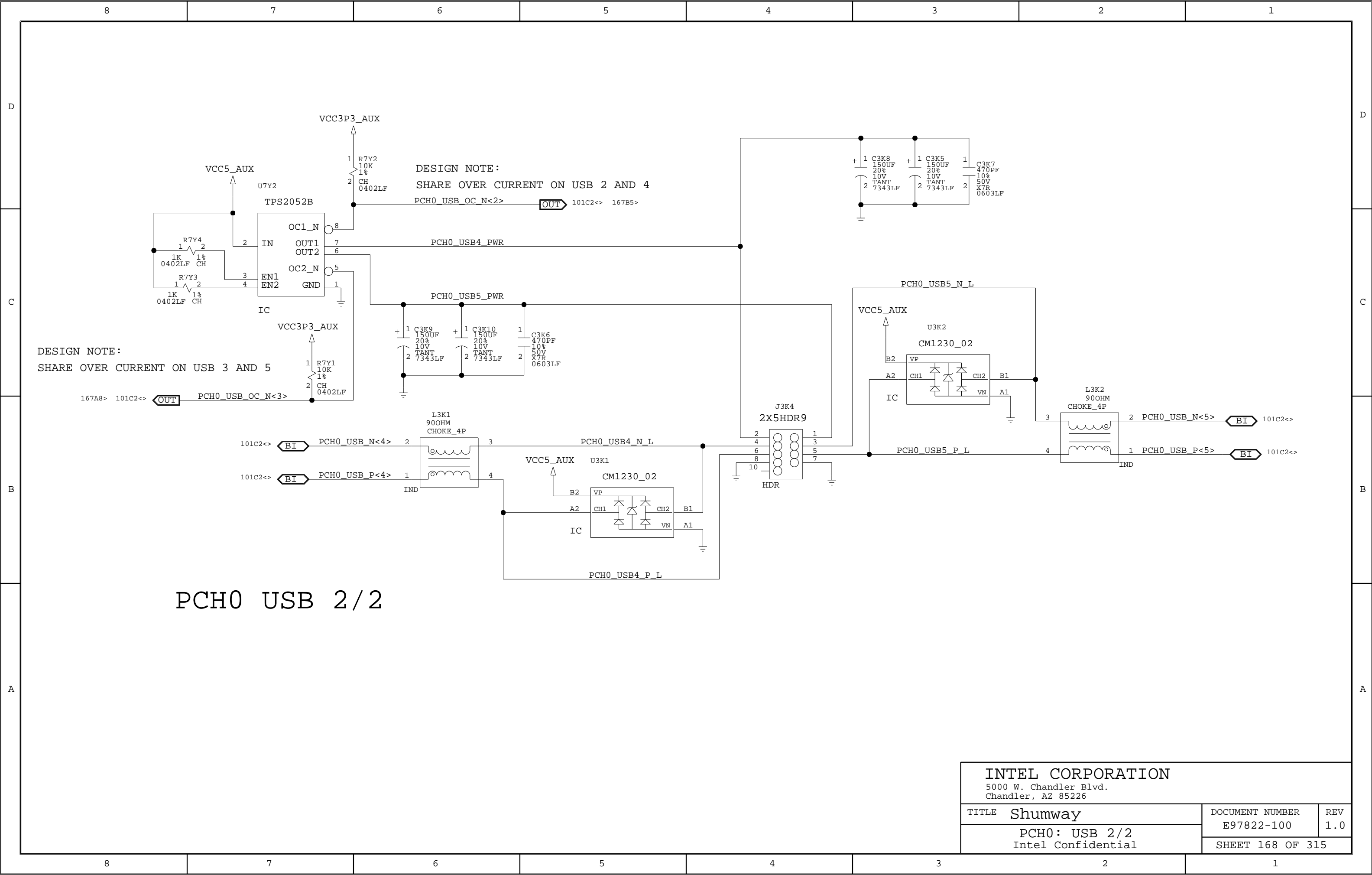
⏏

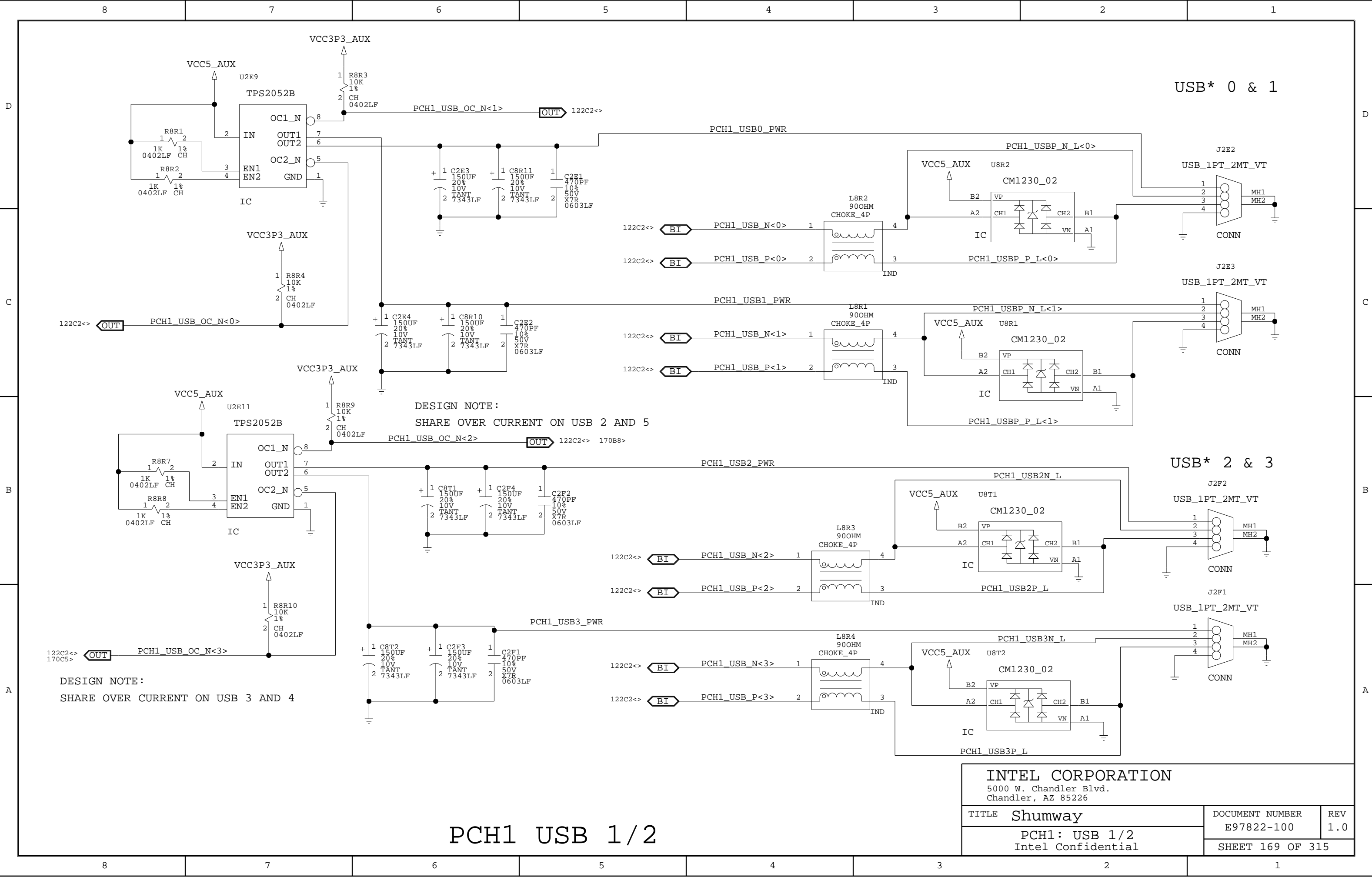
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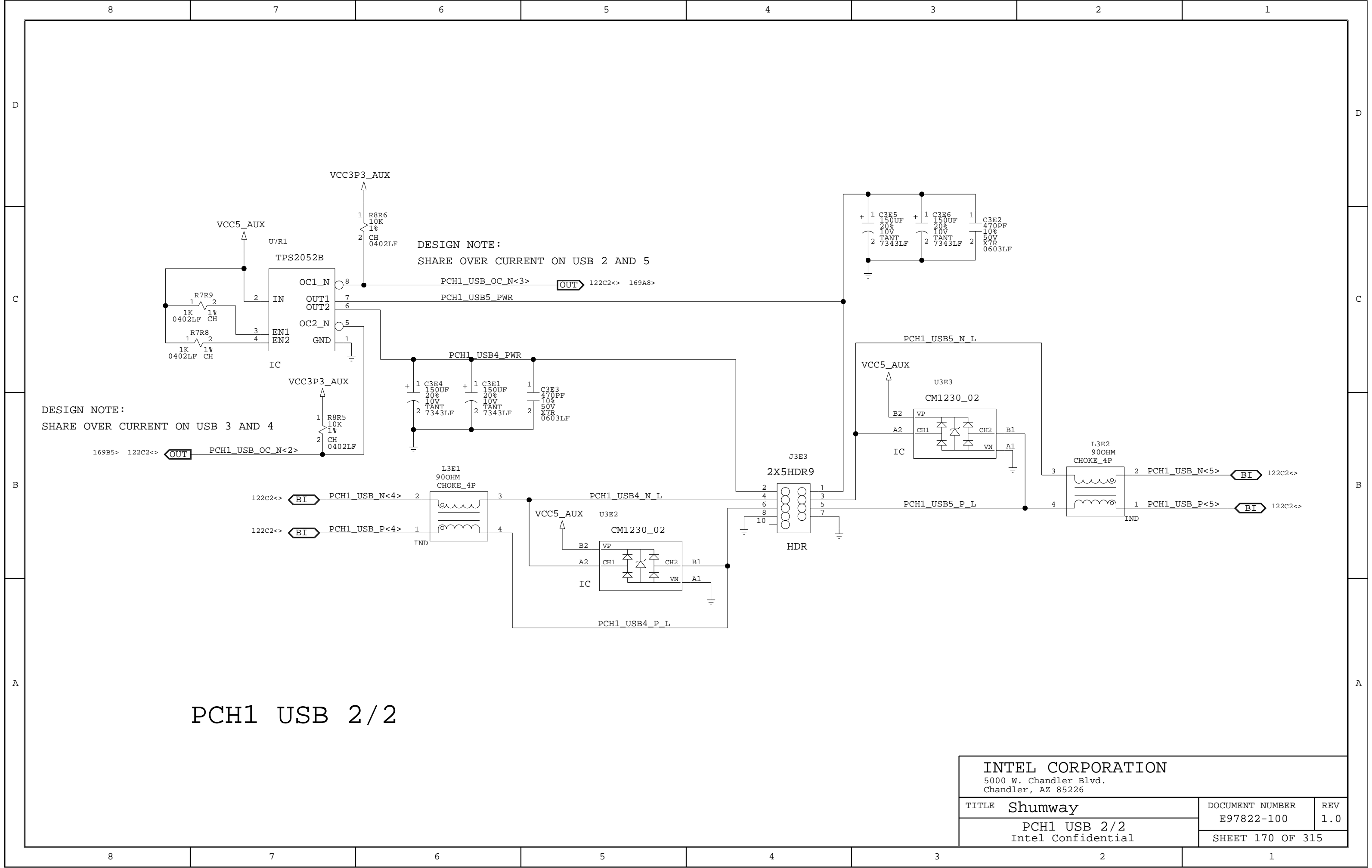


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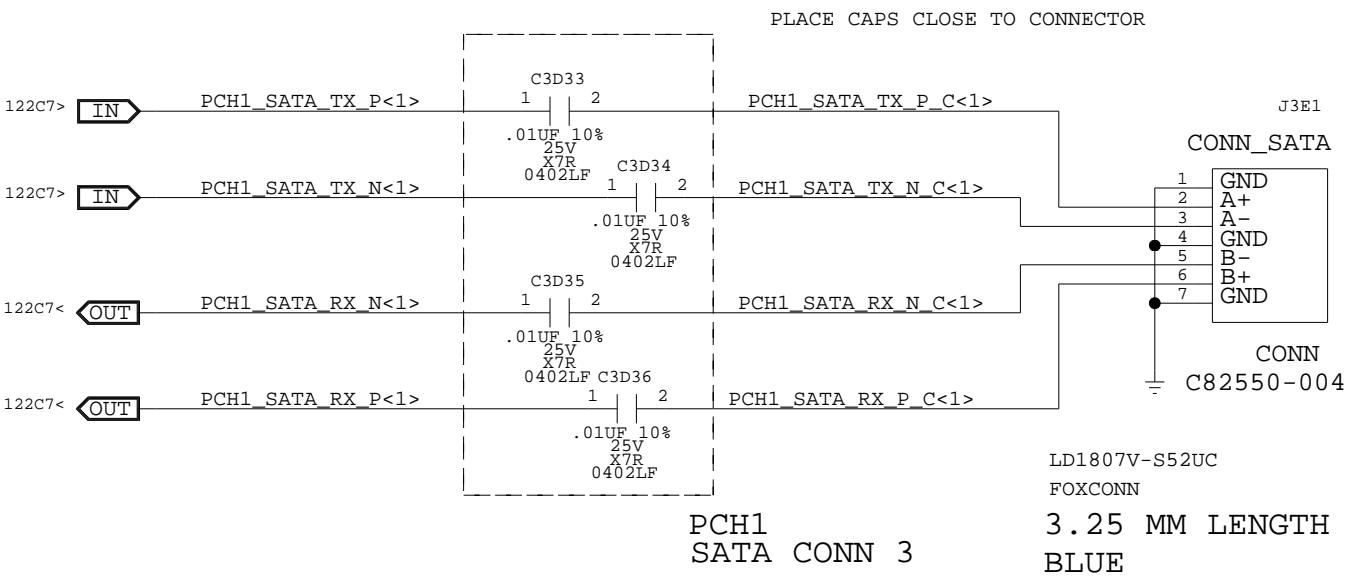
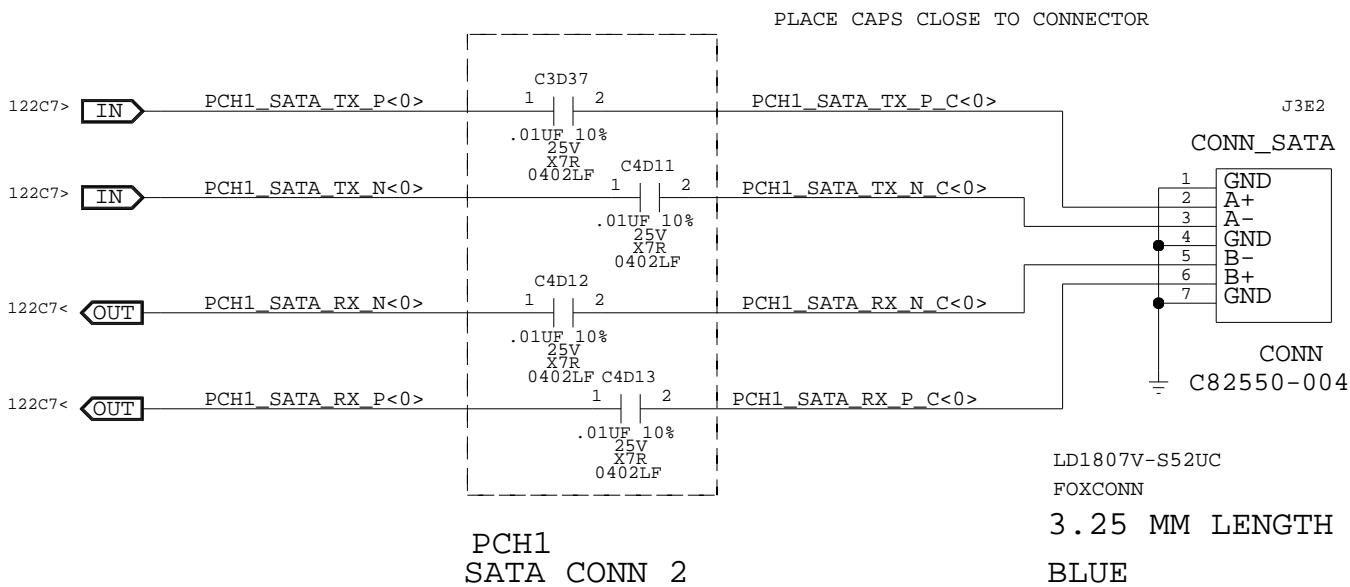
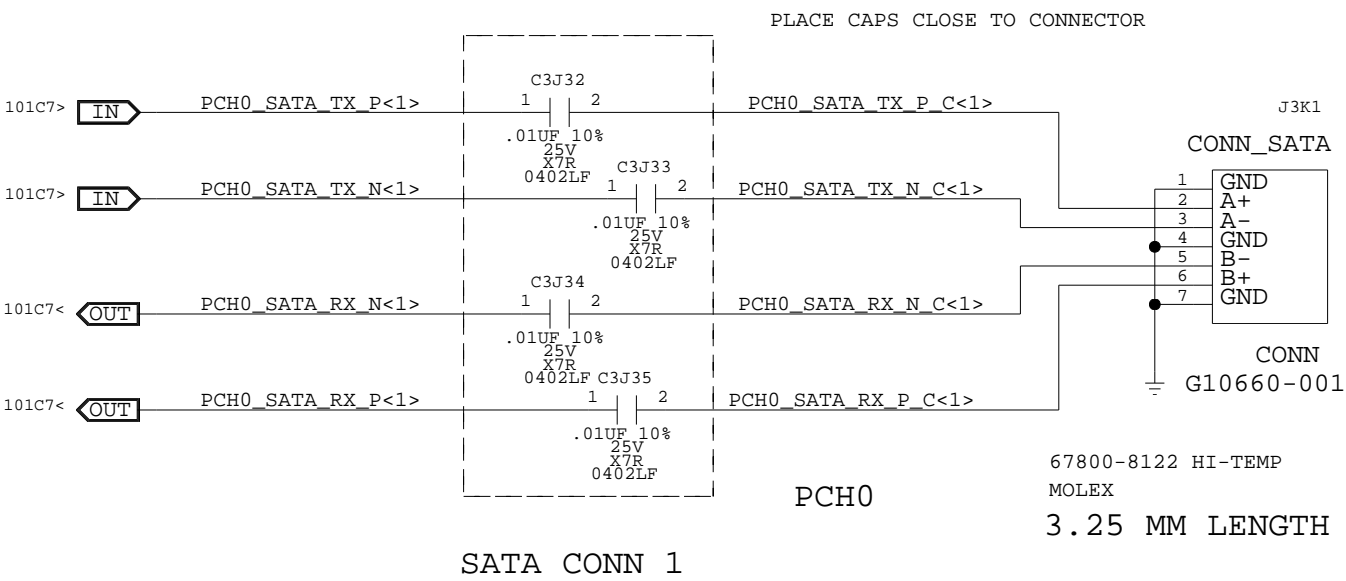
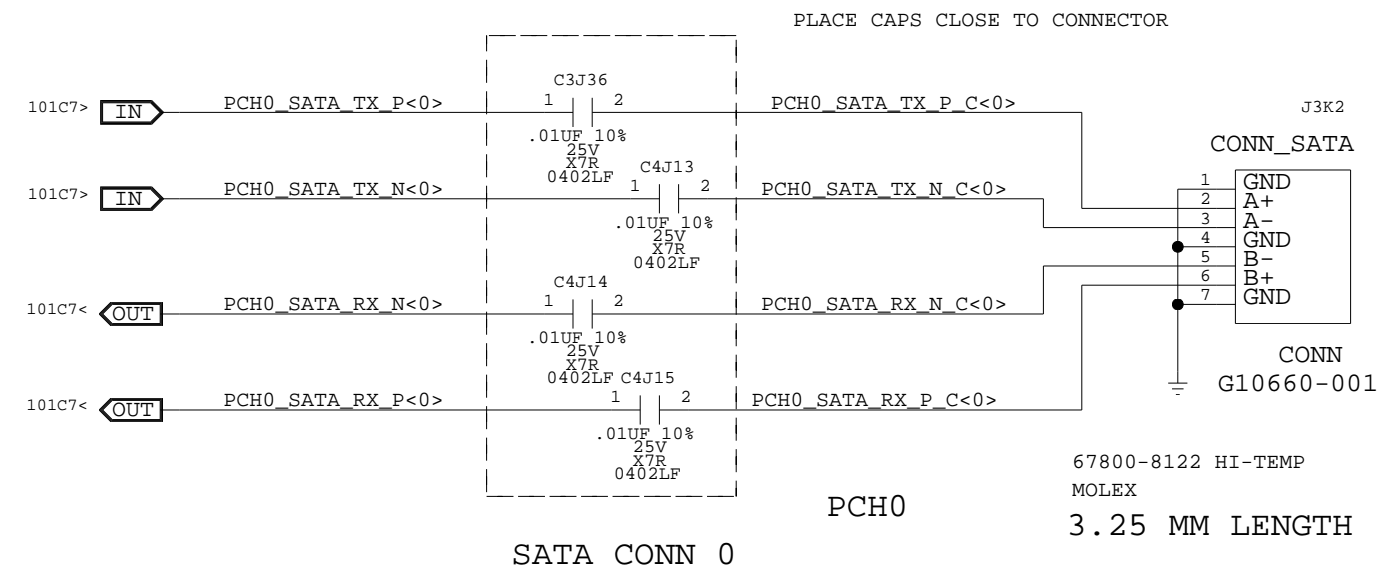








SATA CONNECTORS FROM PCH0 AND PCH1



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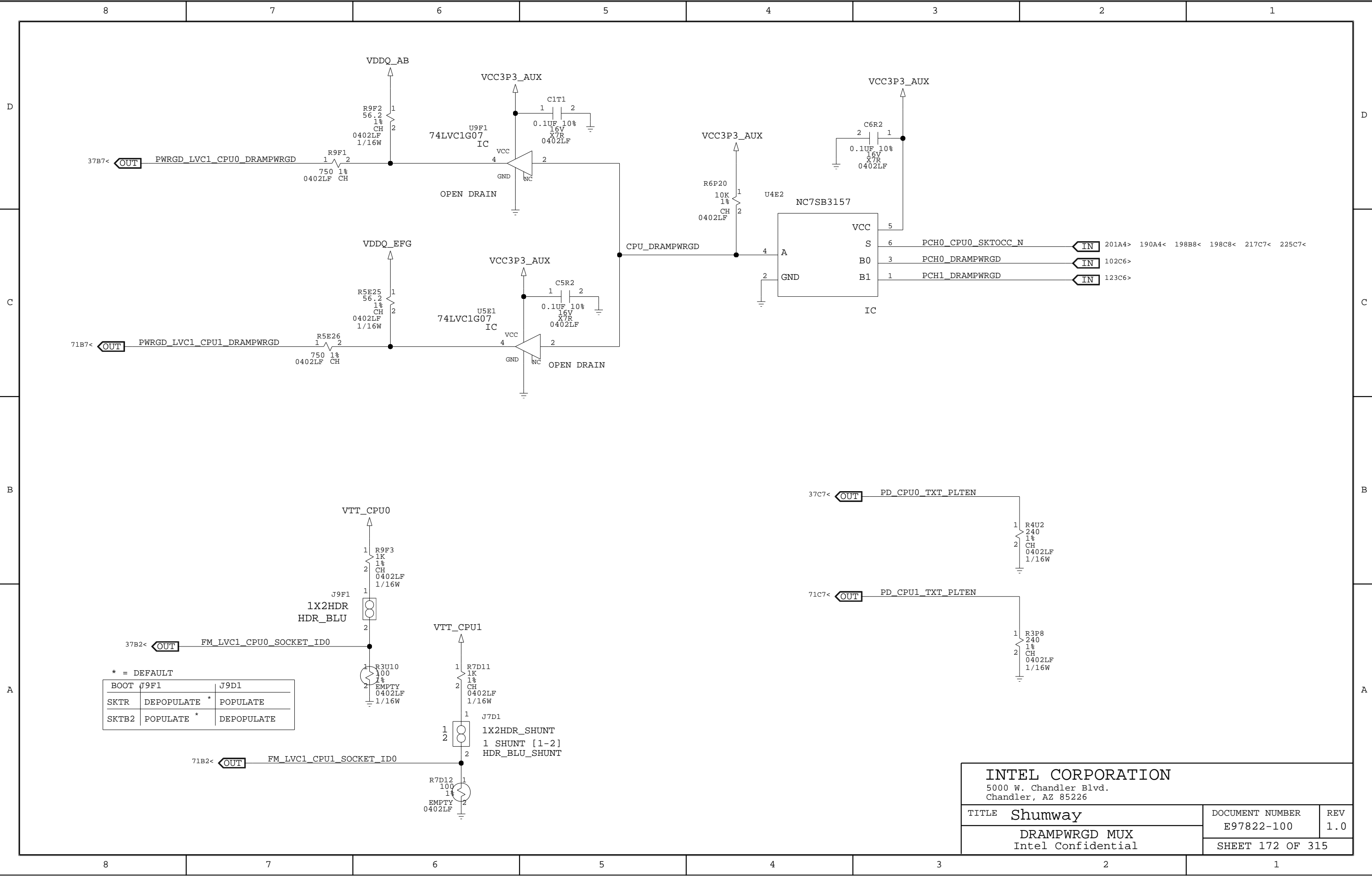
TITLE Shumway

PCH0&1: SATA 0-1  
Intel Confidential

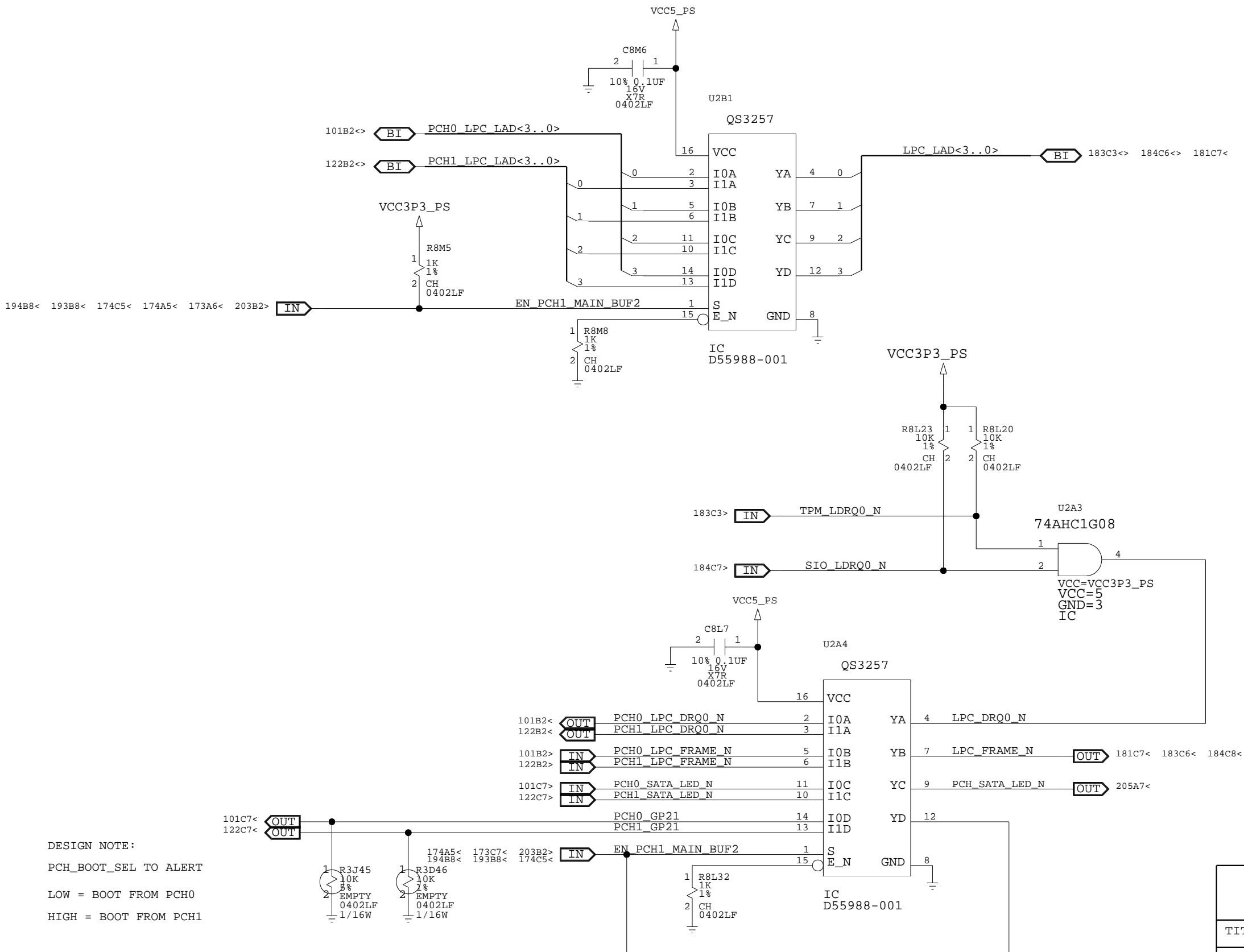
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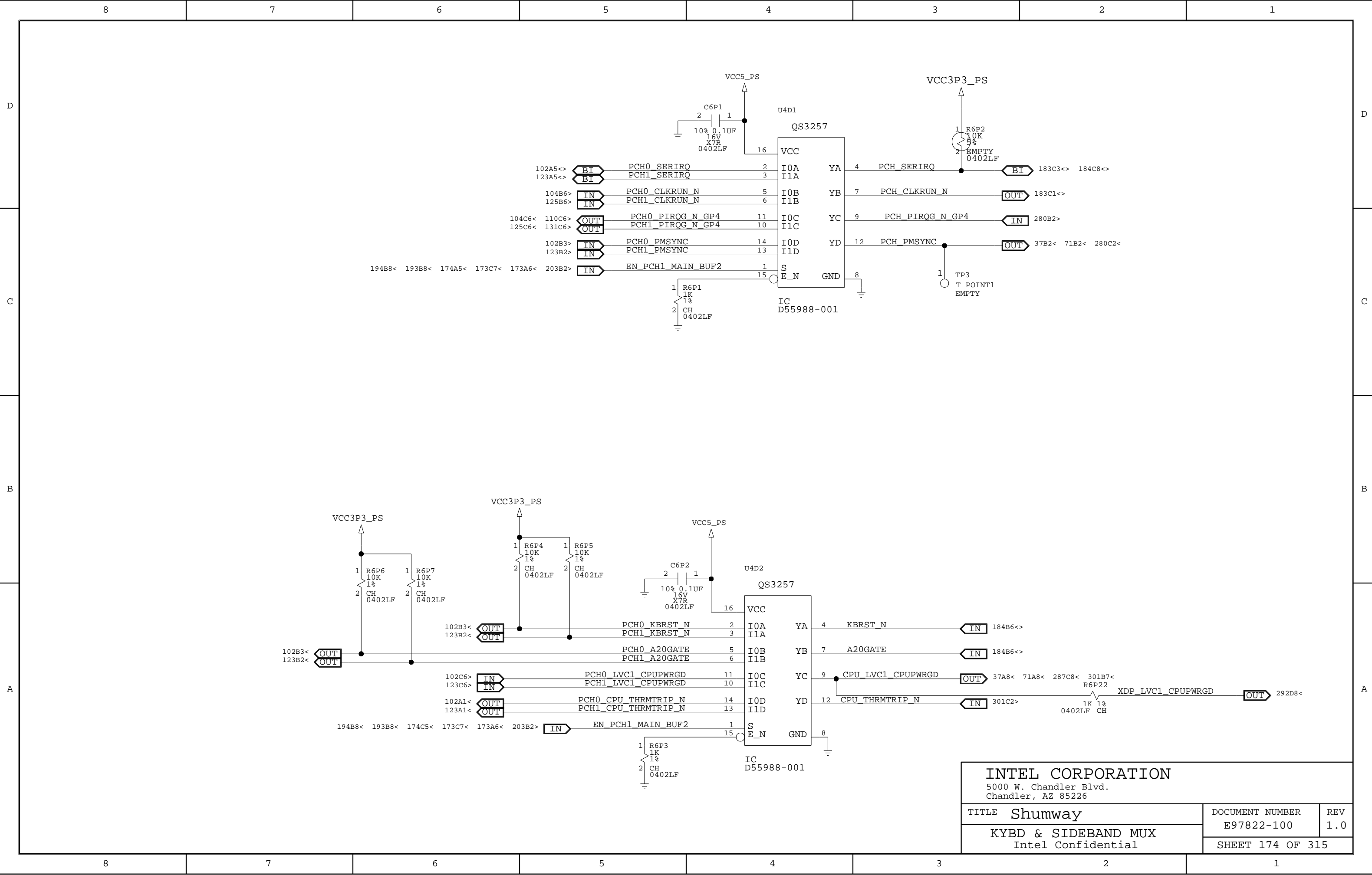
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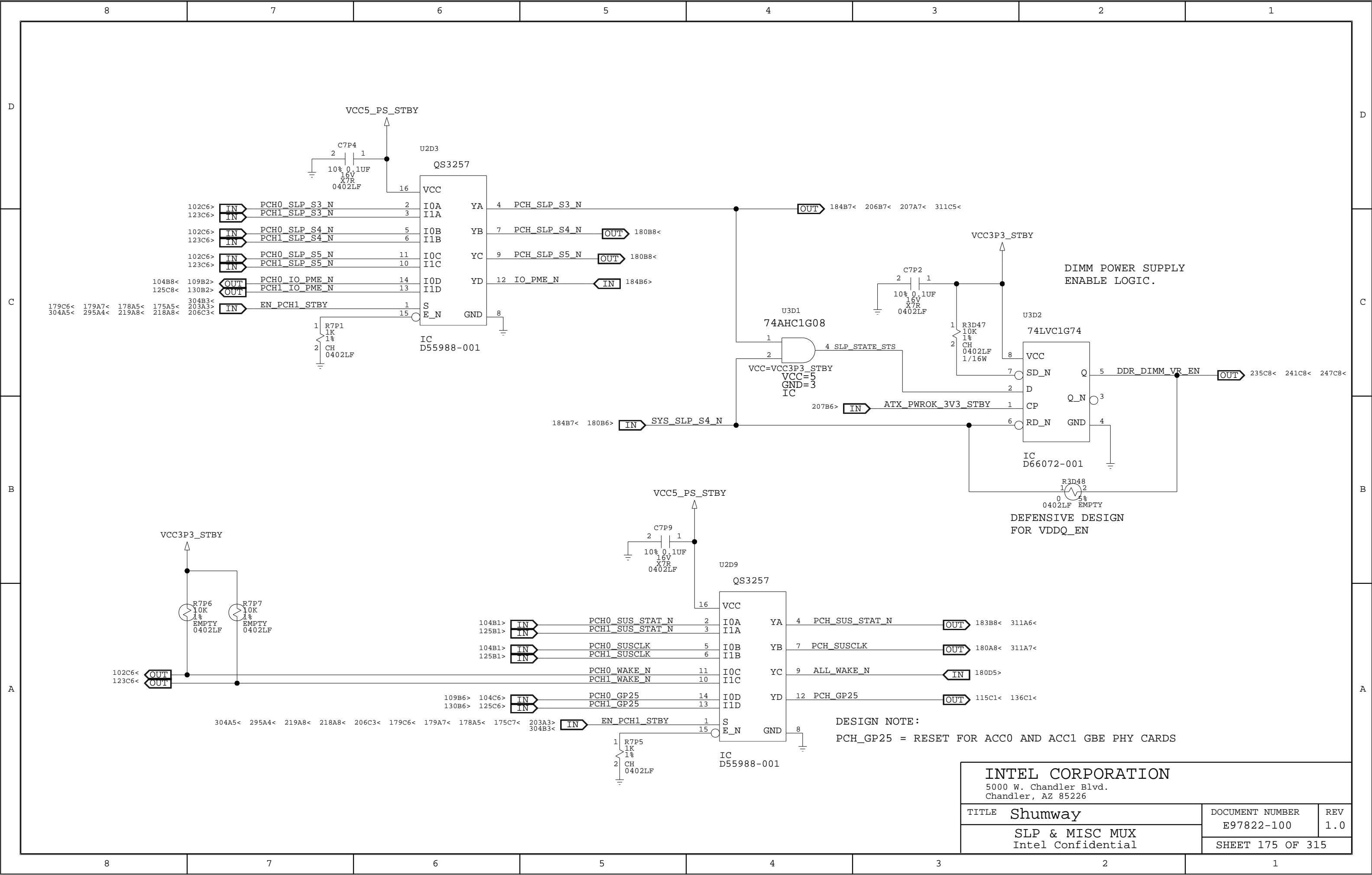


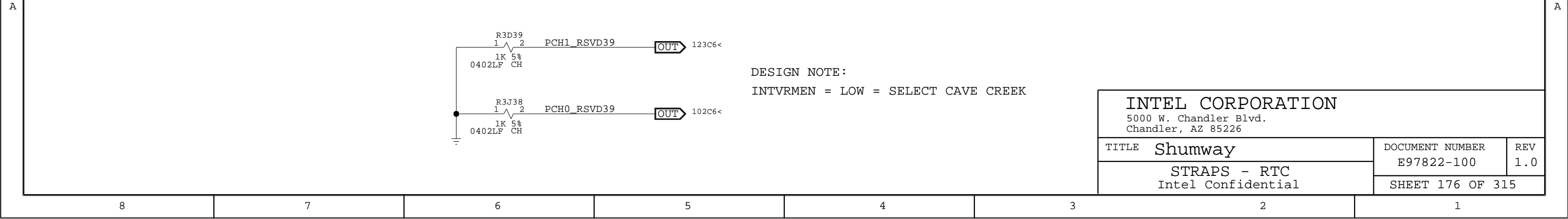
LPC SWITCH BETWEEN PCH0 AND PCH1

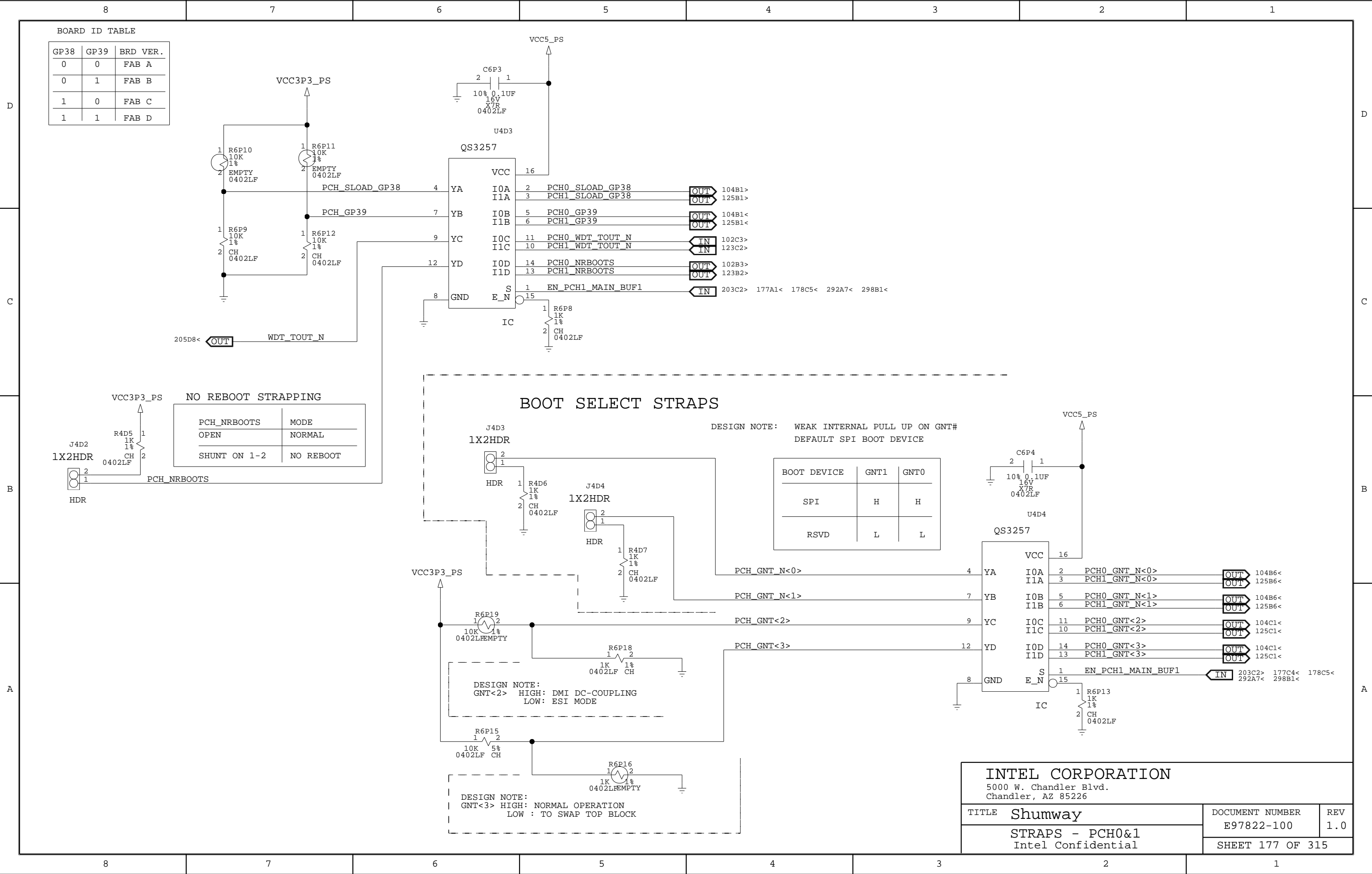


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	PCH0&1: LPC MUX Intel Confidential	E97822-100
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VCC5\_PS

2

C6P3

10%

0.1UF

16V

X7R

0402LF

1

U4D3

QS3257

16

VCC

2

PCH0\_SLOAD\_GP38

OUT

OUT

104B1>

125B1>

3

PCH1\_SLOAD\_GP38

OUT

OUT

104B1<

125B1<

5

PCH0\_GP39

OUT

OUT

104B1<

125B1<

6

PCH1\_GP39

OUT

OUT

104B1<

125B1<

11

PCH0\_WDT\_TOUT\_N

IN

IN

102C3>

123C2>

10

PCH1\_WDT\_TOUT\_N

IN

IN

102C3>

123C2>

14

PCH0\_NRBOOTS

OUT

OUT

102B3>

123B2>

13

PCH1\_NRBOOTS

OUT

OUT

102B3>

123B2>

1

EN\_PCH1\_MAIN\_BUF1

IN

IN

203C2>

177A1<

178C5<

292A7<

298B1<

15

E\_N

8

GND

1

R6P8

1K

1%

CH

0402LF

2

CH

0402LF

IC

S

E\_N

VCC3P3\_PS

1

R4D5

1K

1%

CH

0402LF

2

CH

0402LF

1

J4D2

1X2HDR

HDR

2

HDR

PCH\_NRBOOTS

NO REBOOT STRAPPING

PCH_NRBOOTS	MODE
OPEN	NORMAL
SHUNT ON 1-2	NO REBOOT

BOOT SELECT STRAPS

DESIGN NOTE: WEAK INTERNAL PULL UP ON GNT#  
DEFAULT SPI BOOT DEVICE

BOOT DEVICE	GNT1	GNT0
SPI	H	H
RSVD	L	L

VCC3P3\_PS

1

R6P19

10K

1%

EMPTY

0402LF

2

EMPTY

0402LF

1

R6P18

1K

1%

CH

0402LF

2

CH

0402LF

1

R6P15

10K

5%

CH

0402LF

2

CH

0402LF

1

R6P16

1K

1%

EMPTY

0402LF

2

EMPTY

0402LF

DESIGN NOTE:  
GNT<2> HIGH: DMI DC-COUPLING  
LOW: ESI MODE

DESIGN NOTE:  
GNT<3> HIGH: NORMAL OPERATION  
LOW : TO SWAP TOP BLOCK

VCC5\_PS

2

C6P4

10%

0.1UF

16V

X7R

0402LF

1

U4D4

QS3257

16

VCC

2

PCH0\_GNT\_N<0>

OUT

OUT

104B6<

125B6<

3

PCH1\_GNT\_N<0>

OUT

OUT

104B6<

125B6<

5

PCH0\_GNT\_N<1>

OUT

OUT

104B6<

125B6<

6

PCH1\_GNT\_N<1>

OUT

OUT

104B6<

125B6<

11

PCH0\_GNT<2>

OUT

OUT

104C1<

125C1<

10

PCH1\_GNT<2>

OUT

OUT

104C1<

125C1<

14

PCH0\_GNT<3>

OUT

OUT

104C1<

125C1<

13

PCH1\_GNT<3>

OUT

OUT

104C1<

125C1<

1

EN\_PCH1\_MAIN\_BUF1

IN

IN

203C2>

292A7<

177C4<

298B1<

178C5<

15

E\_N

8

GND

1

R6P13

1K

1%

CH

0402LF

2

CH

0402LF

IC

S

E\_N

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STRAPS - PCH0&1  
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Chandler, AZ 85226

TITLE Shumway

STRAPS - PCH0&1  
Intel Confidential

DOCUMENT NUMBER

E97822-100

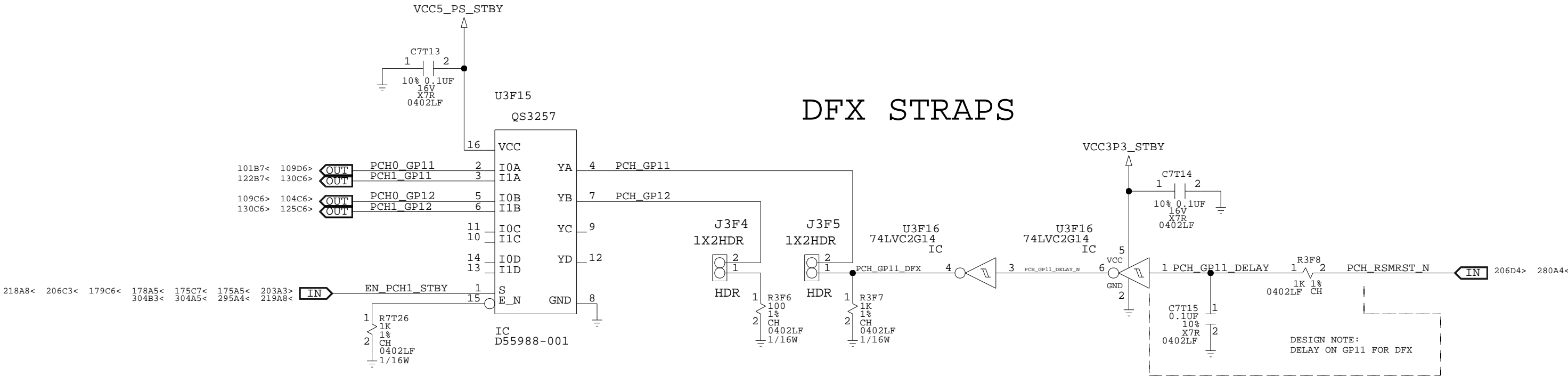
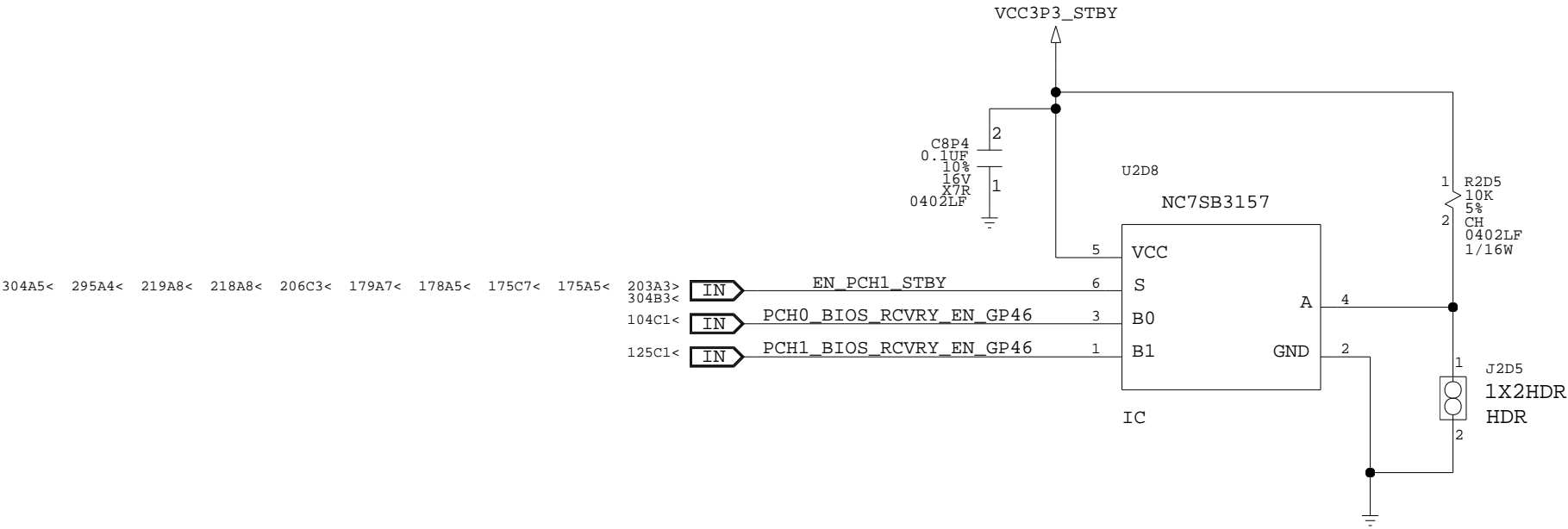
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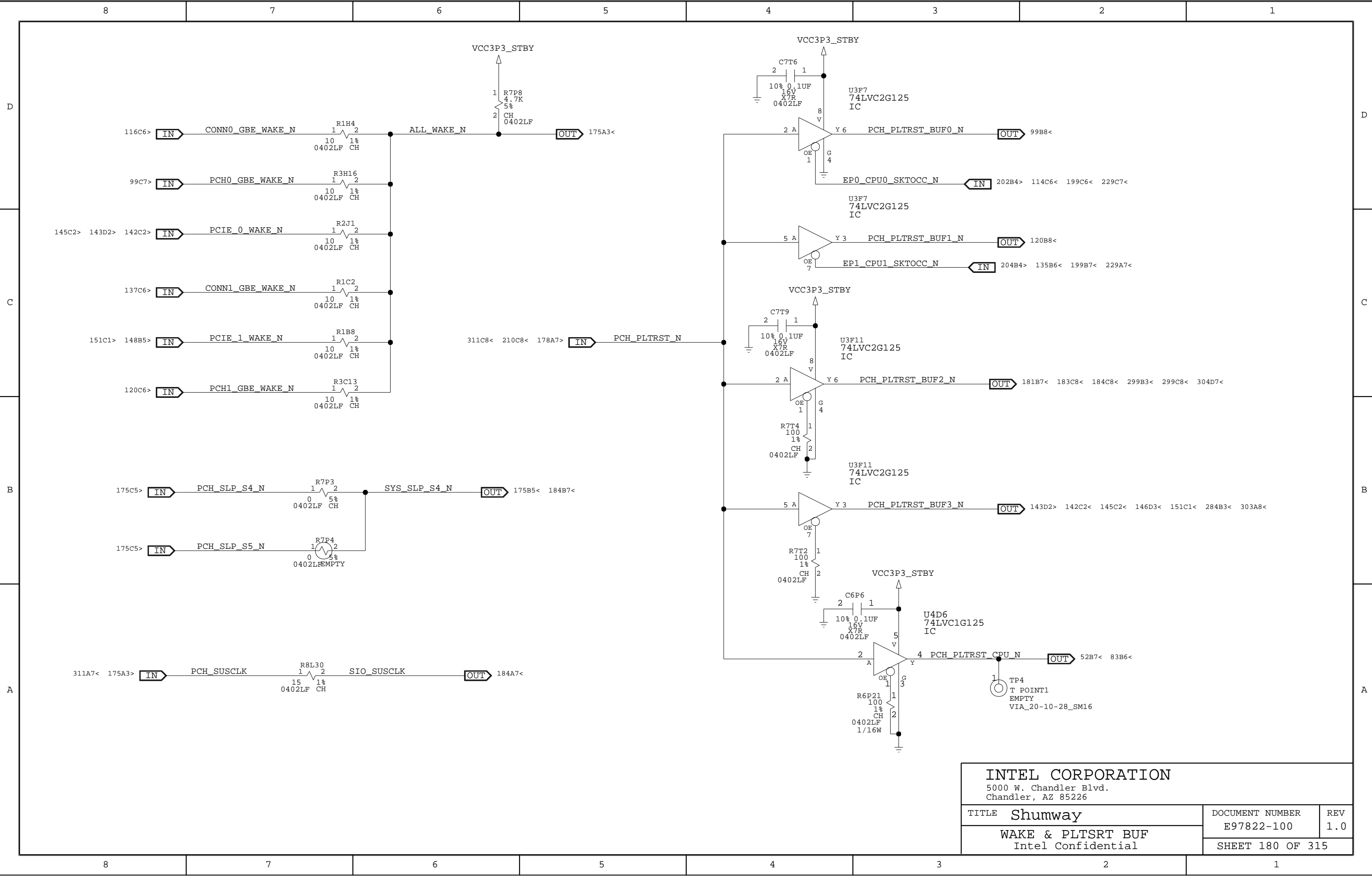


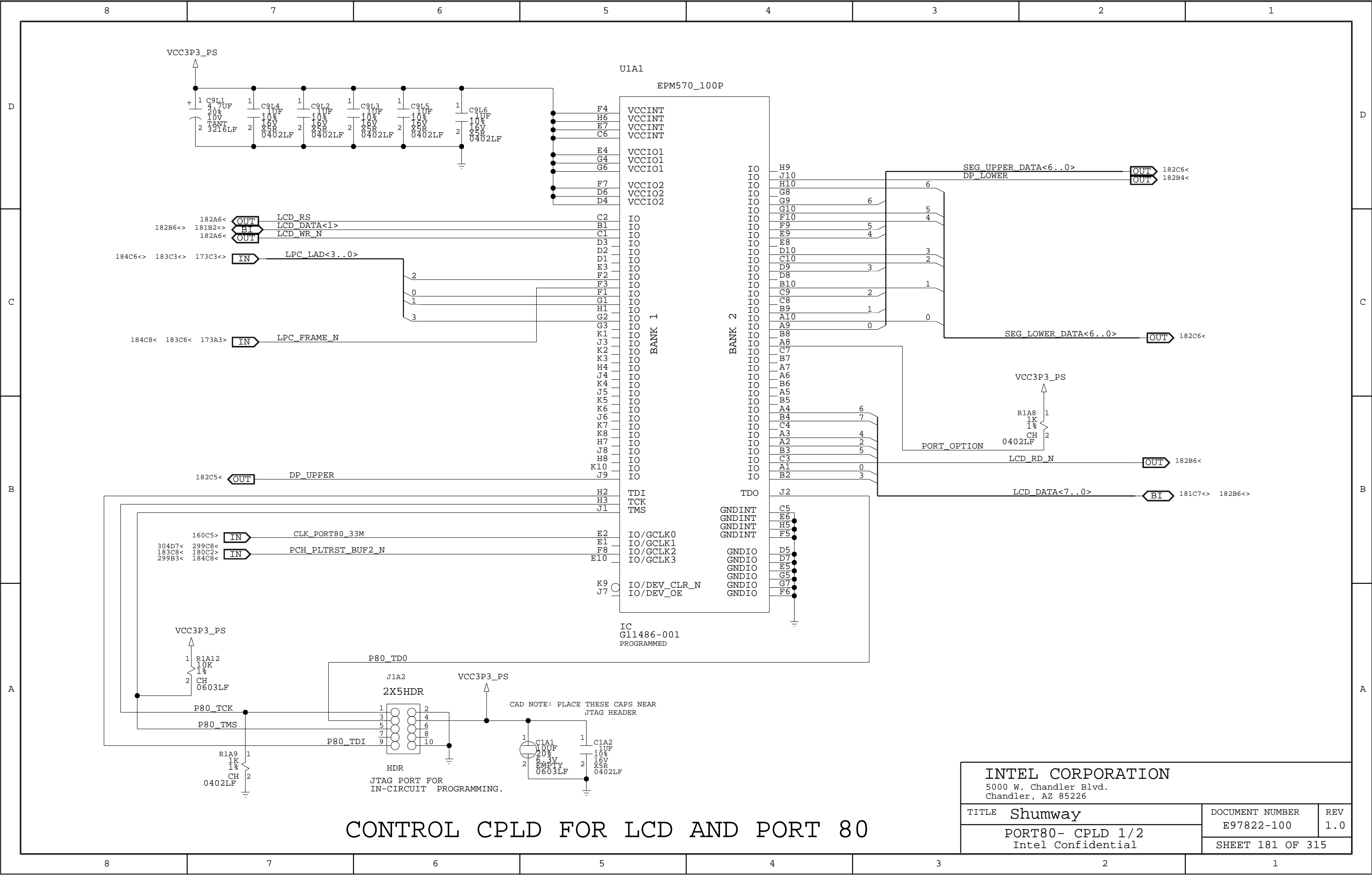


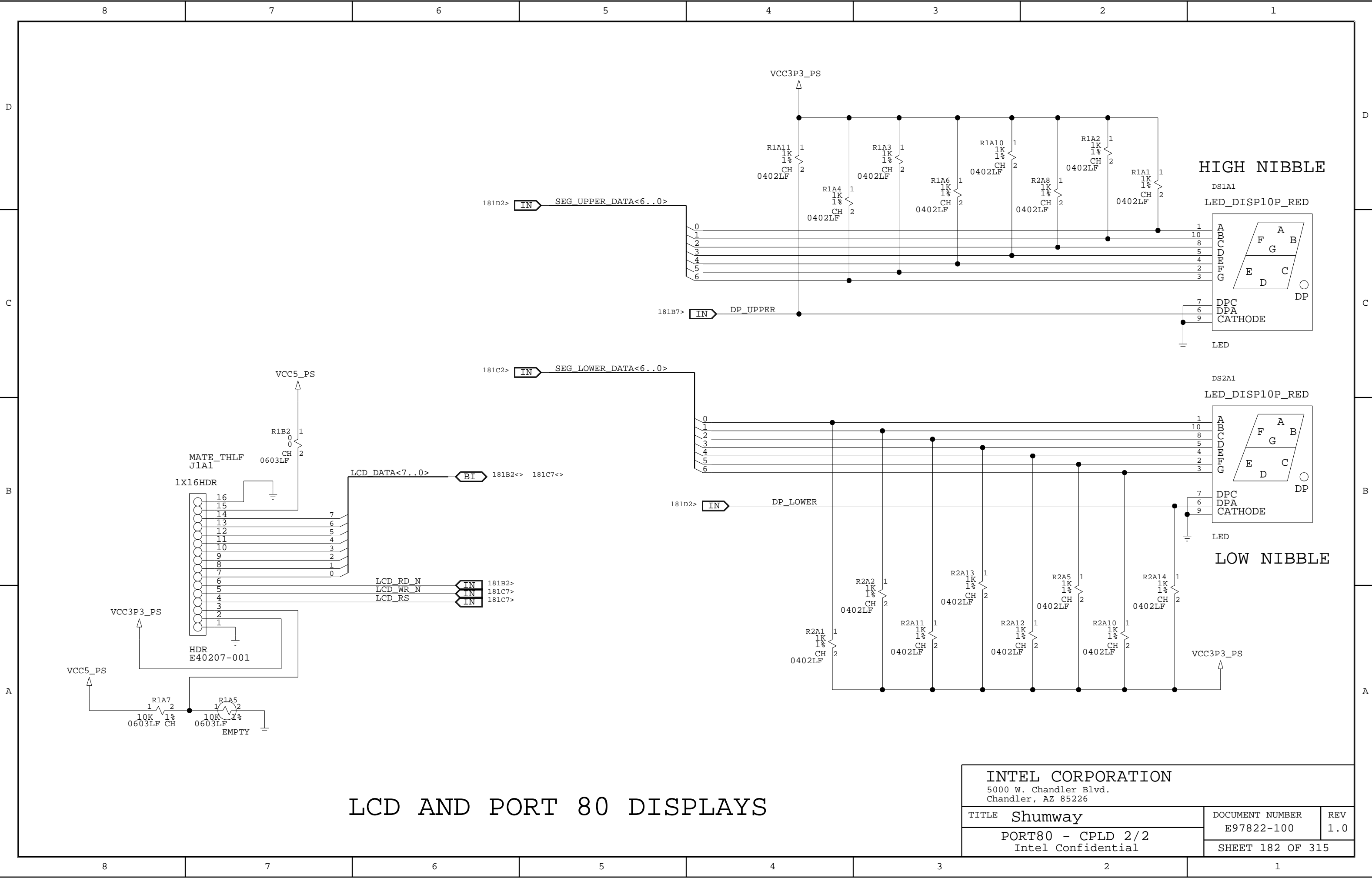
DFX SELECT	J3F5 (GP11)	J3F4 (GP12)
DFX TEST	1-2	1-2
NORMAL*	OPEN	OPEN

\* DEFAULT

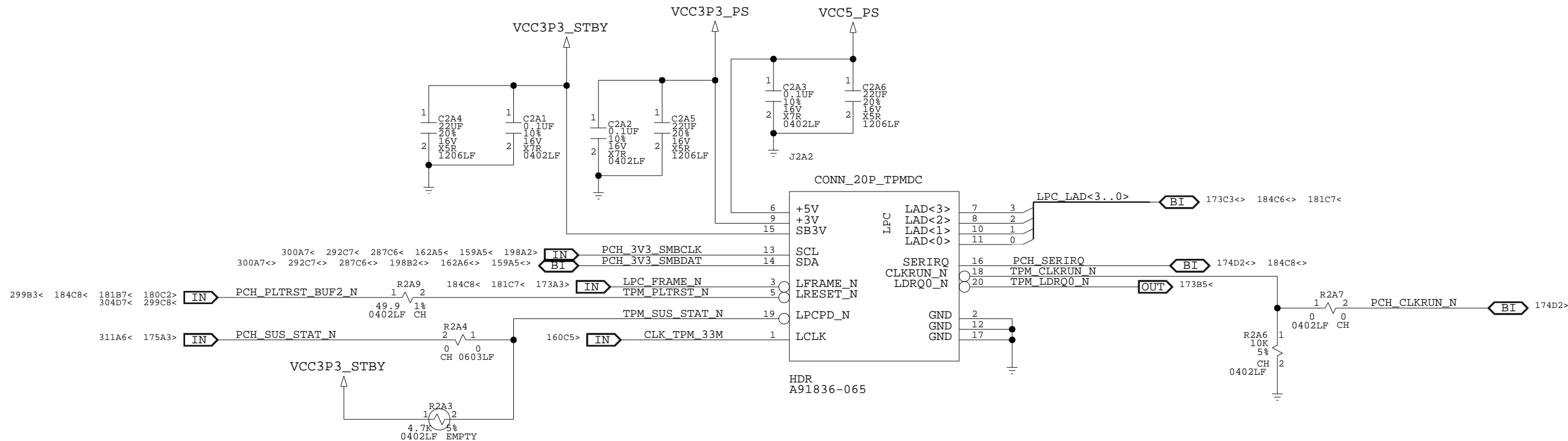
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TITLE Shumway

TPM CONN.  
Intel Confidential

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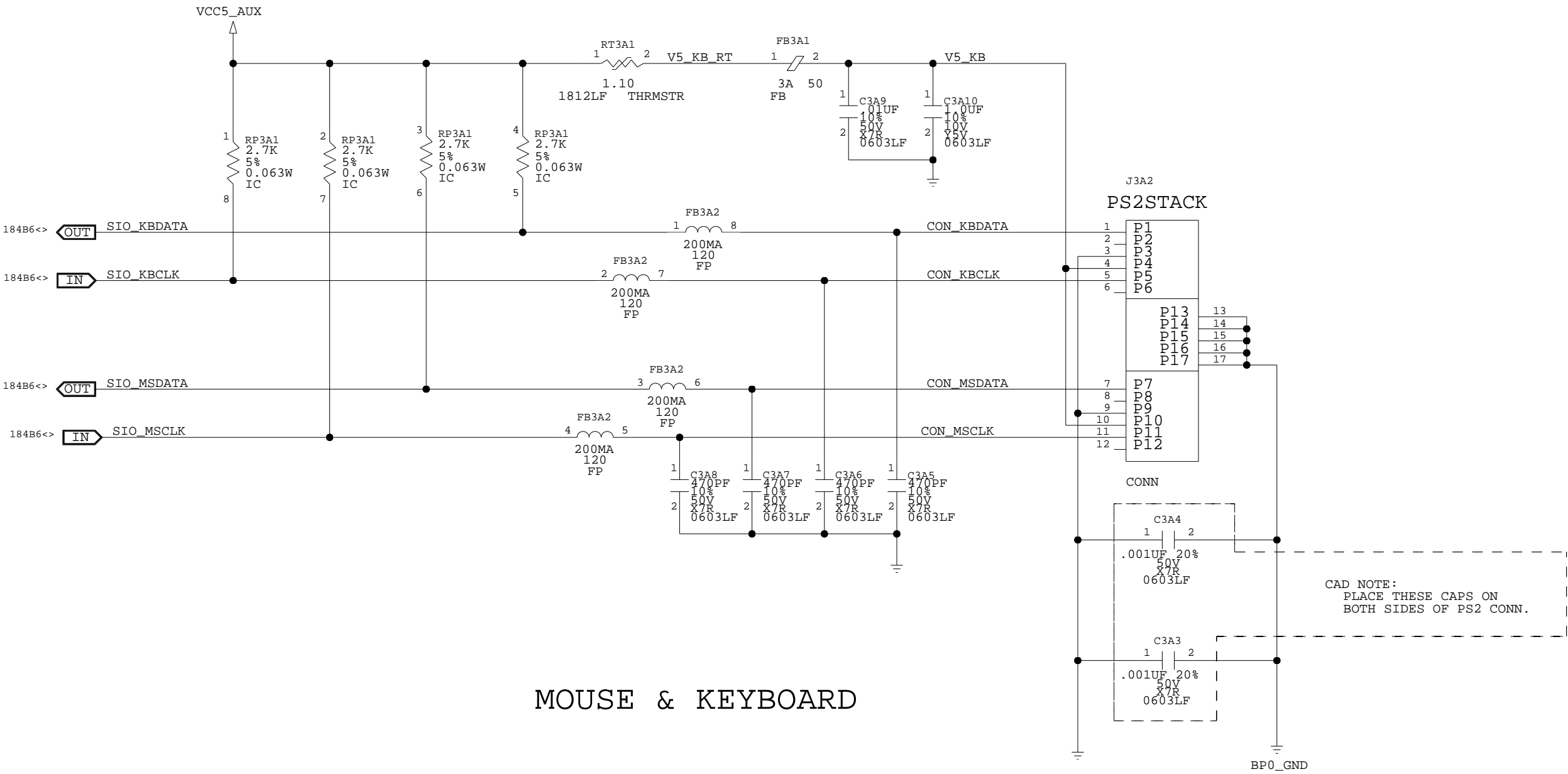
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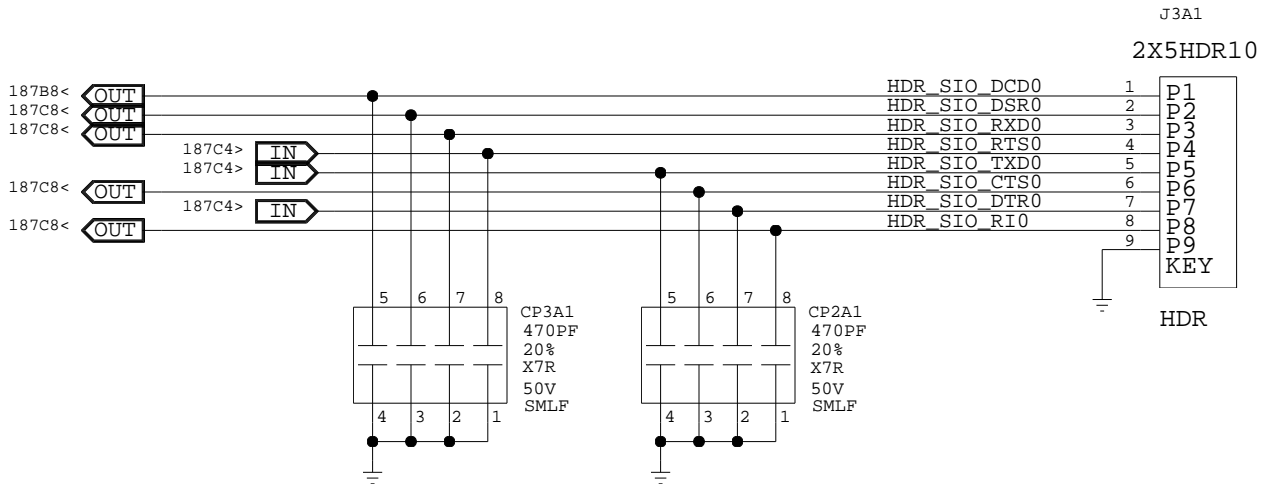
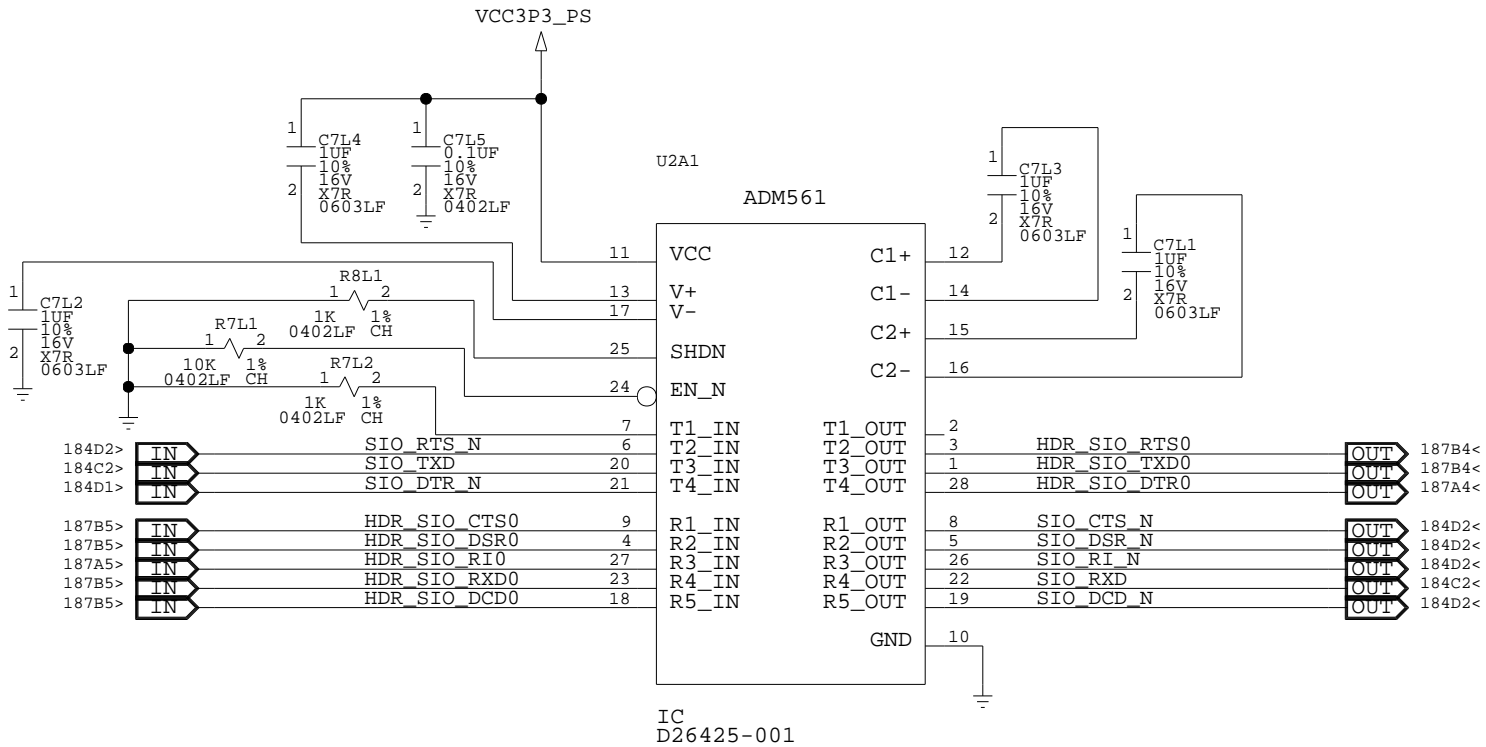
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MOUSE & KEYBOARD

INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
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# SPI CIRCUITS AND FLASH PROGRAMMER HEADERS

INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

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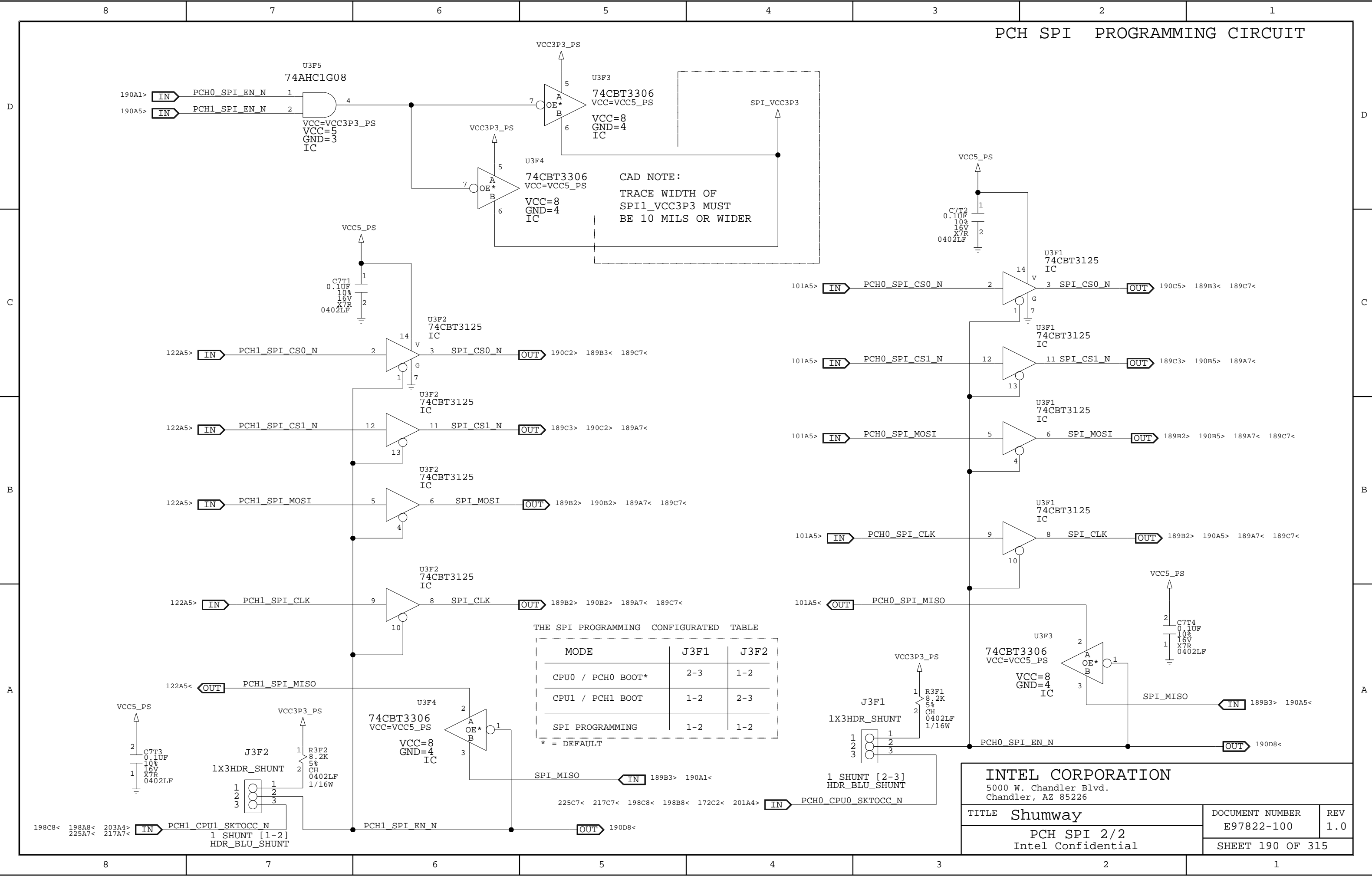
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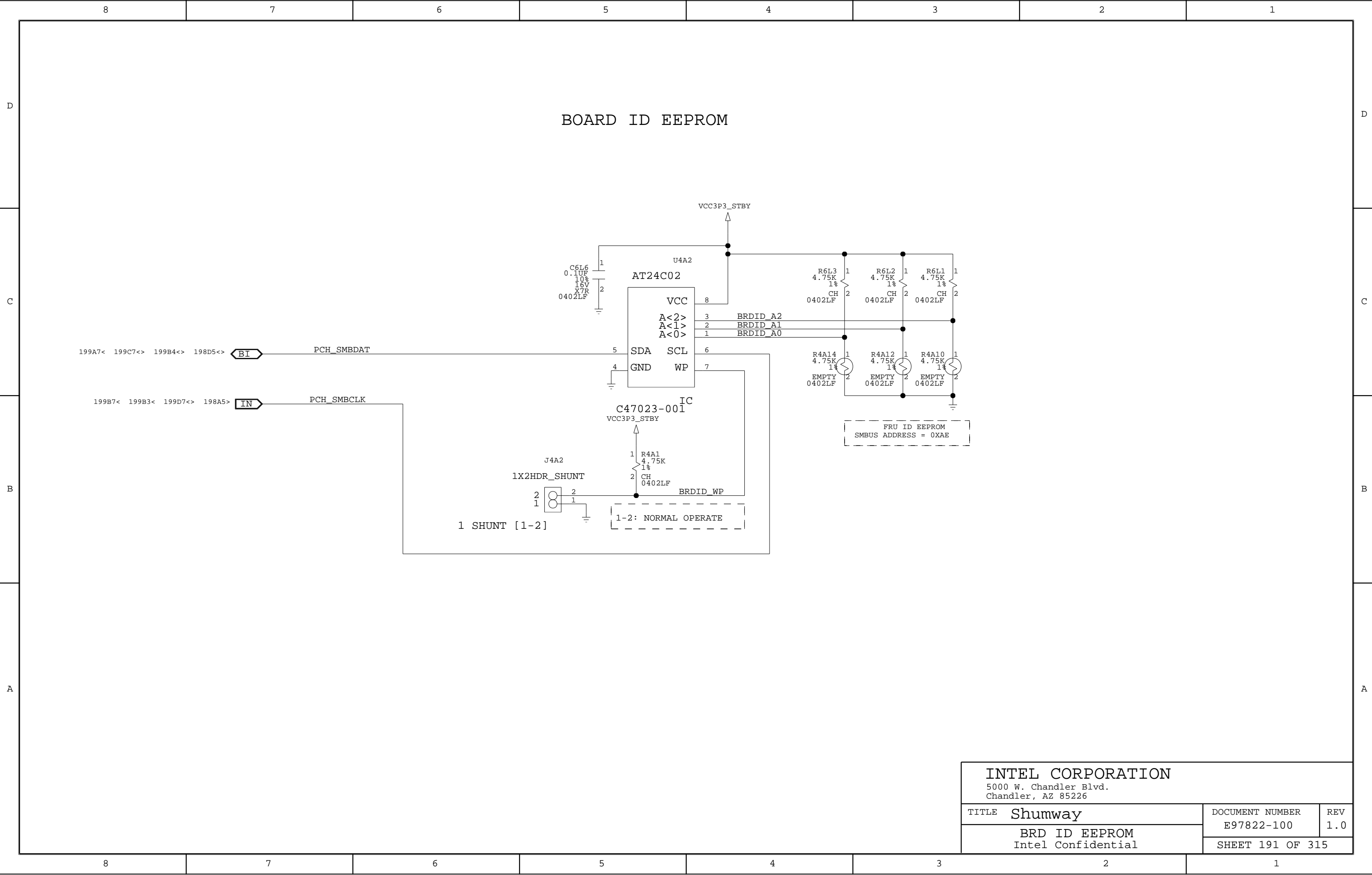
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SERIAL PORTS  
FROM PCH0 AND PCH1

INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

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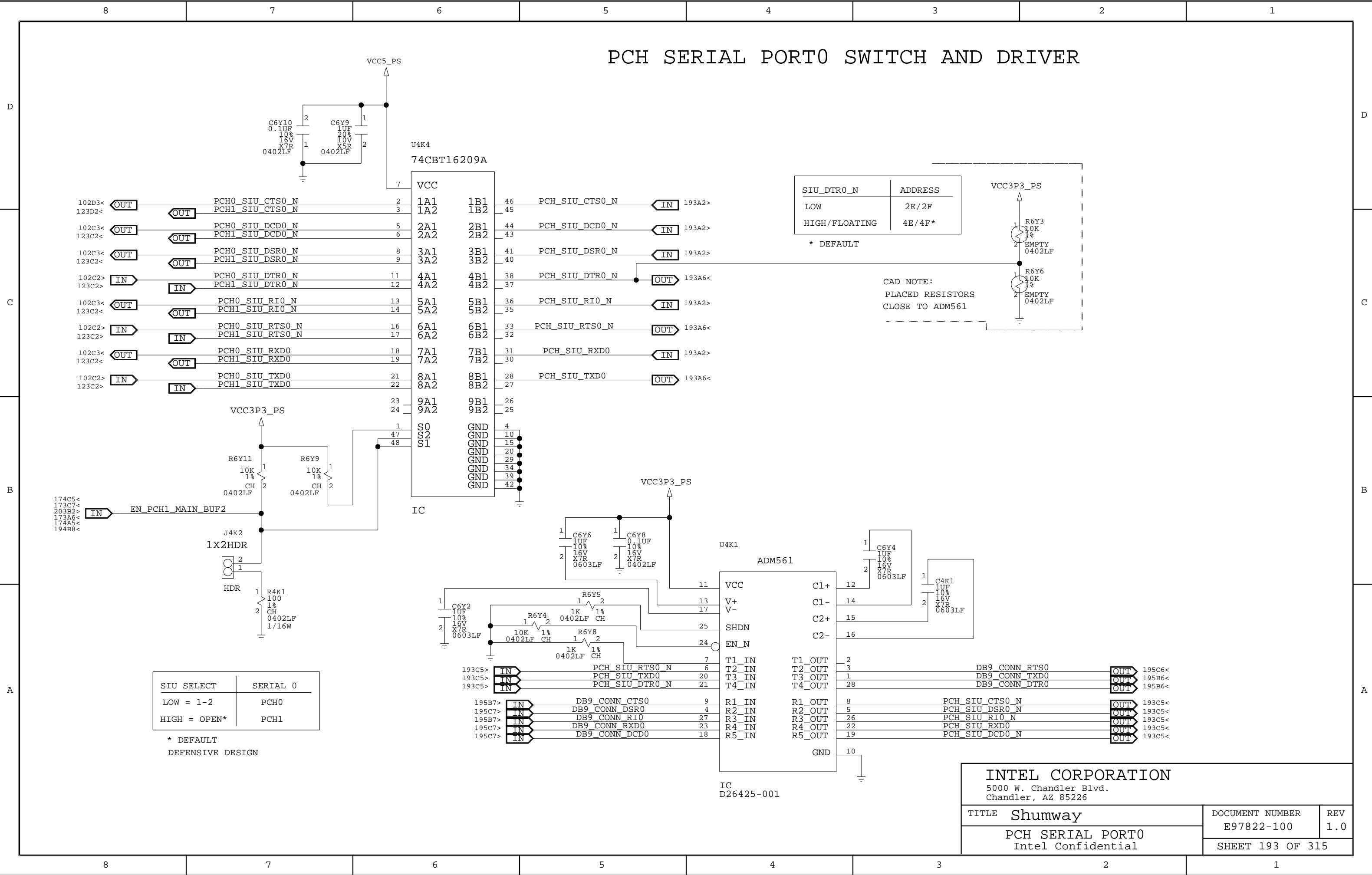
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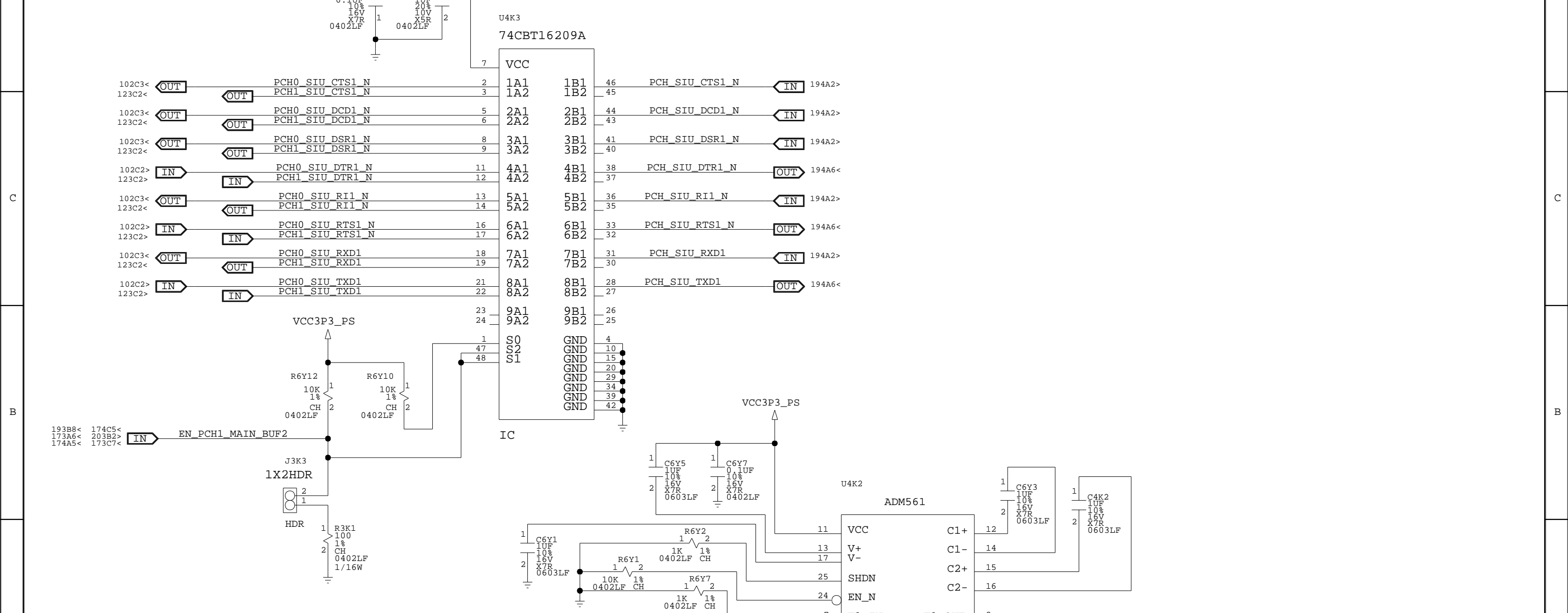
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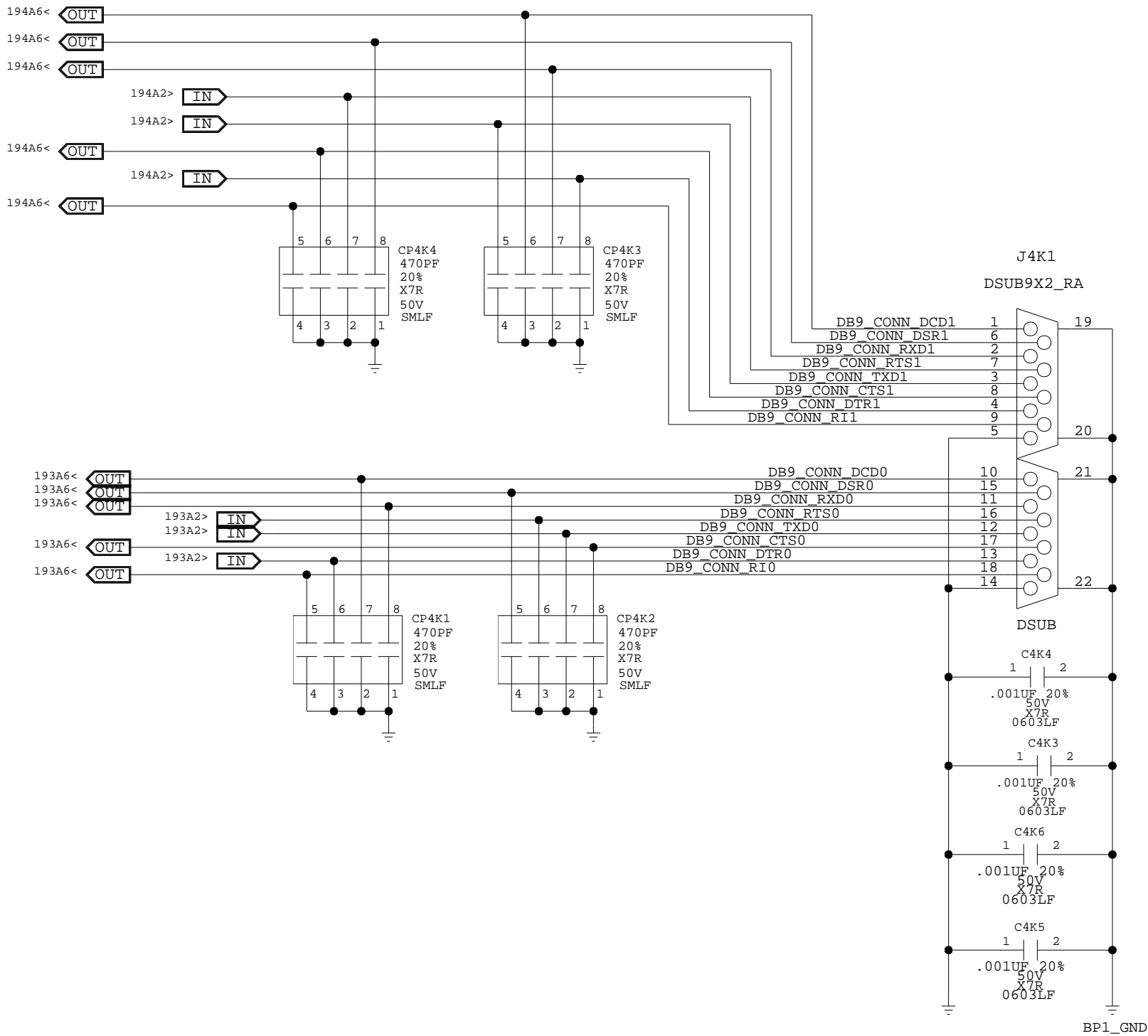
A	<table><tr><td>SIU SELECT</td><td>SERIAL 1</td></tr><tr><td>LOW = 1-2</td><td>PCH0</td></tr><tr><td>HIGH = OPEN*</td><td>PCH1</td></tr></table>		SIU SELECT	SERIAL 1	LOW = 1-2	PCH0	HIGH = OPEN*	PCH1	<table><tr><td>194C4&gt;</td><td></td><td>PCH_SIU_RIS1_N</td><td>6</td><td>T2_IN</td><td>T2_OUT</td><td>3</td><td>DB9_CONN_RIS1</td><td></td><td>195D7&lt;</td></tr><tr><td>194C4&gt;</td><td></td><td>PCH_SIU_TXD1</td><td>20</td><td>T3_IN</td><td>T3_OUT</td><td>1</td><td>DB9_CONN_TXD1</td><td></td><td>195D7&lt;</td></tr><tr><td>194C4&gt;</td><td></td><td>PCH_SIU_DTR1_N</td><td>21</td><td>T4_IN</td><td>T4_OUT</td><td>28</td><td>DB9_CONN_DTR1</td><td></td><td>195D7&lt;</td></tr></table>	194C4>		PCH_SIU_RIS1_N	6	T2_IN	T2_OUT	3	DB9_CONN_RIS1		195D7<	194C4>		PCH_SIU_TXD1	20	T3_IN	T3_OUT	1	DB9_CONN_TXD1		195D7<	194C4>		PCH_SIU_DTR1_N	21	T4_IN	T4_OUT	28	DB9_CONN_DTR1		195D7<															
	SIU SELECT	SERIAL 1																																																				
	LOW = 1-2	PCH0																																																				
	HIGH = OPEN*	PCH1																																																				
	194C4>		PCH_SIU_RIS1_N	6	T2_IN	T2_OUT	3	DB9_CONN_RIS1		195D7<																																												
	194C4>		PCH_SIU_TXD1	20	T3_IN	T3_OUT	1	DB9_CONN_TXD1		195D7<																																												
	194C4>		PCH_SIU_DTR1_N	21	T4_IN	T4_OUT	28	DB9_CONN_DTR1		195D7<																																												
			<table><tr><td>195D7&gt;</td><td></td><td>DB9_CONN_CTS1</td><td>9</td><td>R1_IN</td><td>R1_OUT</td><td>8</td><td>PCH_SIU_CTS1_N</td><td></td><td>194C4&lt;</td></tr><tr><td>195D7&gt;</td><td></td><td>DB9_CONN_DSR1</td><td>4</td><td>R2_IN</td><td>R2_OUT</td><td>5</td><td>PCH_SIU_DSR1_N</td><td></td><td>194C4&lt;</td></tr><tr><td>195D7&gt;</td><td></td><td>DB9_CONN_R11</td><td>27</td><td>R3_IN</td><td>R3_OUT</td><td>26</td><td>PCH_SIU_R11_N</td><td></td><td>194C4&lt;</td></tr><tr><td>195D7&gt;</td><td></td><td>DB9_CONN_RXD1</td><td>23</td><td>R4_IN</td><td>R4_OUT</td><td>22</td><td>PCH_SIU_RXD1</td><td></td><td>194C4&lt;</td></tr><tr><td>195D7&gt;</td><td></td><td>DB9_CONN_DCD1</td><td>18</td><td>R5_IN</td><td>R5_OUT</td><td>19</td><td>PCH_SIU_DCD1_N</td><td></td><td>194C4&lt;</td></tr></table>	195D7>		DB9_CONN_CTS1	9	R1_IN	R1_OUT	8	PCH_SIU_CTS1_N		194C4<	195D7>		DB9_CONN_DSR1	4	R2_IN	R2_OUT	5	PCH_SIU_DSR1_N		194C4<	195D7>		DB9_CONN_R11	27	R3_IN	R3_OUT	26	PCH_SIU_R11_N		194C4<	195D7>		DB9_CONN_RXD1	23	R4_IN	R4_OUT	22	PCH_SIU_RXD1		194C4<	195D7>		DB9_CONN_DCD1	18	R5_IN	R5_OUT	19	PCH_SIU_DCD1_N		194C4<	
	195D7>		DB9_CONN_CTS1	9	R1_IN	R1_OUT	8	PCH_SIU_CTS1_N		194C4<																																												
	195D7>		DB9_CONN_DSR1	4	R2_IN	R2_OUT	5	PCH_SIU_DSR1_N		194C4<																																												
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195D7>		DB9_CONN_RXD1	23	R4_IN	R4_OUT	22	PCH_SIU_RXD1		194C4<																																													
195D7>		DB9_CONN_DCD1	18	R5_IN	R5_OUT	19	PCH_SIU_DCD1_N		194C4<																																													
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DEFENSIVE DESIGN																																																						

INTEL CORPORATION  
5000 N. Channel Blvd.

5000 W. Chandler Blvd.  
Chandler, AZ 85226

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PCH SERIAL PORT CONNECTOR

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PCH SERIAL PORT CONN. Intel Confidential	SHEET 195 OF 315	

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INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE	Shumway
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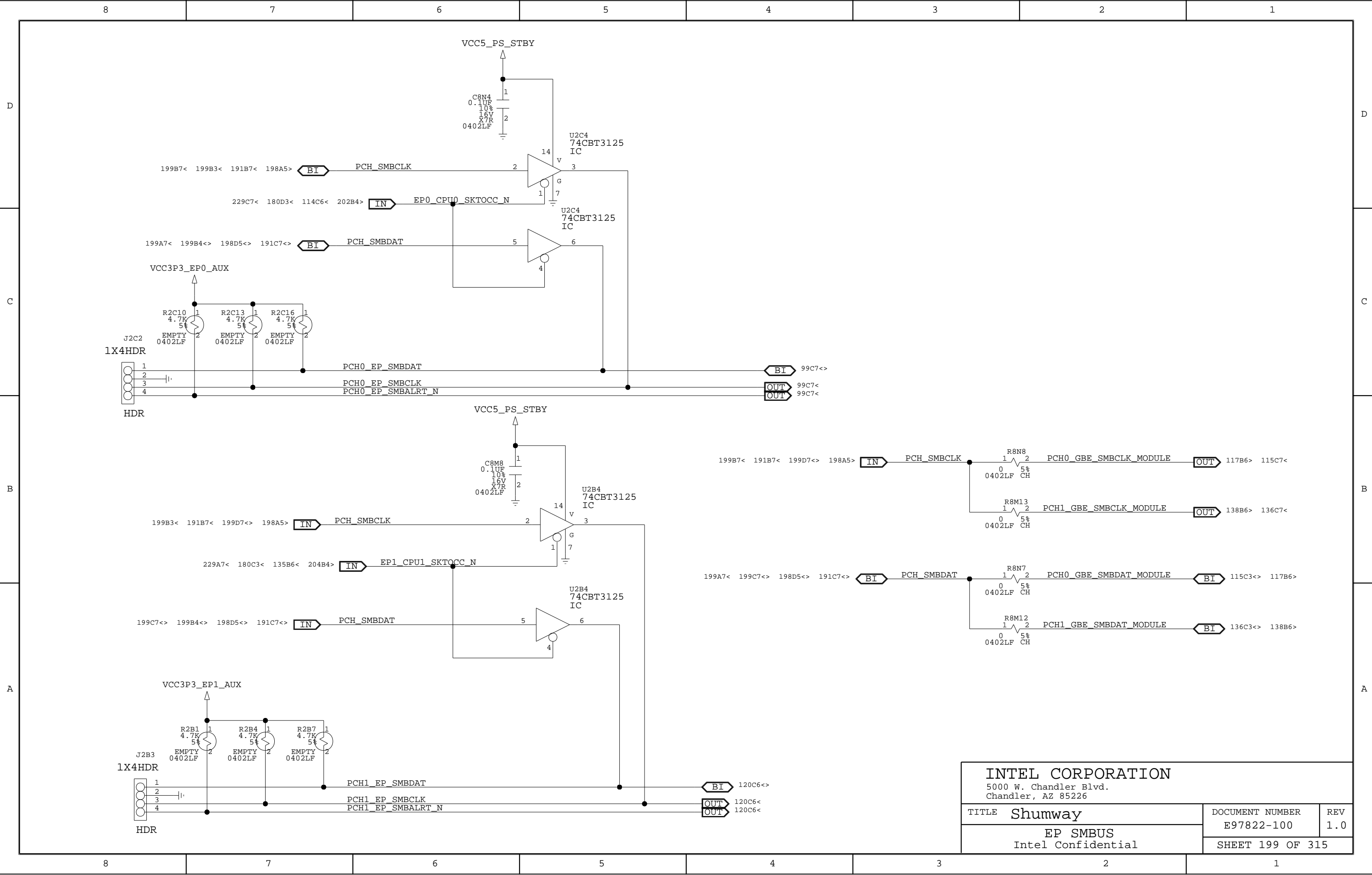
DOCUMENT NUMBER  
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# GLUE LOGICS TO SELECT PCH0 AND PCH1

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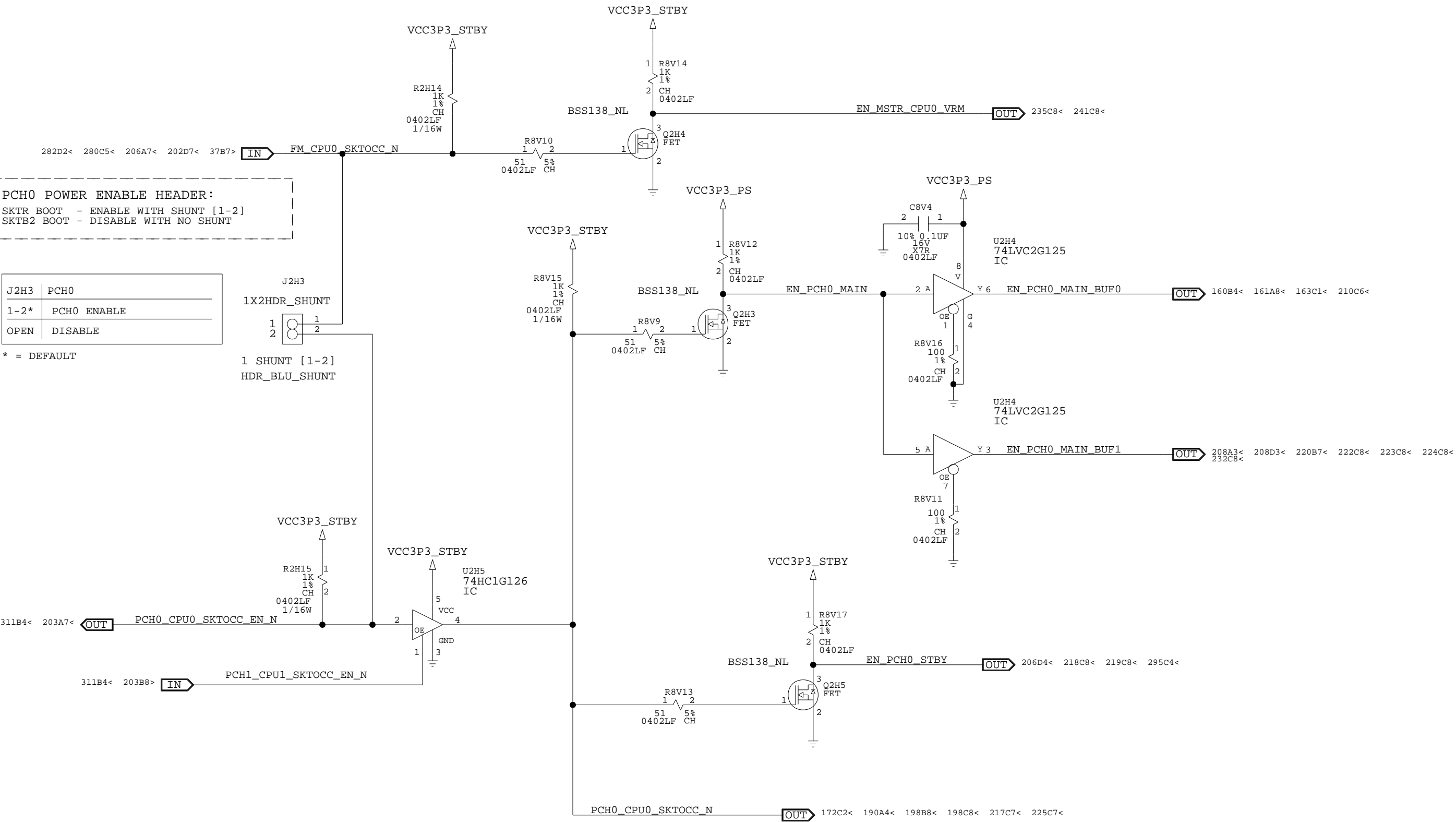
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PCH0 POWER ENABLE HEADER:  
SKTR BOOT - ENABLE WITH SHUNT [1-2]  
SKTB2 BOOT - DISABLE WITH NO SHUNT

J2H3	PCH0
1-2*	PCH0 ENABLE
OPEN	DISABLE

\* = DEFAULT

J2H3  
1X2HDR\_SHUNT  
1 2  
1 SHUNT [1-2]  
HDR\_BLU\_SHUNT



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BRD CONFIG 1/4 Intel Confidential		SHEET 201 OF 315			

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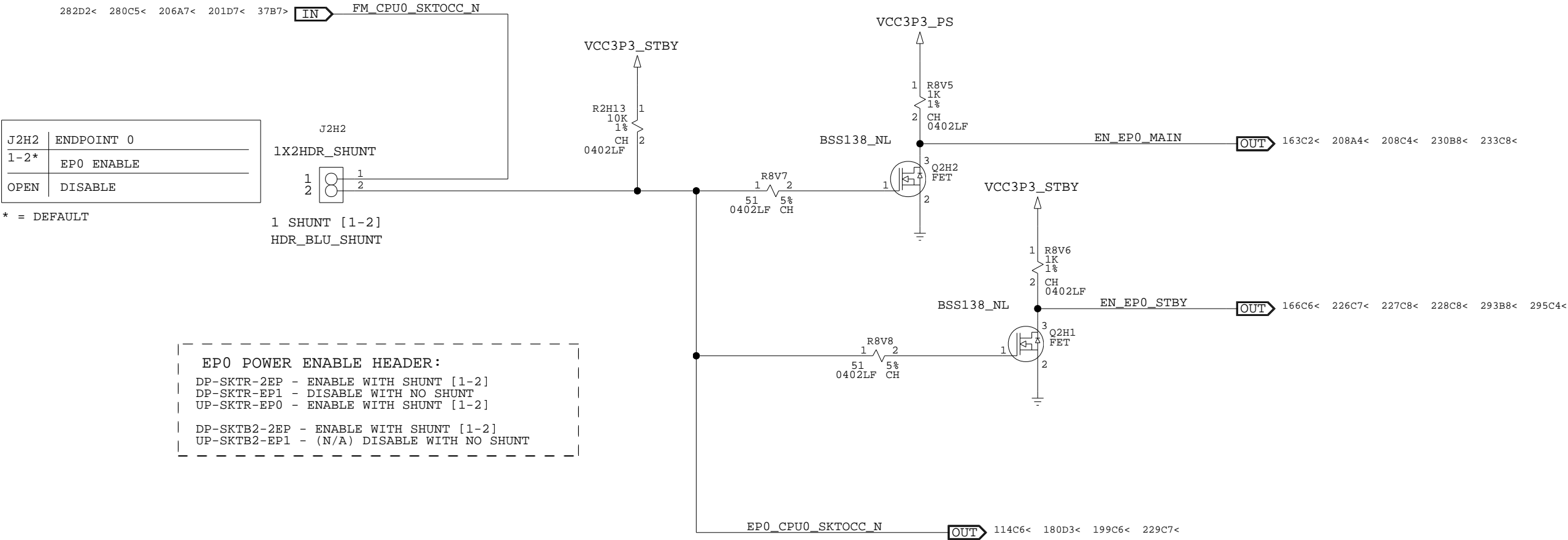
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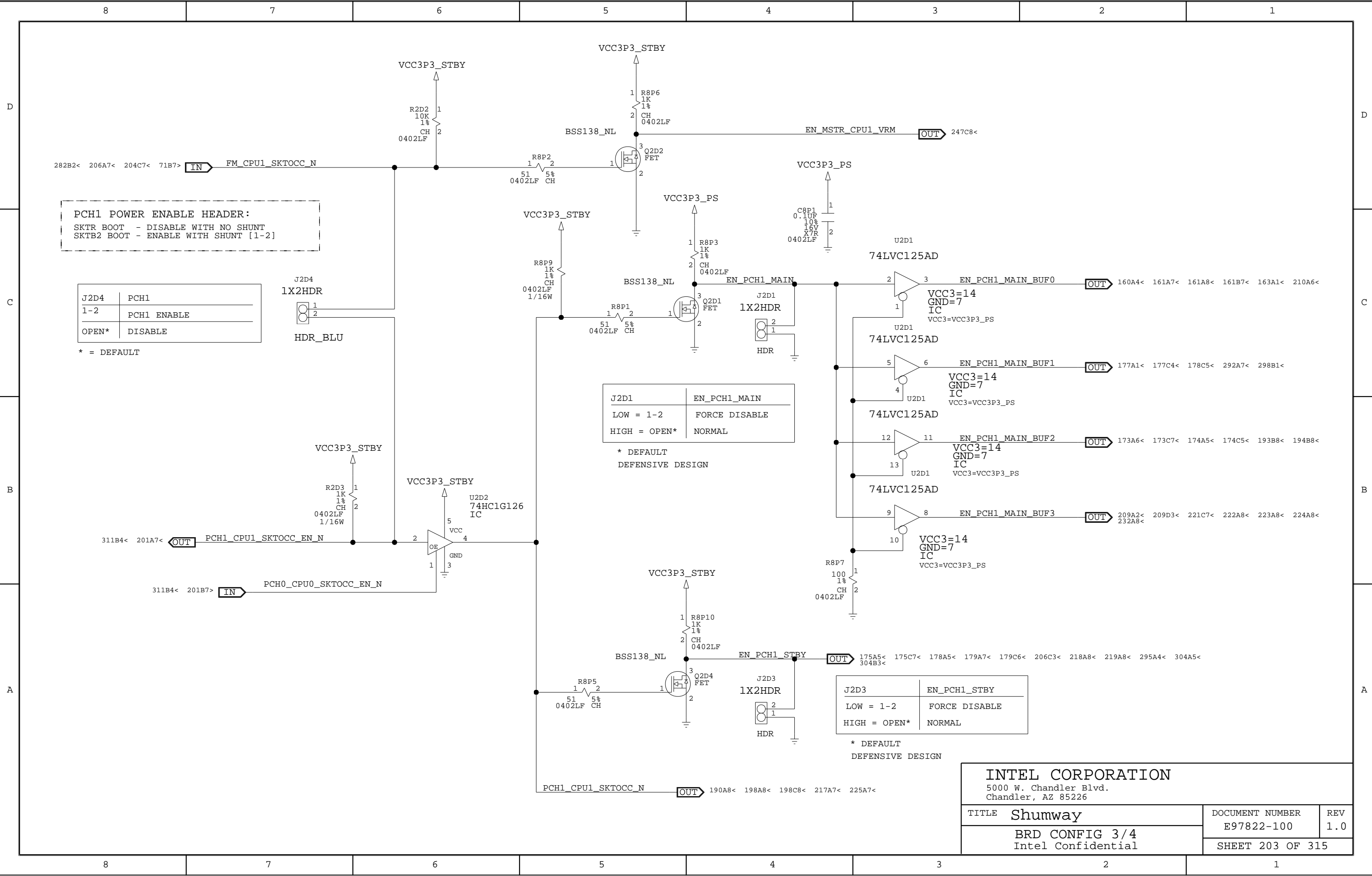
INTEL CORPORATION

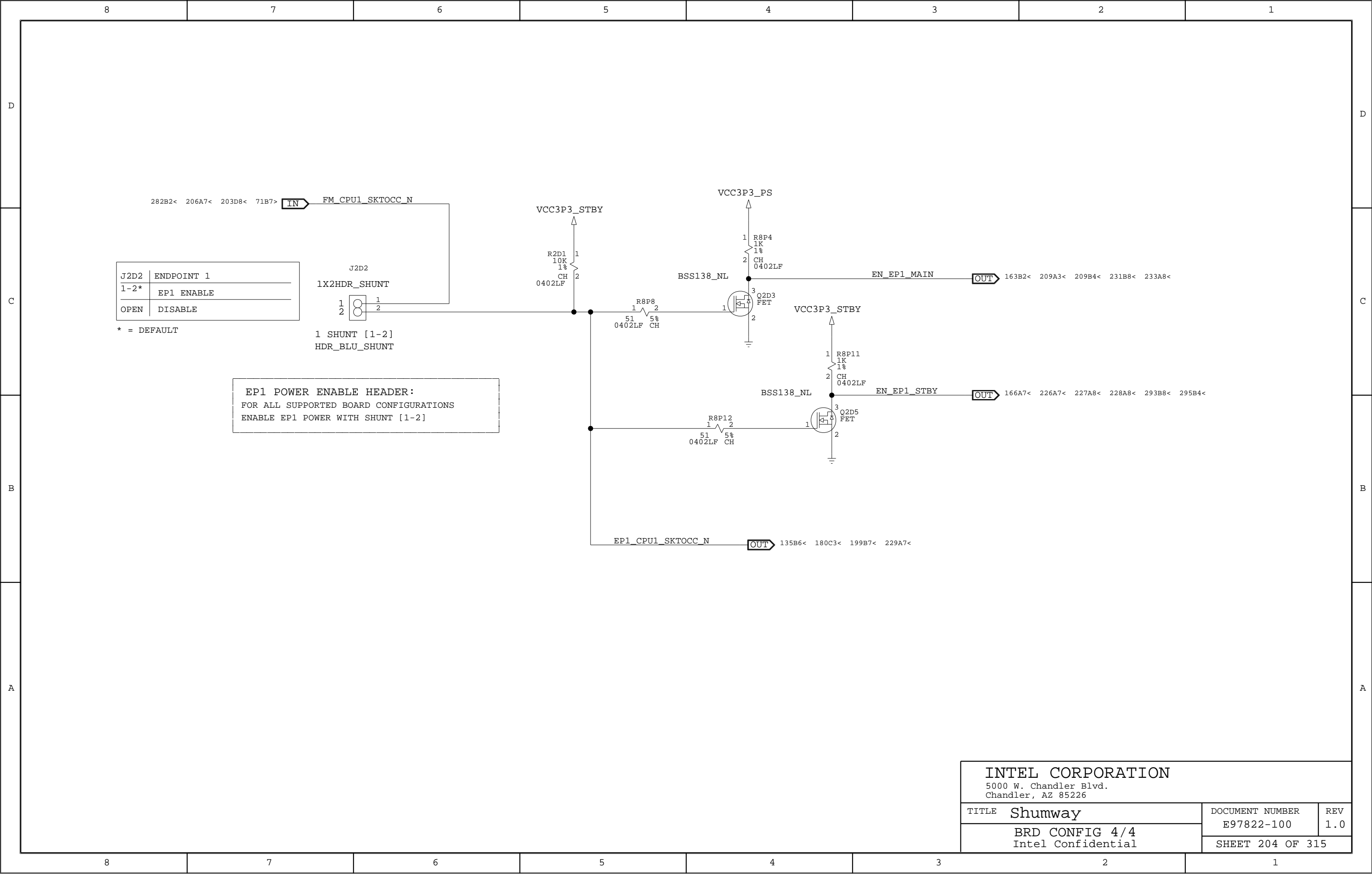
5000 W. Chandler Blvd.  
Chandler, AZ 85226

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	BRD CONFIG 2/4 Intel Confidential	E97822-100	1.0
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5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

BRD CONFIG 4/4  
Intel Confidential

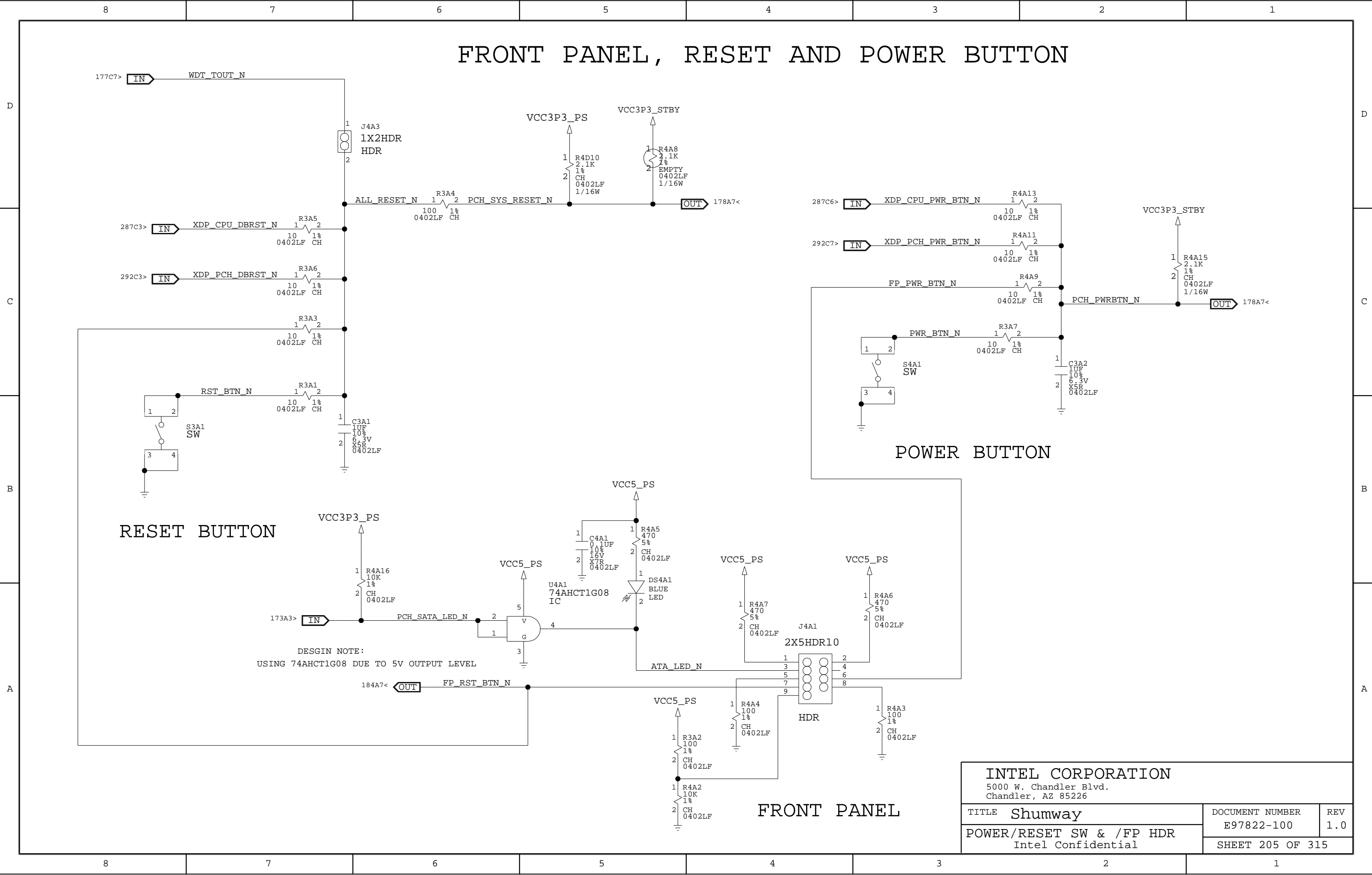
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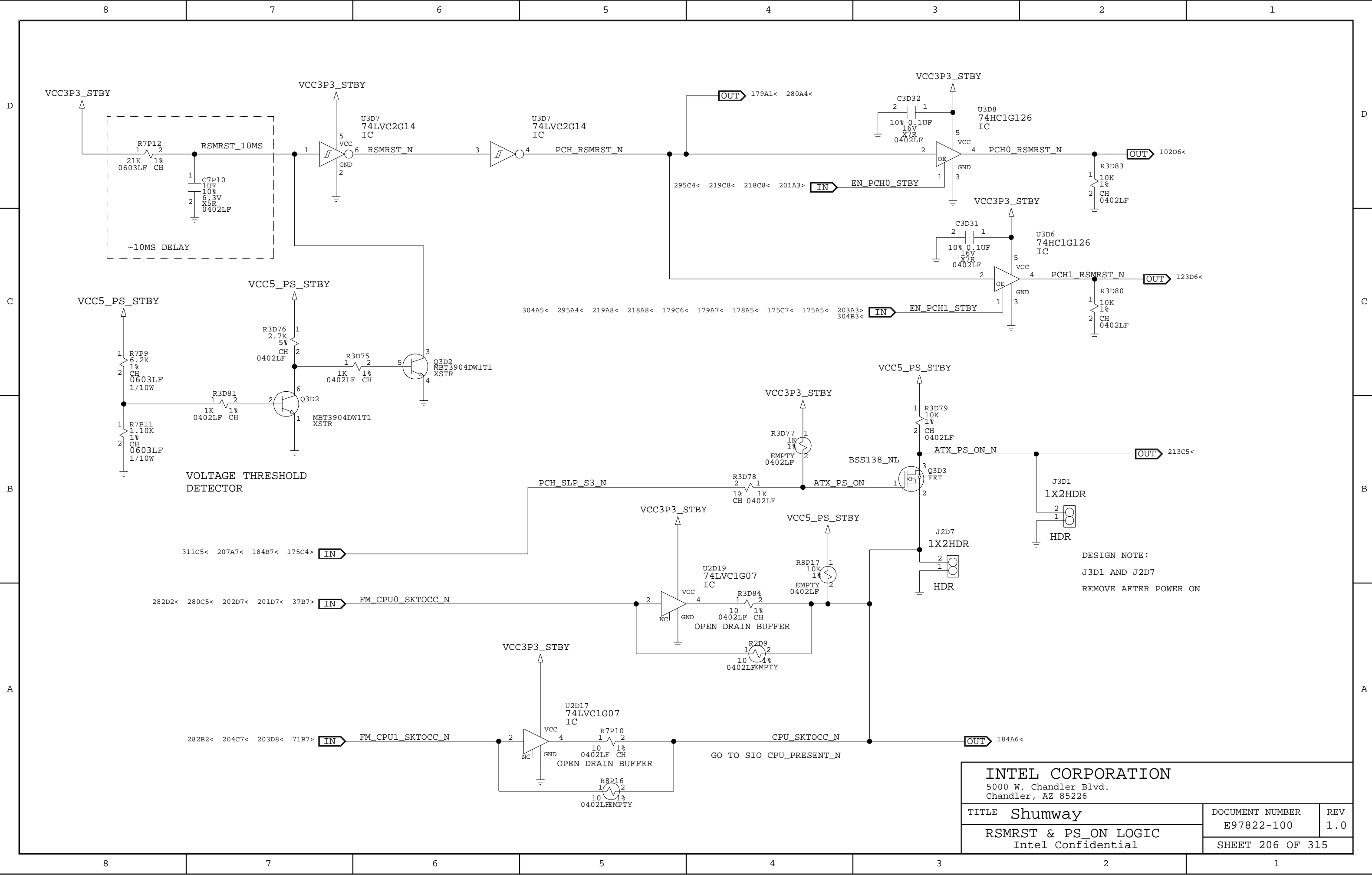
E97822-100

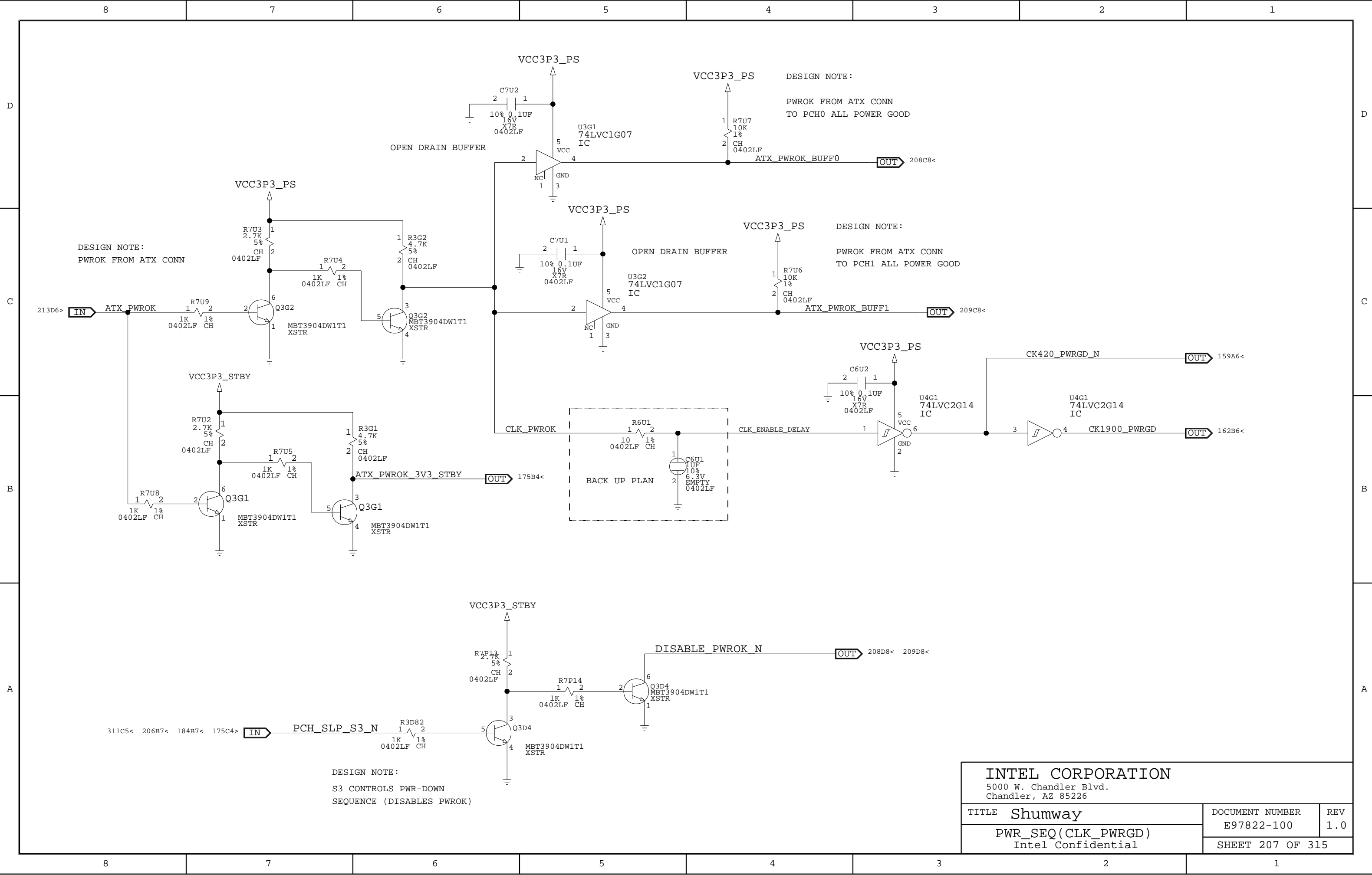
REV

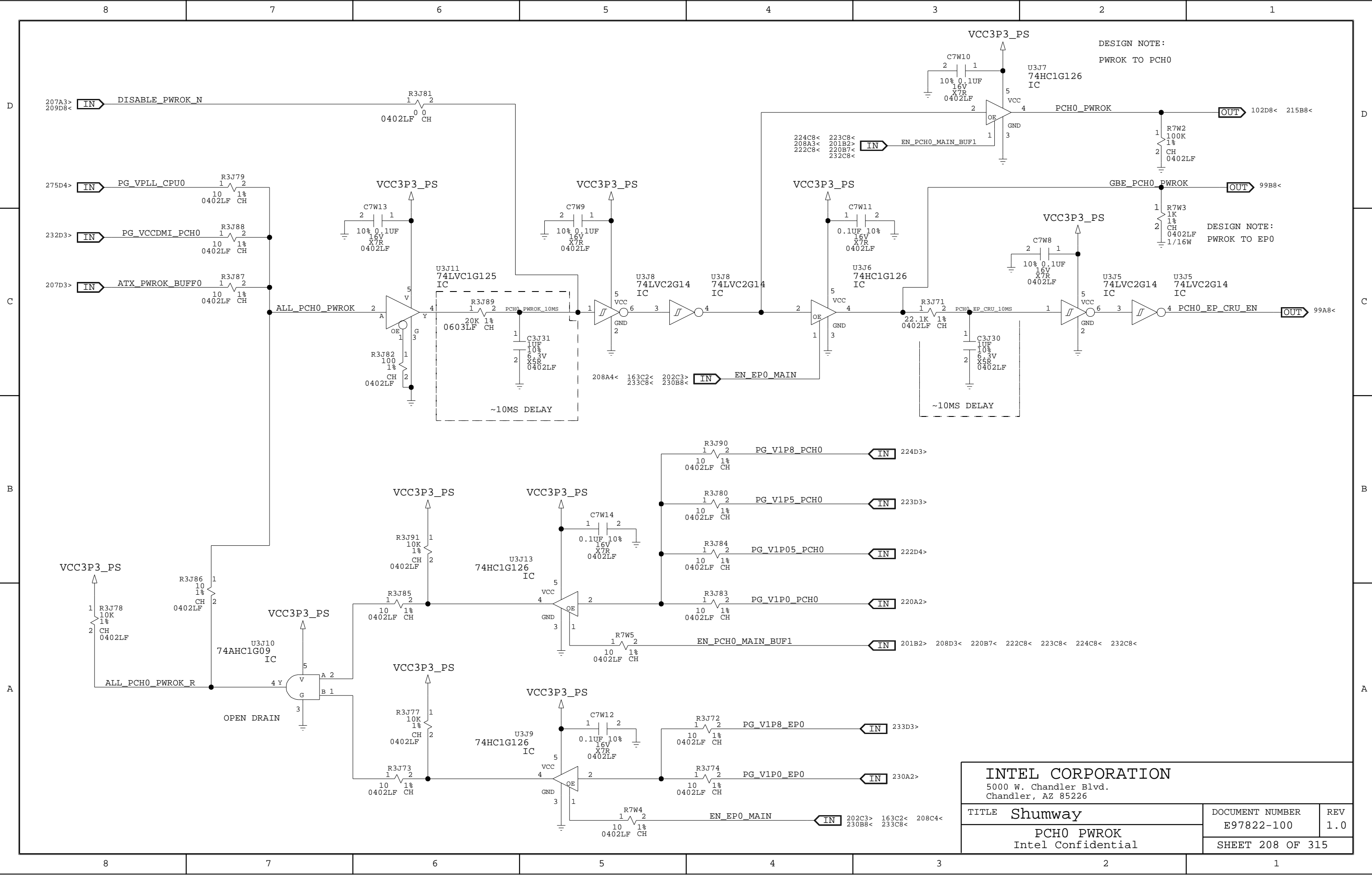
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5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

PCH0 PWROK  
Intel Confidential

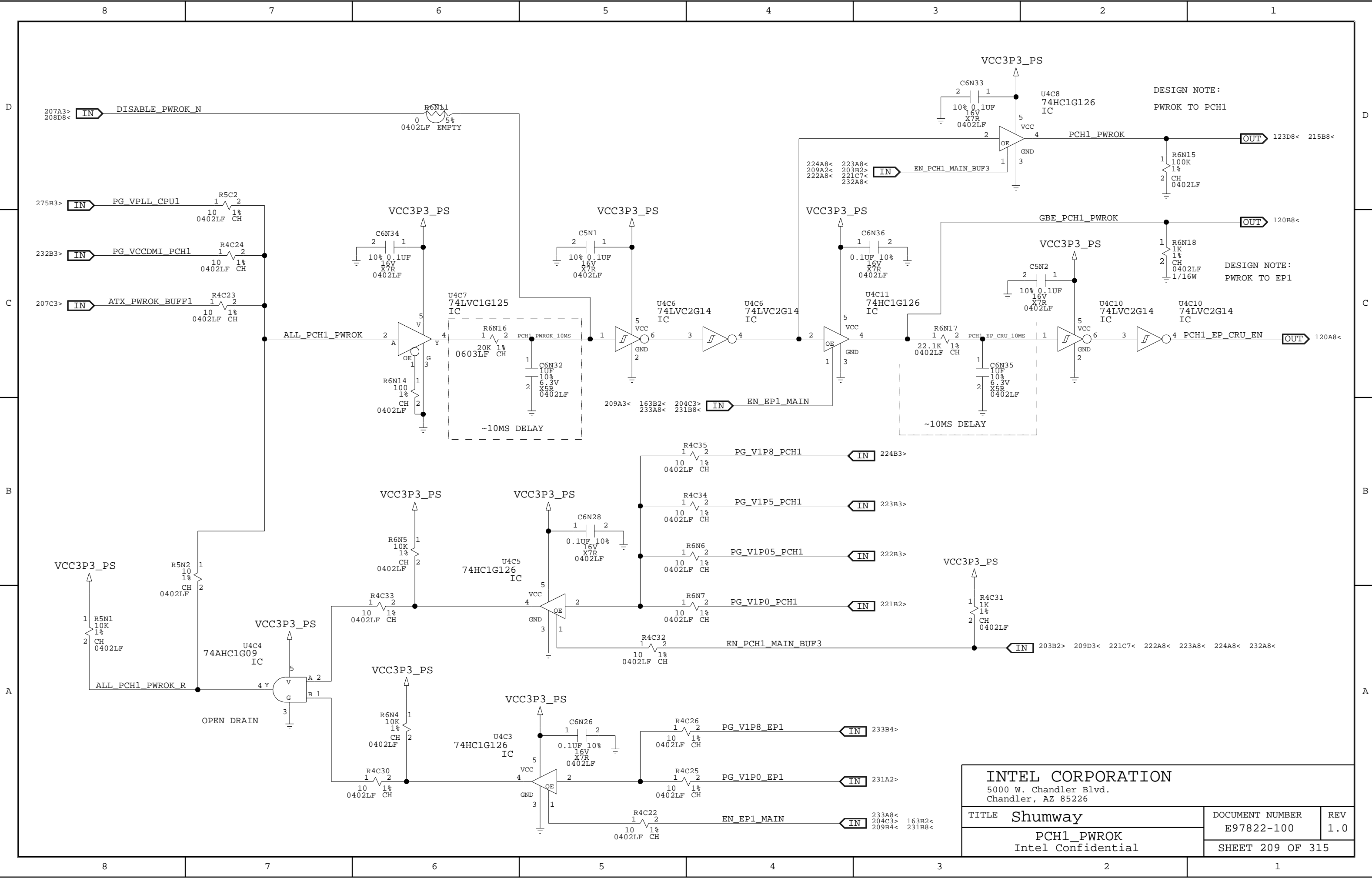
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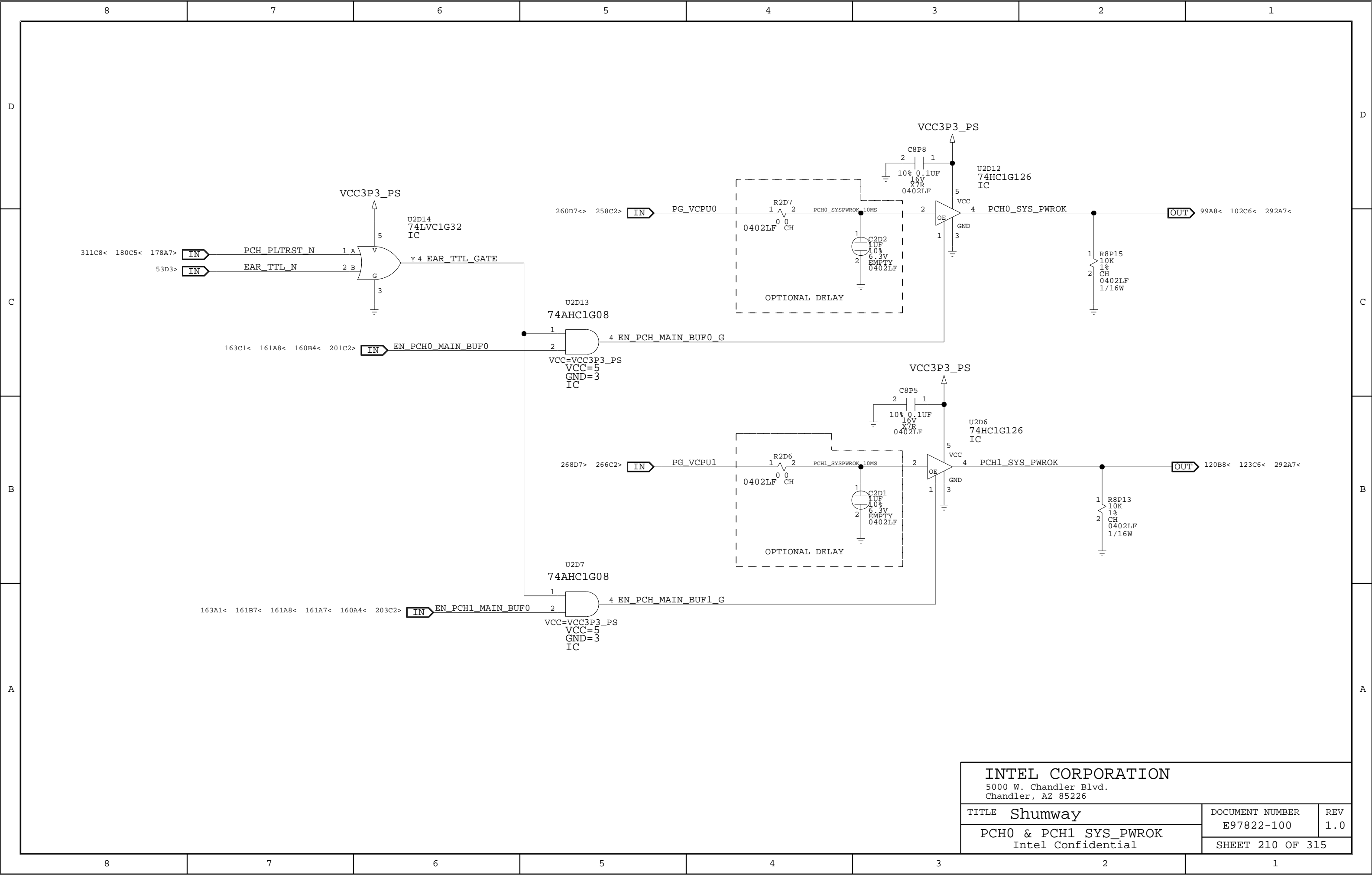
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TITLE Shumway

PCH0 & PCH1 SYS\_PWROK  
Intel Confidential

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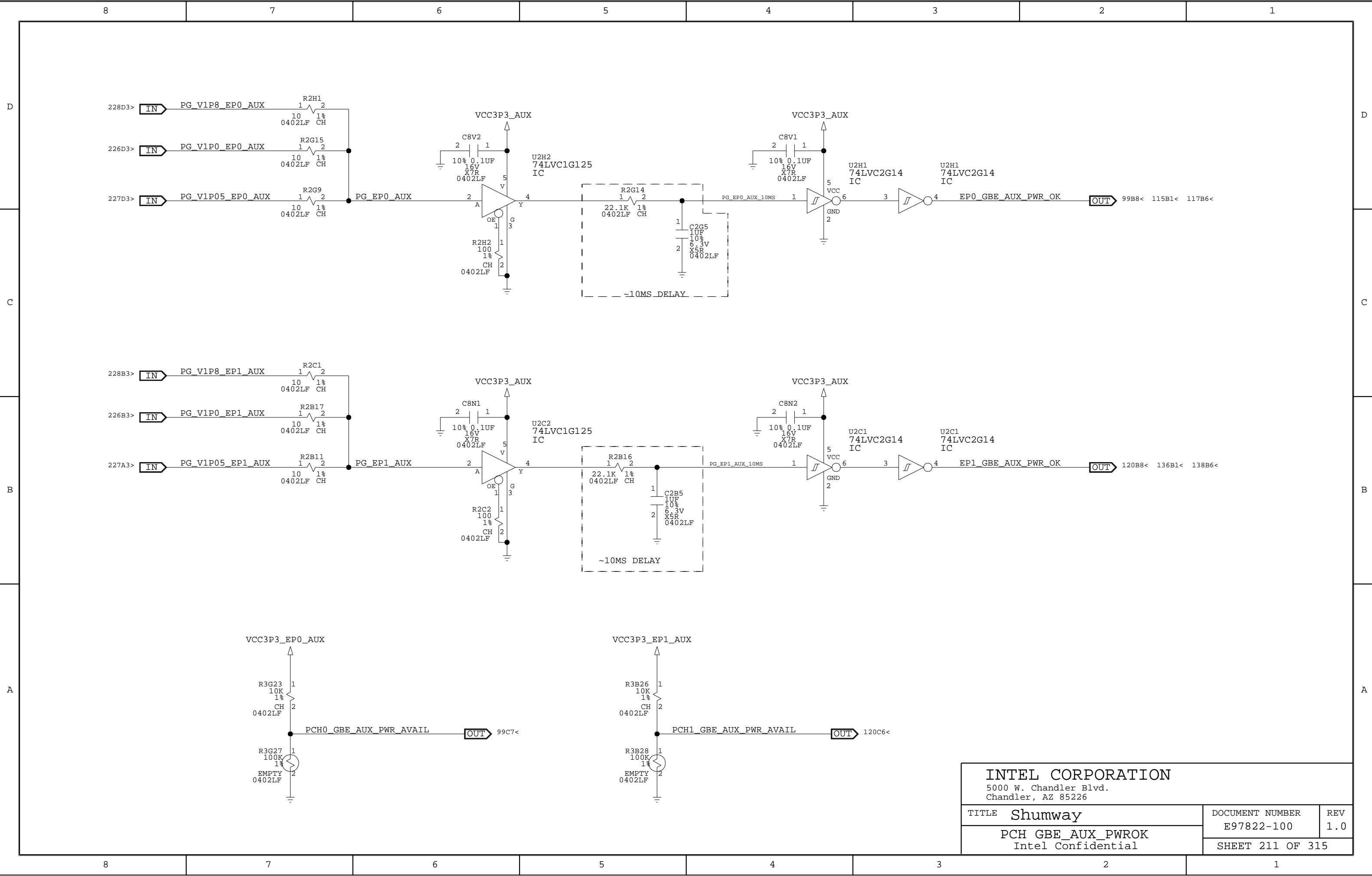
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## POWER SUPPLIES

INTEL CORPORATION

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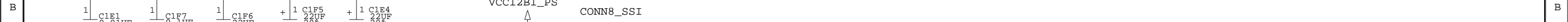
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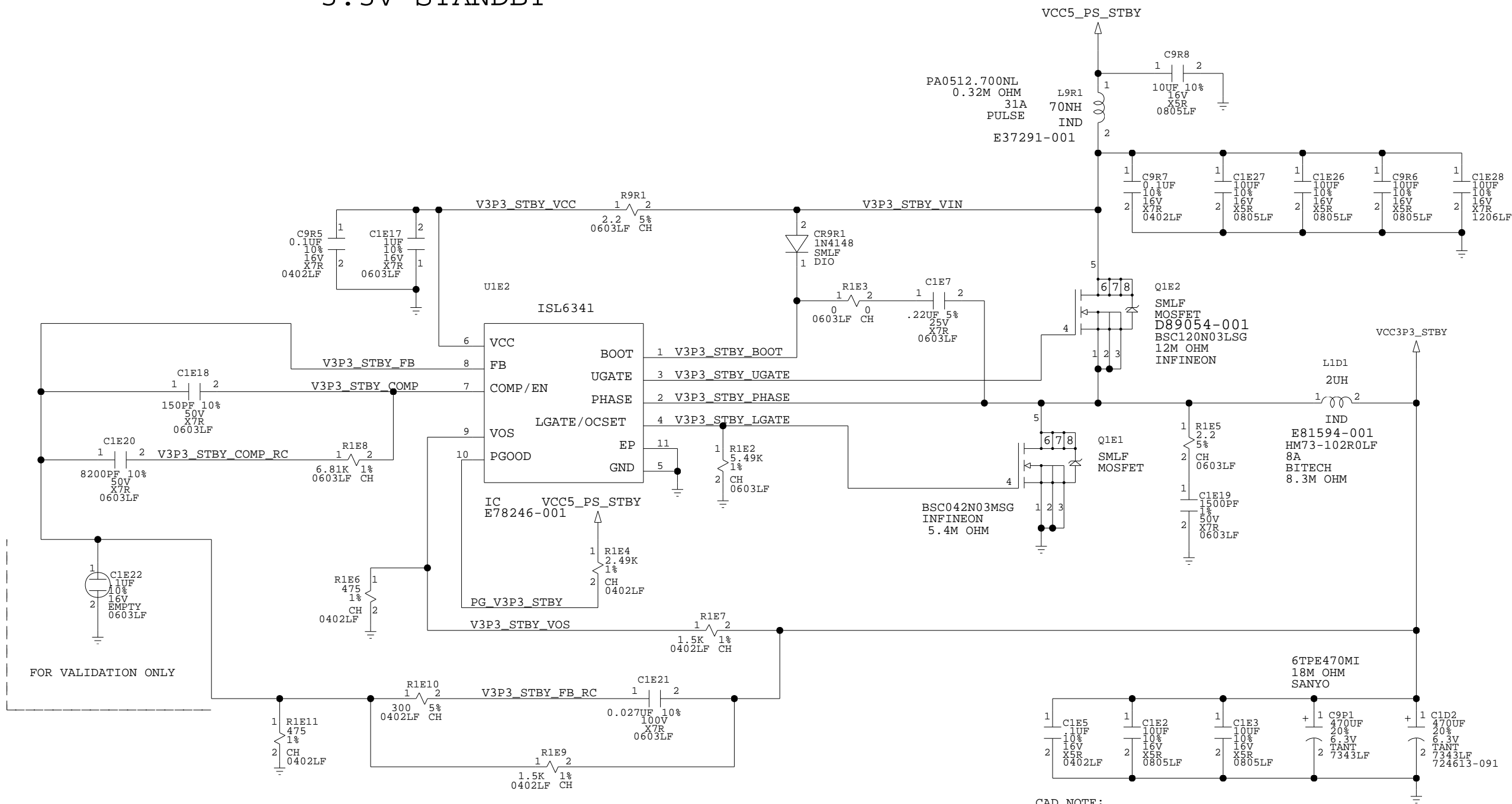
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D		MBRD1035CTL	MBRD1035CTL	D
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3.3V STANDBY



FOR VALIDATION ONLY

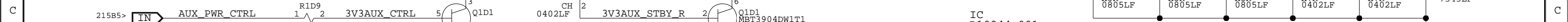
CAD NOTE:  
PLACE THESE CAPS  
CLOSE TO  
THE OUTPUT INDUCTOR

VCC3P3_STBY = 3.3V STBY	
PEAK	5A
ESTIMATED USE	3A
ACTIVE STATE	S0-S5

$VOUT = 0.8 (RFS + ROS) / ROS$

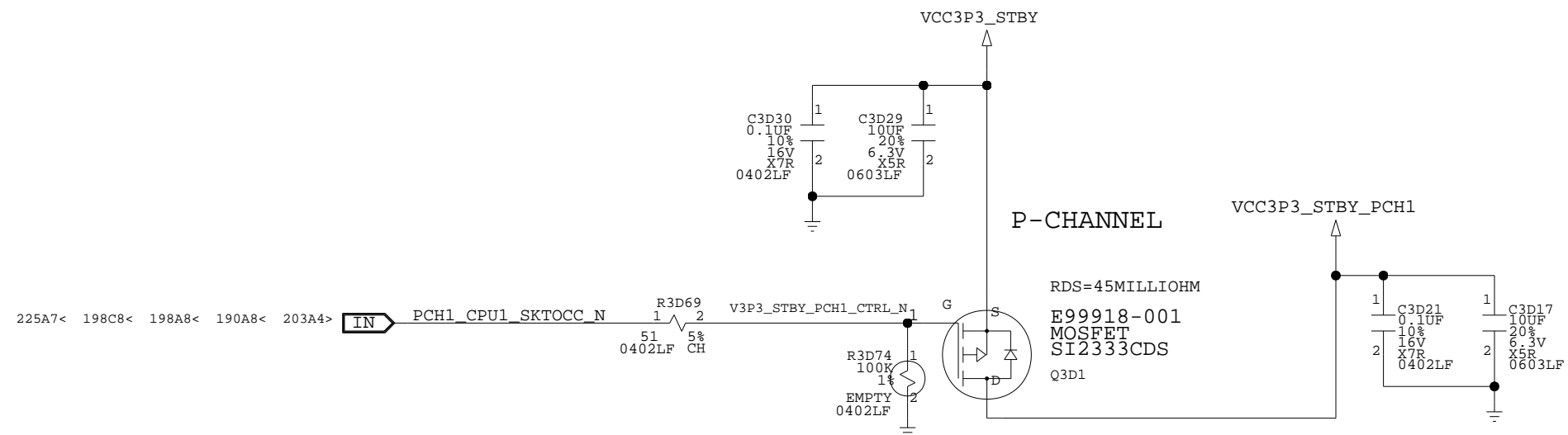
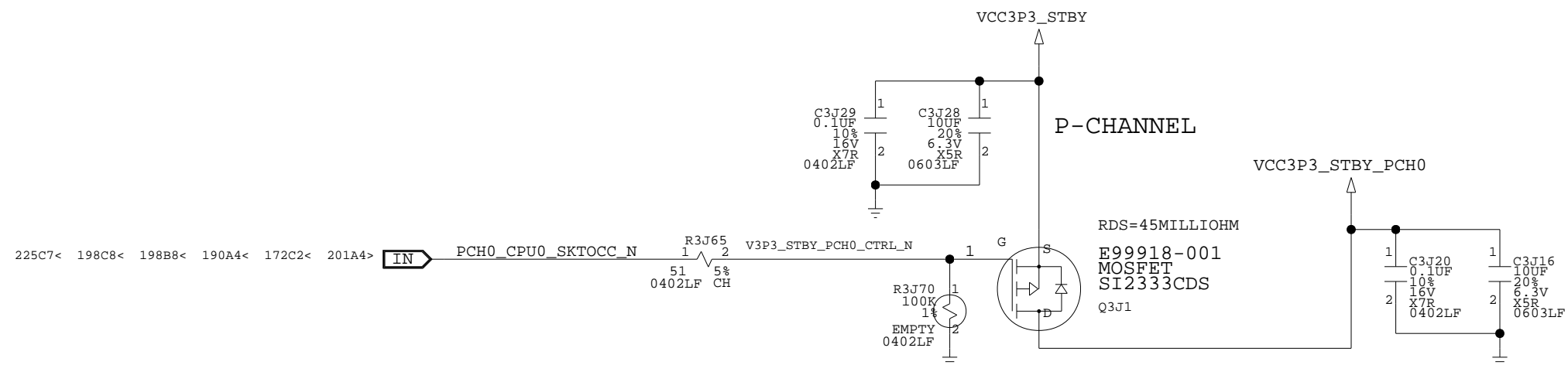
INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
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	+3.3V STBY	E97822-100
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\* = DEFAULT

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+3.3V AUX Intel Confidential	<b>SHEET 216 OF 315</b>	



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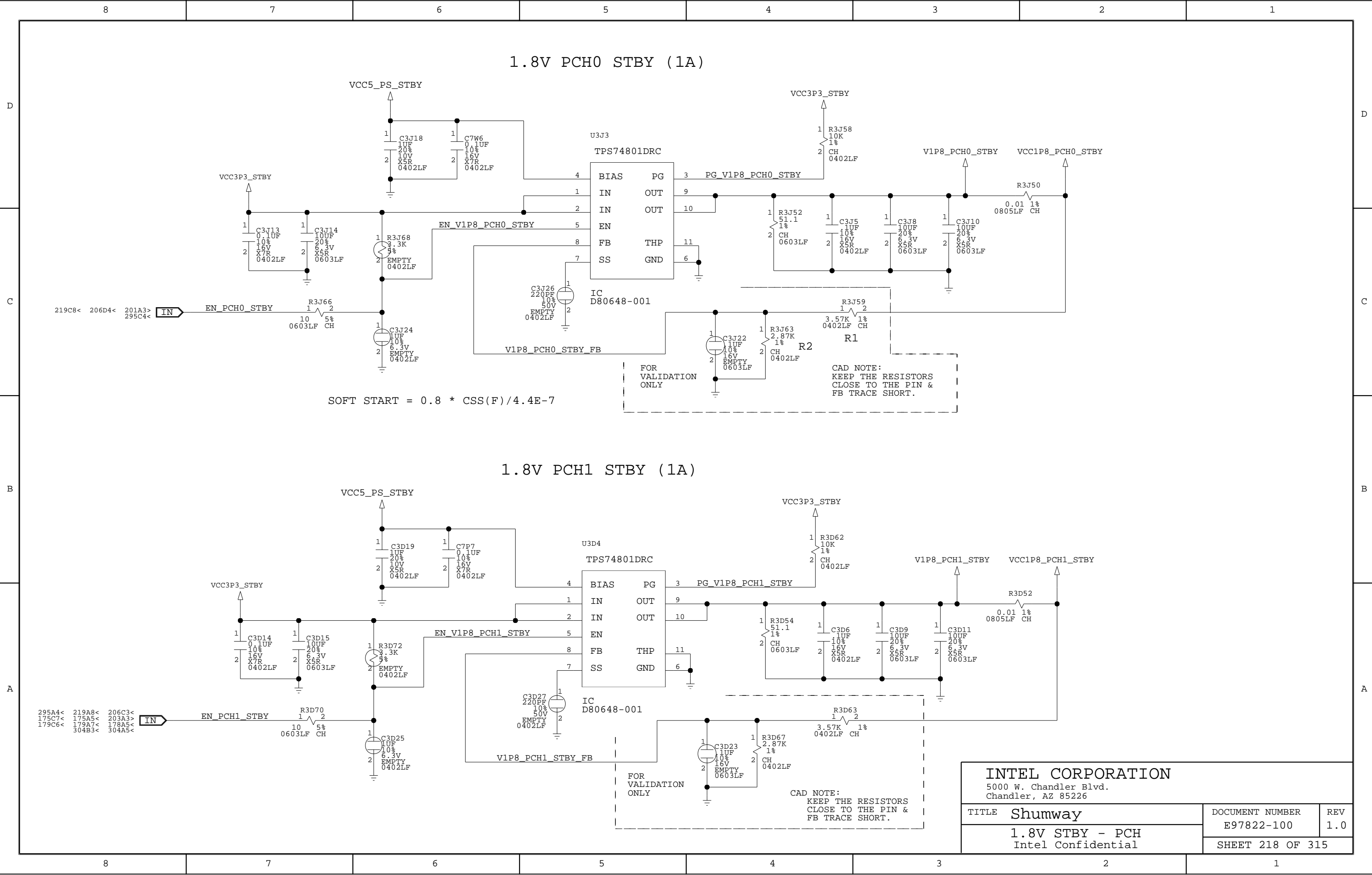
3.3V STBY - PCH  
Intel Confidential

DOCUMENT NUMBER

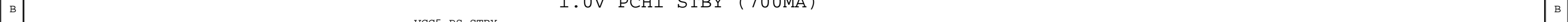
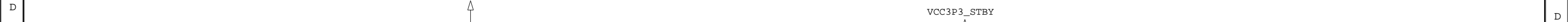
E97822-100

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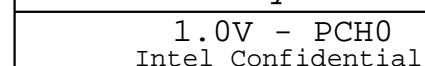
SHEET 217 OF 315

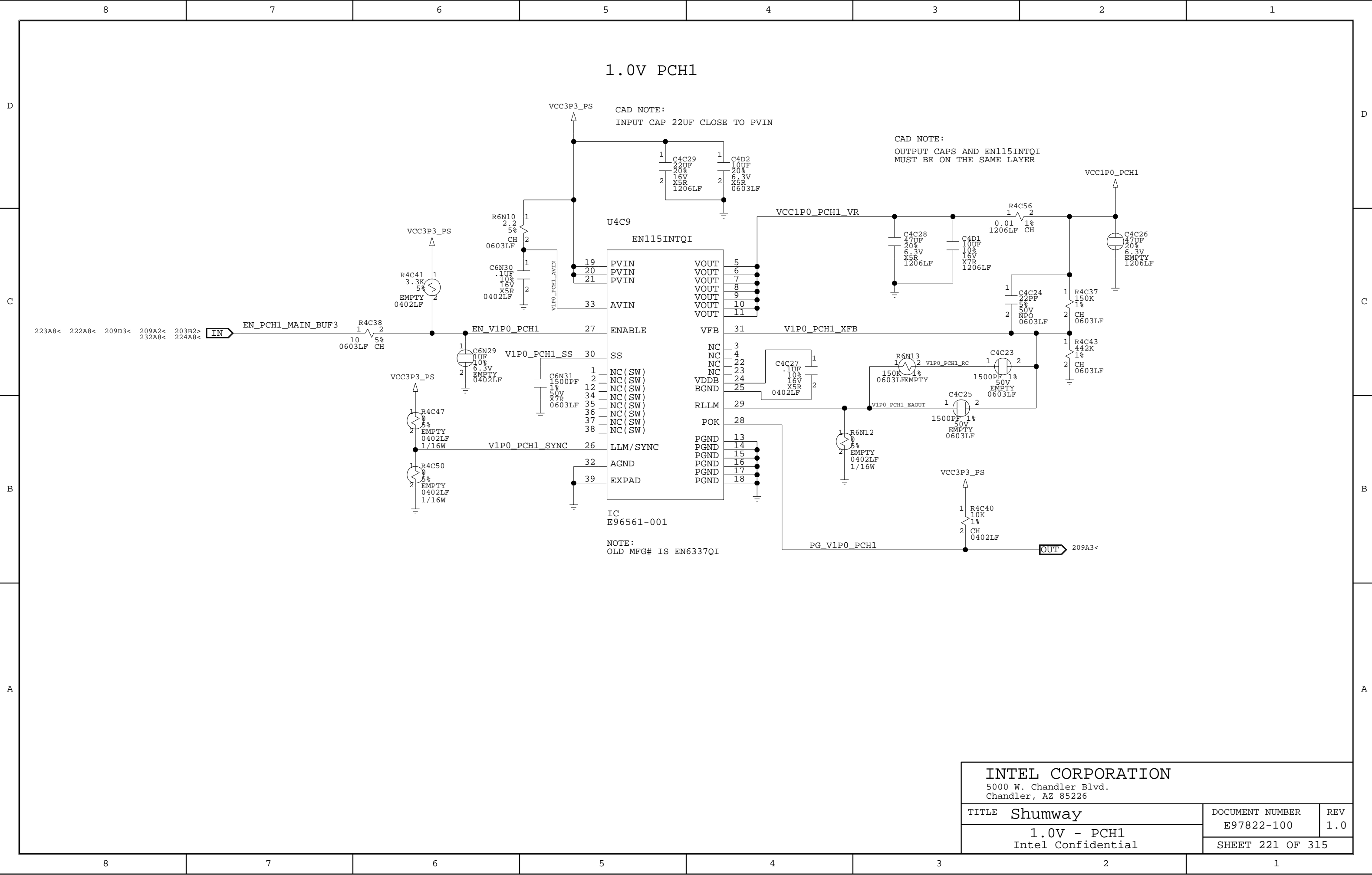


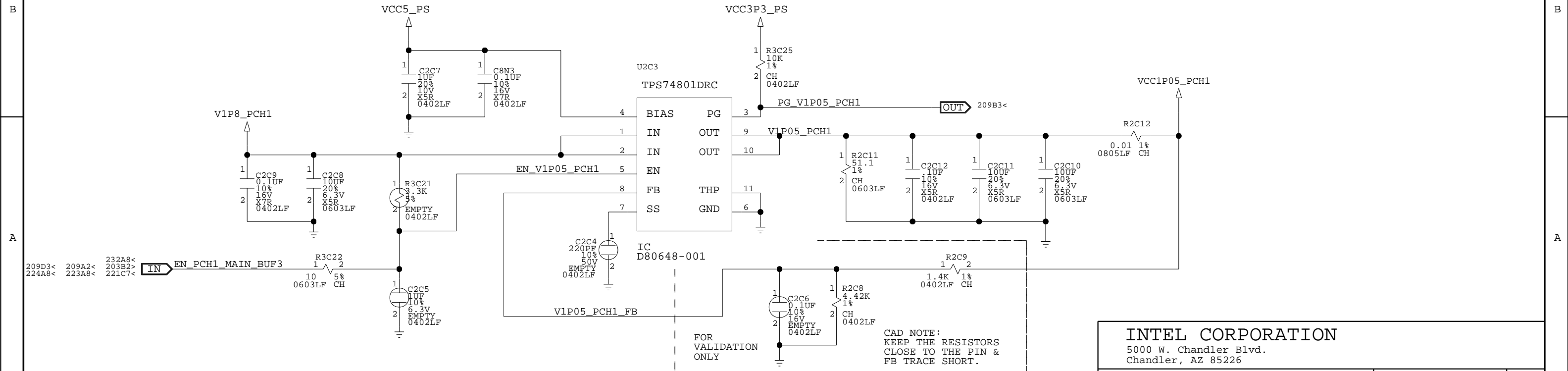
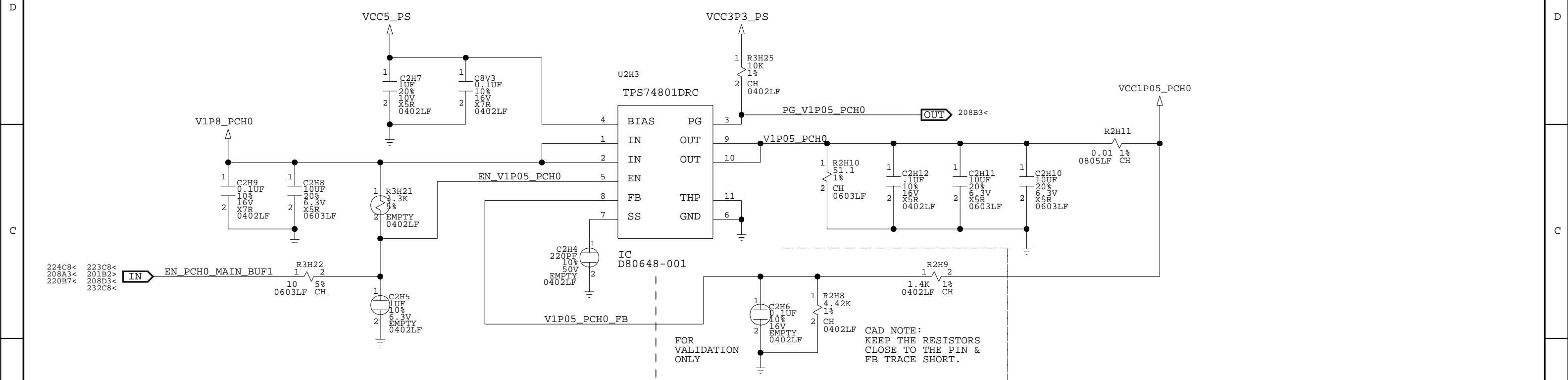




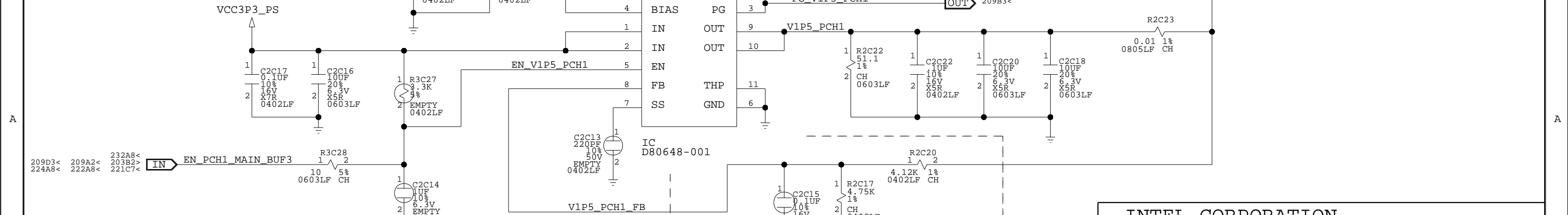
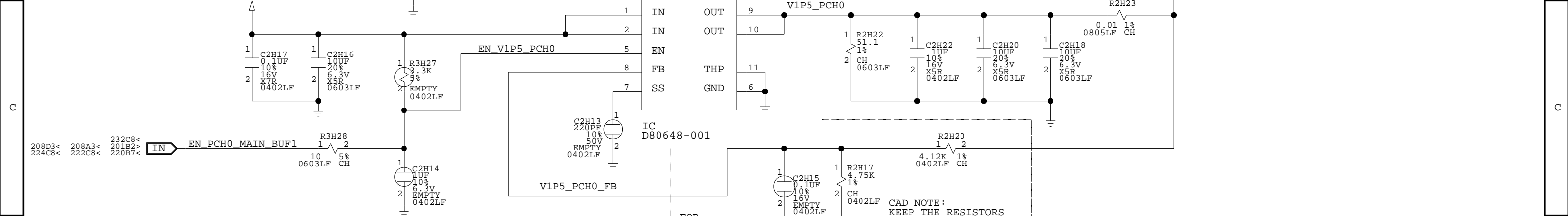
5000 W. Chandler Blvd. Chandler, AZ 85226		
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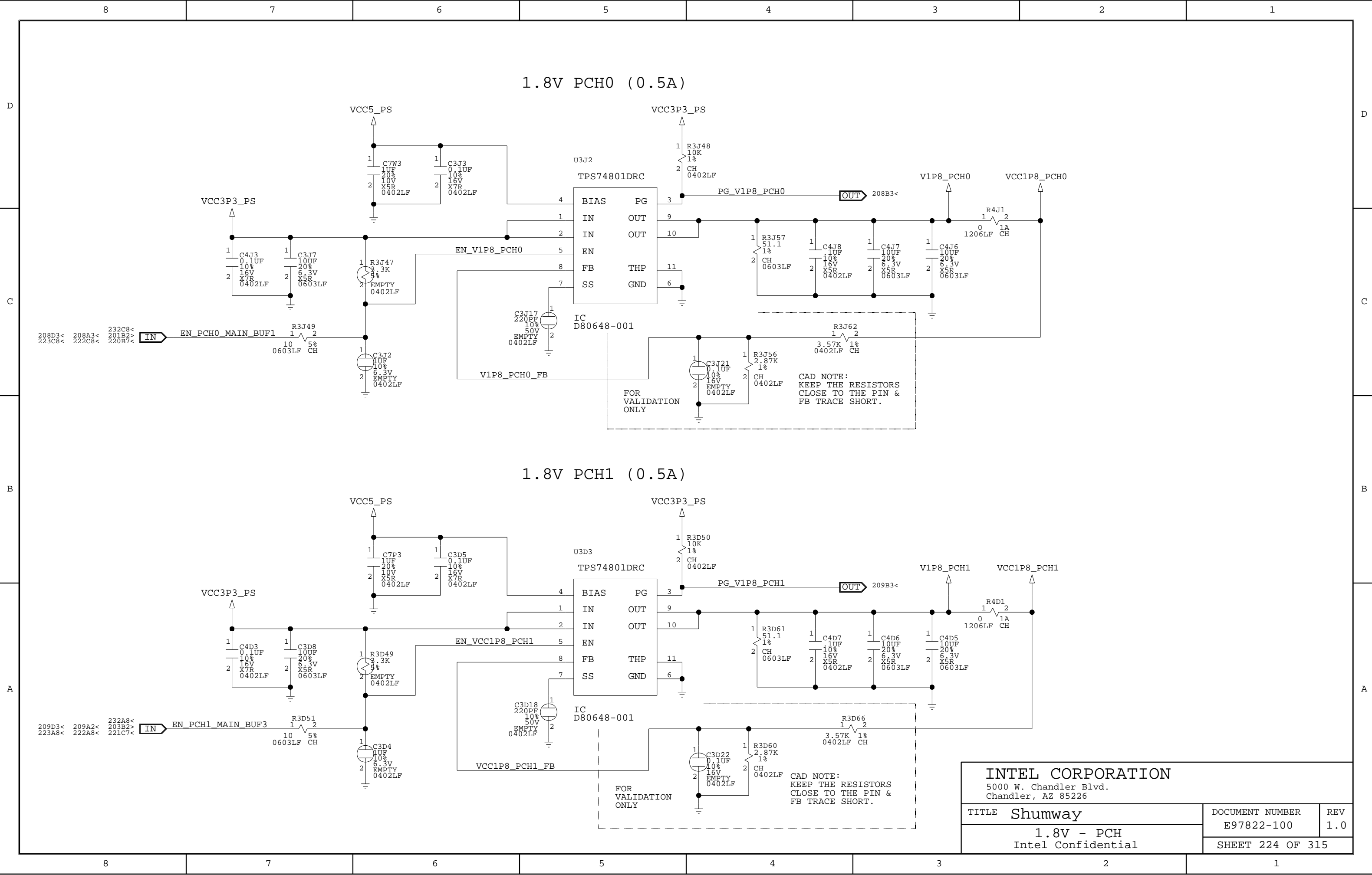


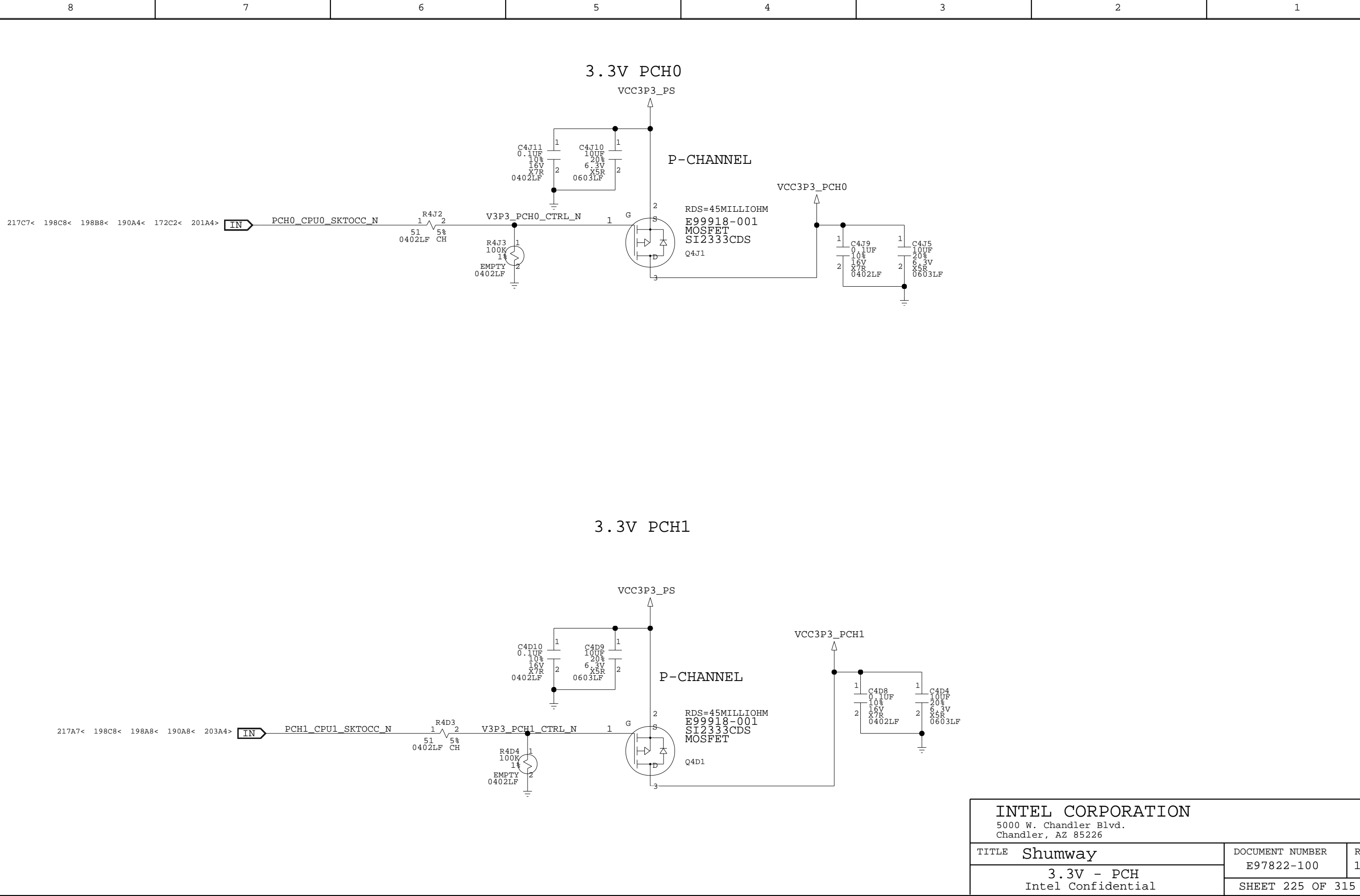


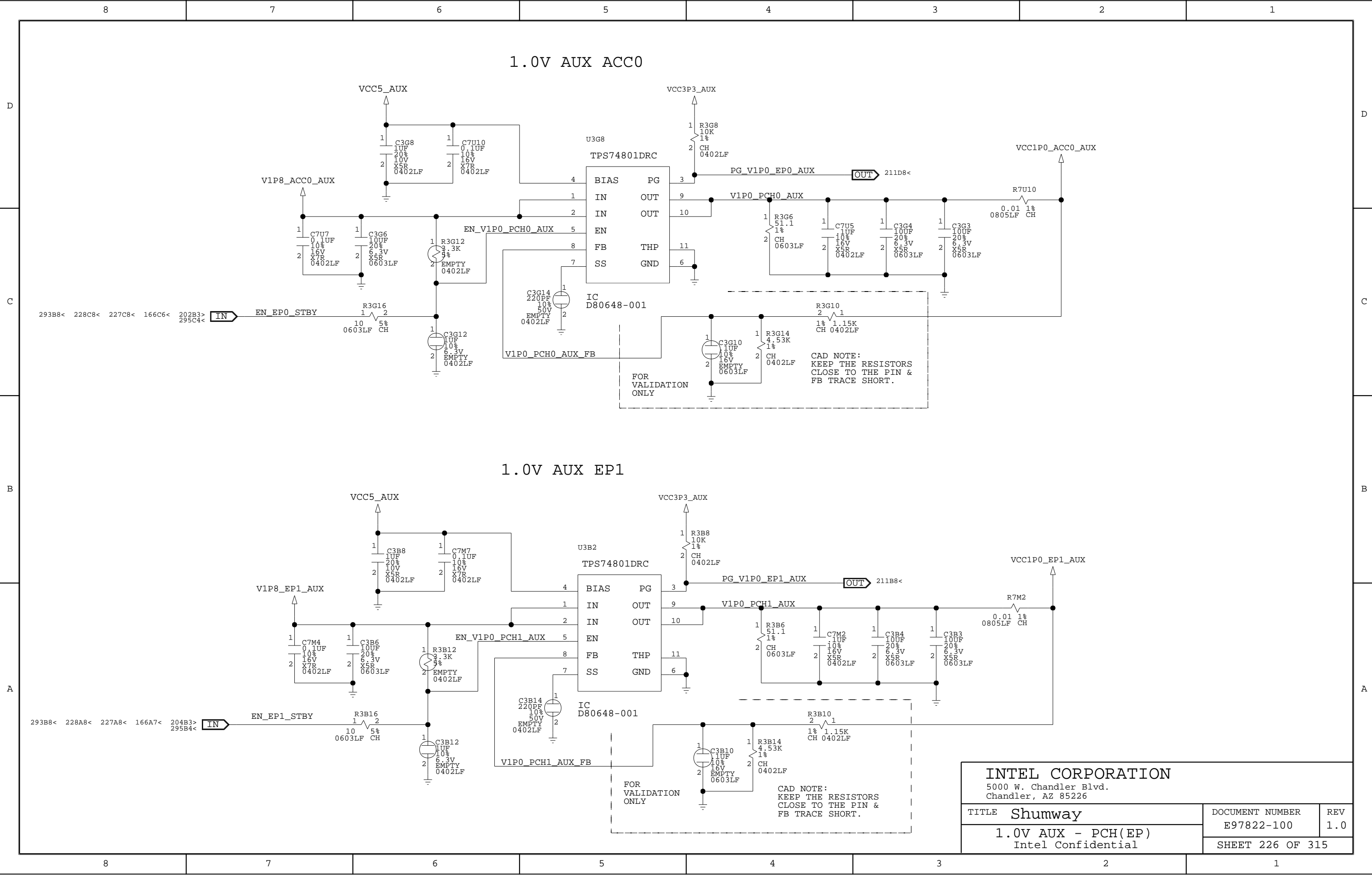


TITLE	Shumway	DOCUMENT NUMBER	REV
1.05V - PCH		E97822-100	1.0
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1

2

EN\_EP0\_STBY

IN

1

2

R3G8

10K

1%

CH

0402LF

1

2

PG\_V1P0\_EP0\_AUX

OUT

211D8<

1

2

V1P0\_PCH0\_AUX

1

2

R3G6

51.1

1%

CH

0603LF

1

2

C7U5

1UF

10%

16V

X5R

0402LF

1

2

C3G4

10UF

20%

6.3V

X5R

0603LF

1

2

C3G3

10UF

20%

6.3V

X5R

0603LF

1

2

R7U10

0.01

1%

0805LF

CH

1

2

VCC1P0\_ACC0\_AUX

1

2

R3G10

2

1

1.15K

CH

0402LF

1

2

R3G14

4.53K

1%

CH

0402LF

1

2

C3G10

1UF

10%

16V

EMPTY

0603LF

1

2

C3G14

220PF

10%

50V

EMPTY

0402LF

1

2

V1P0\_PCH0\_AUX\_FB

1

2

IC

D80648-001

1

2

BIAS

PG

1

2

IN

OUT

1

2

IN

OUT

1

2

EN

THP

1

2

FB

GND

1

2

SS

GND

1

2

U3G8

TPS74801DRC

1

2

VCC5\_AUX

1

2

VCC3P3\_AUX

1

2

V1P8\_ACC0\_AUX

1

2

V1P0\_PCH0\_AUX

1

2

VCC1P0\_ACC0\_AUX

1

2

V1P0\_PCH0\_AUX\_FB

1

2

FOR VALIDATION ONLY

1

2

CAD NOTE:

KEEP THE RESISTORS

CLOSE TO THE PIN &

FB TRACE SHORT.

1.0V AUX EP1

V1P8\_EP1\_AUX

1

2

C7M4

0.1UF

10%

16V

X7R

0402LF

1

2

C3B6

10UF

20%

6.3V

X5R

0603LF

1

2

R3B12

3.3K

1%

EMPTY

0402LF

1

2

C3B12

1UF

10%

6.3V

EMPTY

0402LF

1

2

R3B16

10

5%

0603LF

CH

1

2

EN\_EP1\_STBY

IN

1

2

R3B8

10K

1%

CH

0402LF

1

2

PG\_V1P0\_EP1\_AUX

OUT

211B8<

1

2

V1P0\_PCH1\_AUX

1

2

R3B6

51.1

1%

CH

0603LF

1

2

C7M2

1UF

10%

16V

X5R

0402LF

1

2

C3B4

10UF

20%

6.3V

X5R

0603LF

1

2

C3B3

10UF

20%

6.3V

X5R

0603LF

1

2

R7M2

0.01

1%

0805LF

CH

1

2

VCC1P0\_EP1\_AUX

1

2

R3B10

2

1

1.15K

CH

0402LF

1

2

R3B14

4.53K

1%

CH

0402LF

1

2

C3B10

1UF

10%

16V

EMPTY

0603LF

1

2

C3B14

220PF

10%

50V

EMPTY

0402LF

1

2

V1P0\_PCH1\_AUX\_FB

1

2

IC

D80648-001

1

2

BIAS

PG

1

2

IN

OUT

1

2

IN

OUT

1

2

EN

THP

1

2

FB

GND

1

2

SS

GND

1

2

U3B2

TPS74801DRC

1

2

VCC5\_AUX

1

2

VCC3P3\_AUX

1

2

V1P8\_EP1\_AUX

1

2

V1P0\_PCH1\_AUX

1

2

VCC1P0\_EP1\_AUX

1

2

V1P0\_PCH1\_AUX\_FB

1

2

FOR VALIDATION ONLY

1

2

CAD NOTE:

KEEP THE RESISTORS

CLOSE TO THE PIN &

FB TRACE SHORT.

INTEL CORPORATION

5000 W. Chandler Blvd.

Chandler, AZ 85226

TITLE Shumway

1.0V AUX - PCH(EP)

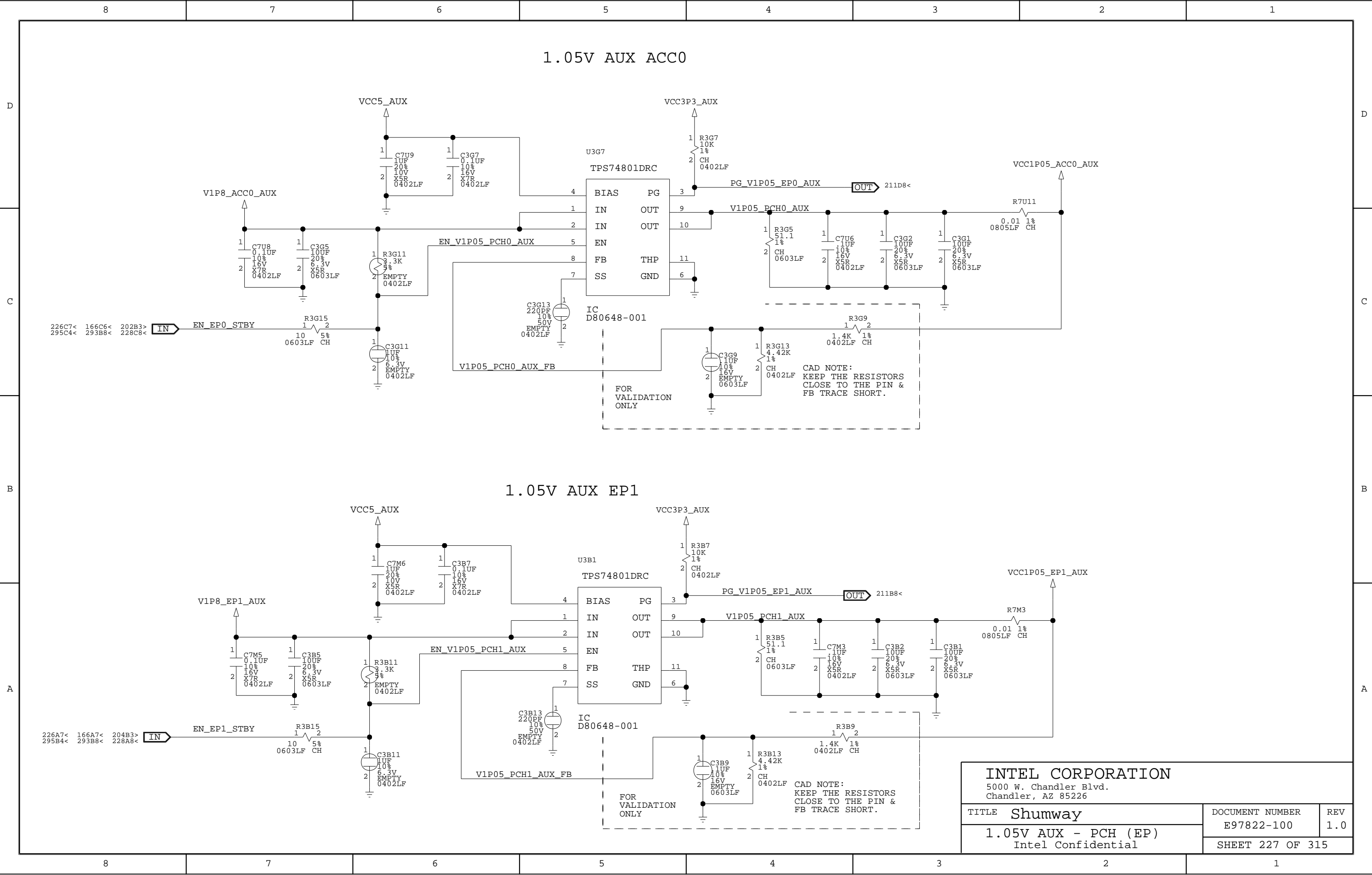
Intel Confidential

DOCUMENT NUMBER E97822-100

SHEET 226 OF 315

REV 1.0





1

2

C3G2

10UF

20%

6.3V

X5R

0603LF

1

2

C3G1

10UF

20%

6.3V

X5R

0603LF

PG\_V1P05\_EP0\_AUX

OUT

211D8<

VCC3P3\_AUX

1

2

R3G7

10K

1%

CH

0402LF

1

2

C3G9

1UF

10%

16V

EMPTY

0603LF

1

2

R3G13

4.42K

1%

CH

0402LF

1

2

R3G9

1.4K

1%

CH

1

0.01

1%

CH

R7U11

0805LF

VCC1P05\_ACC0\_AUX

IC

D80648-001

FOR VALIDATION ONLY

CAD NOTE:

KEEP THE RESISTORS

CLOSE TO THE PIN &

FB TRACE SHORT.

1.05V AUX EP1

V1P8\_EP1\_AUX

1

2

C7M5

0.1UF

10%

16V

X7R

0402LF

1

2

C3B5

10UF

20%

6.3V

X5R

0603LF

1

2

R3B11

3.3K

5%

EMPTY

0402LF

1

2

C3B11

1UF

10%

6.3V

EMPTY

0402LF

1

2

R3B15

5%

CH

10

0603LF

EN\_EP1\_STBY

IN

226A7<

166A7<

204B3>

295B4<

293B8<

228A8<

VCC5\_AUX

1

2

C7M6

1UF

20%

10V

X5R

0402LF

1

2

C3B7

0.1UF

10%

16V

X7R

0402LF

4

1

2

5

8

7

U3B1

TPS74801DRC

BIAS

IN

IN

EN

FB

SS

PG

OUT

OUT

THP

GND

3

9

10

11

6

V1P05\_PCH1\_AUX

1

2

R3B5

51.1

1%

CH

0603LF

1

2

C7M3

1UF

10%

16V

X5R

0402LF

1

2

C3B2

10UF

20%

6.3V

X5R

0603LF

1

2

C3B1

10UF

20%

6.3V

X5R

0603LF

PG\_V1P05\_EP1\_AUX

OUT

211B8<

VCC3P3\_AUX

1

2

R3B7

10K

1%

CH

0402LF

1

2

C3B9

1UF

10%

16V

EMPTY

0603LF

1

2

R3B13

4.42K

1%

CH

0402LF

1

2

R3B9

1.4K

1%

CH

1

0.01

1%

CH

R7M3

0805LF

VCC1P05\_EP1\_AUX

IC

D80648-001

FOR VALIDATION ONLY

CAD NOTE:

KEEP THE RESISTORS

CLOSE TO THE PIN &

FB TRACE SHORT.

INTEL CORPORATION

5000 W. Chandler Blvd.

Chandler, AZ 85226

TITLE

Shumway

1.05V AUX - PCH (EP)

Intel Confidential

DOCUMENT NUMBER

E97822-100

REV

1.0

SHEET 227 OF 315

8

7

6

5

4

3

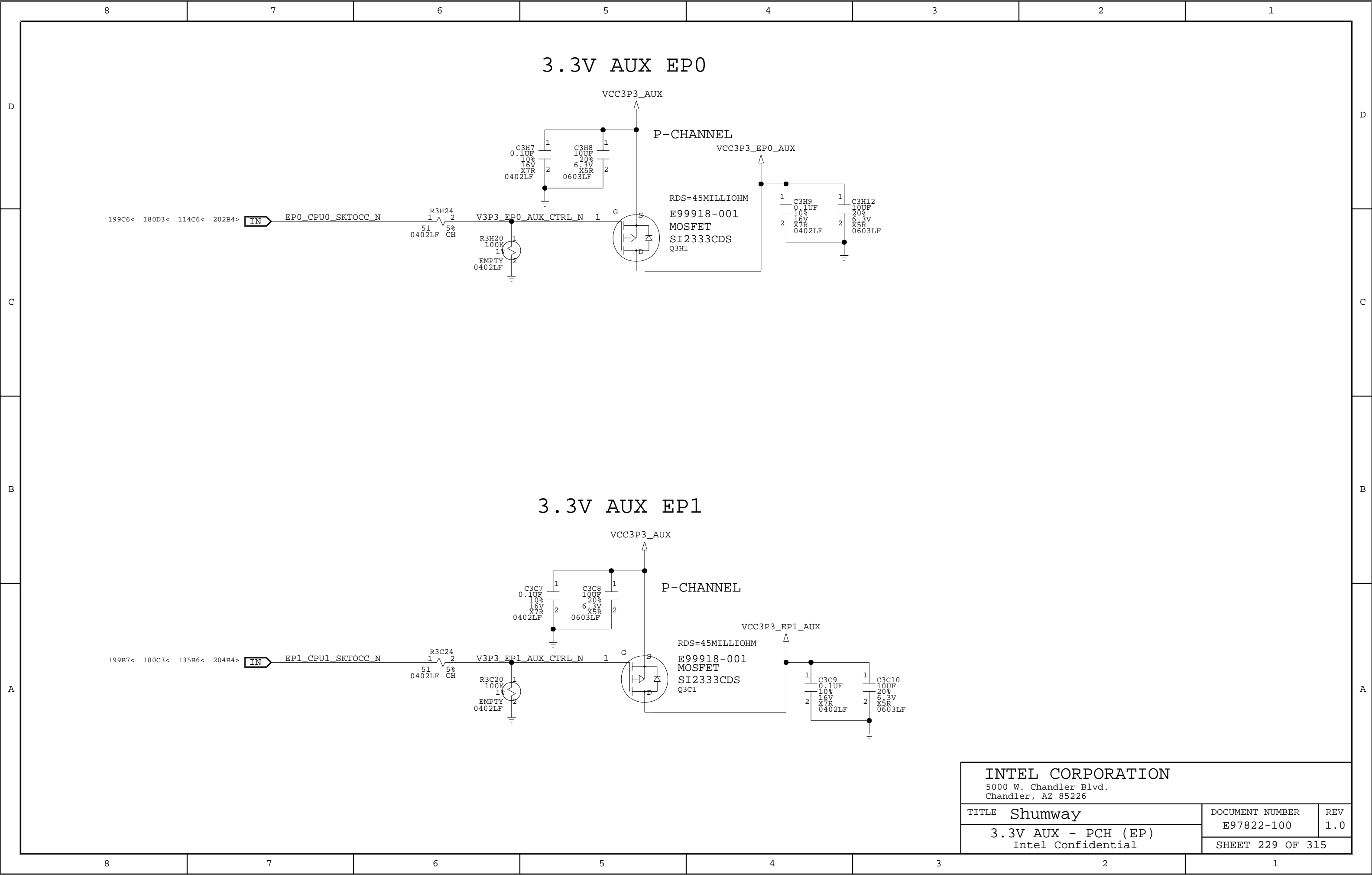
2

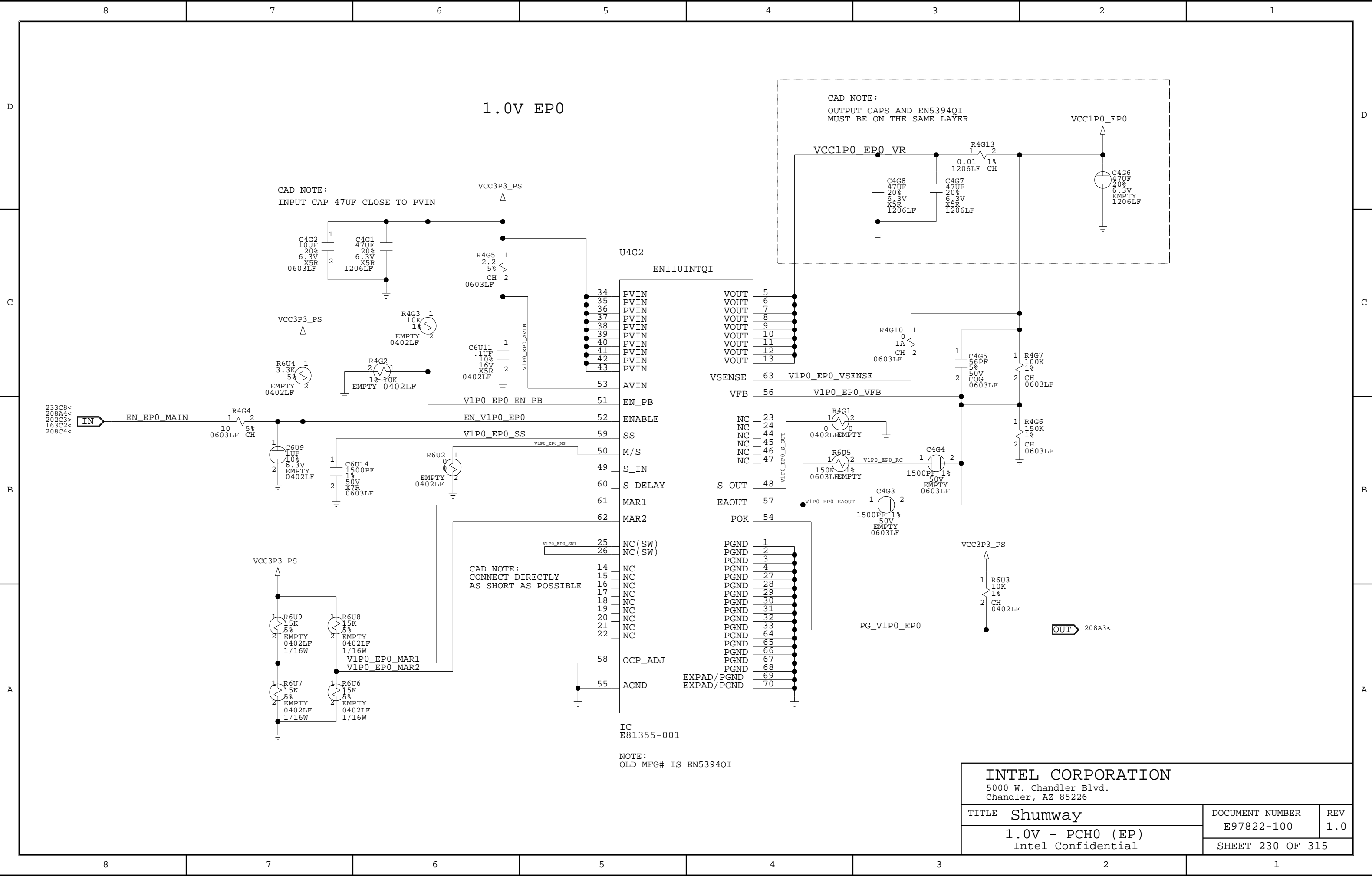
1

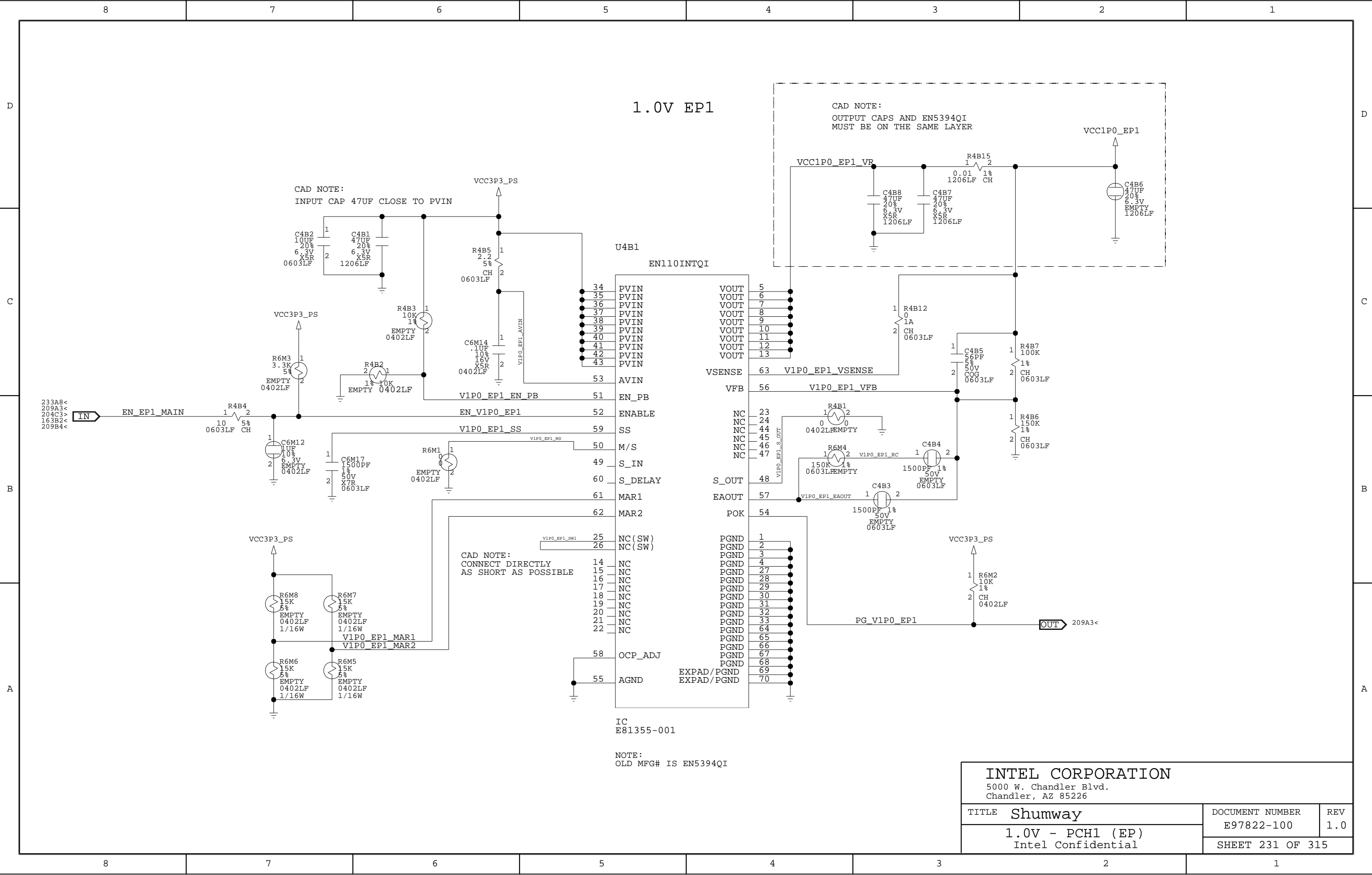
A



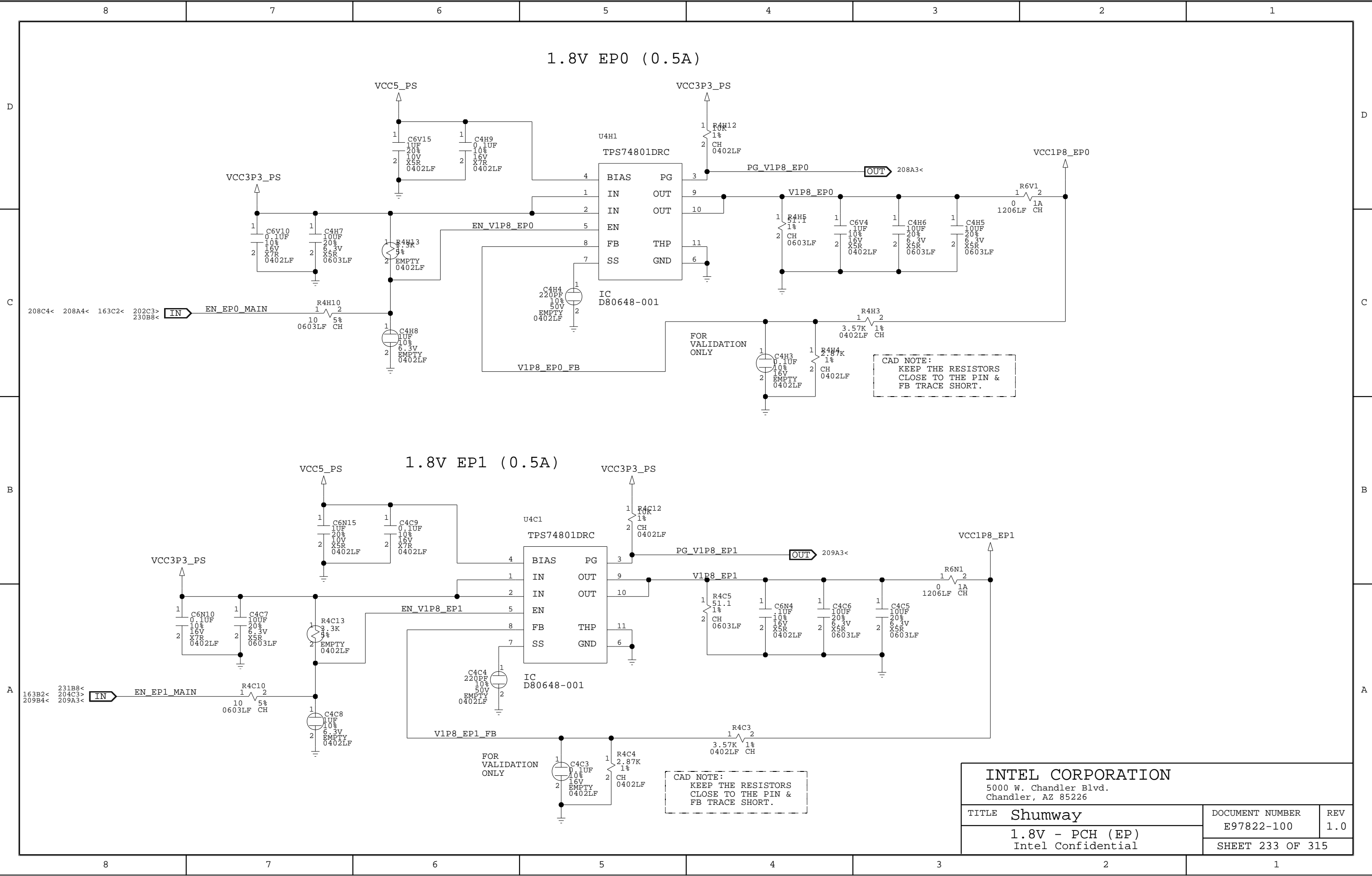
SHEET 228 OF 315











8

7

6

5

4

3

2

1

CPU1 CHANNEL EFG

5000 W. Chandler Blvd.  
Chandler, AZ 85226

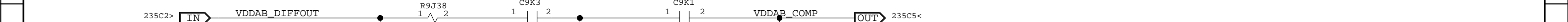
1.0

SHEET 234 OF 315

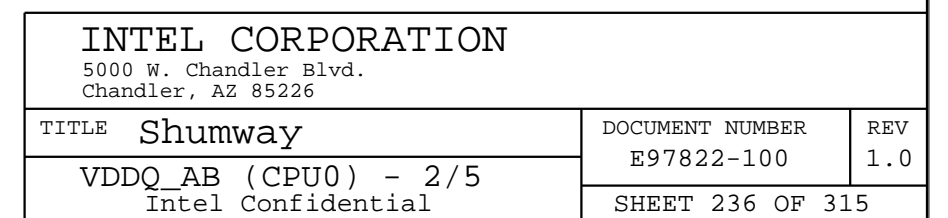




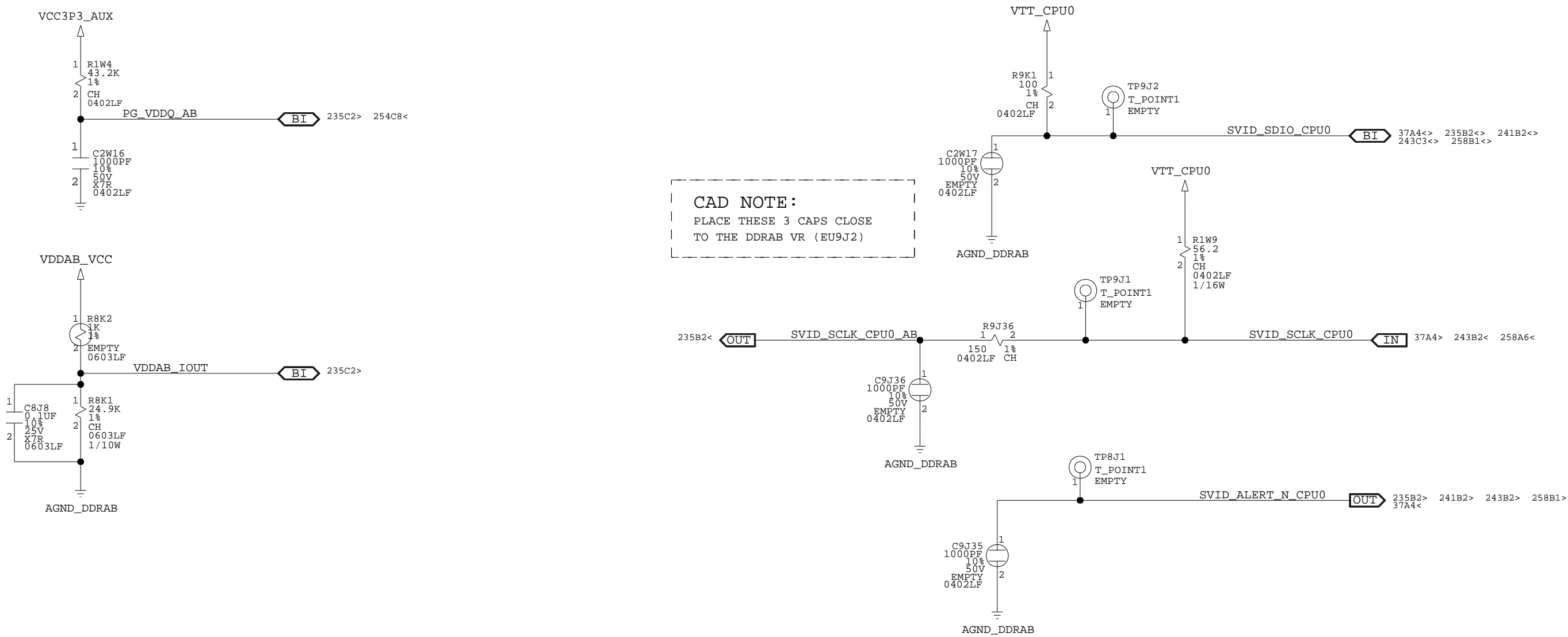
D	235056	VDDAR_DROOP	D
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A	0603LFP		A
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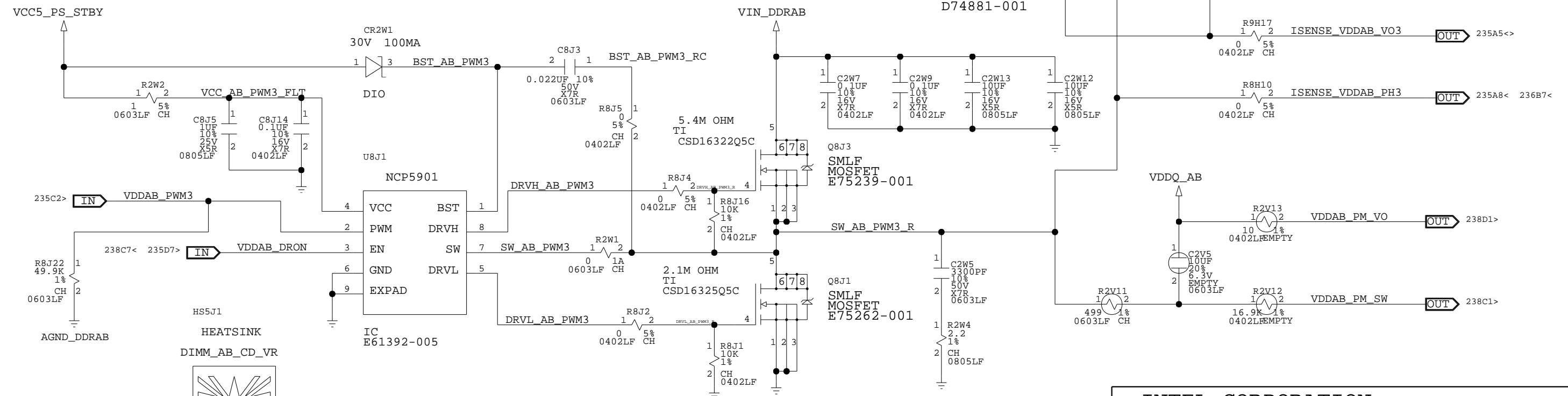
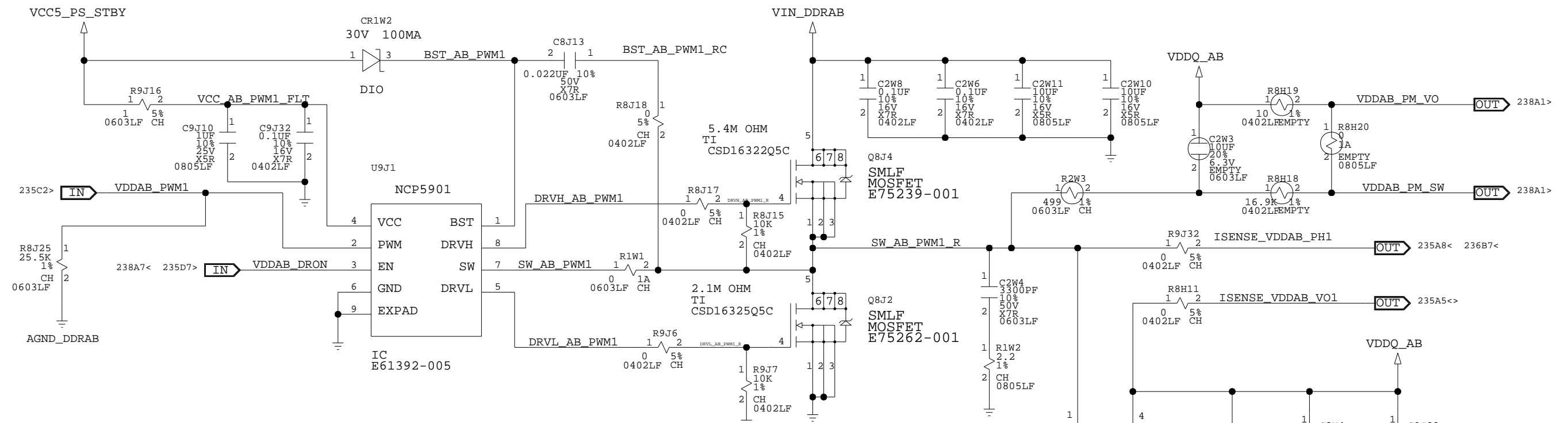
DDR3 CHANNEL AB 3/5 - CPU0



CAD NOTE:  
PLACE THESE 3 CAPS CLOSE  
TO THE DDRAB VR (EU9J2)

INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VDDQ_AB (CPU0) - 3/5 Intel Confidential	SHEET 237 OF 315	

# DDR3 CHANNEL AB 4/5 - CPU0



HTSK  
E66260-001

HEAT SINK REQUIRED ON FETS

INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE	Shumway
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VDDQ\_AB (CPU0) - 4/5  
Intel Confidential

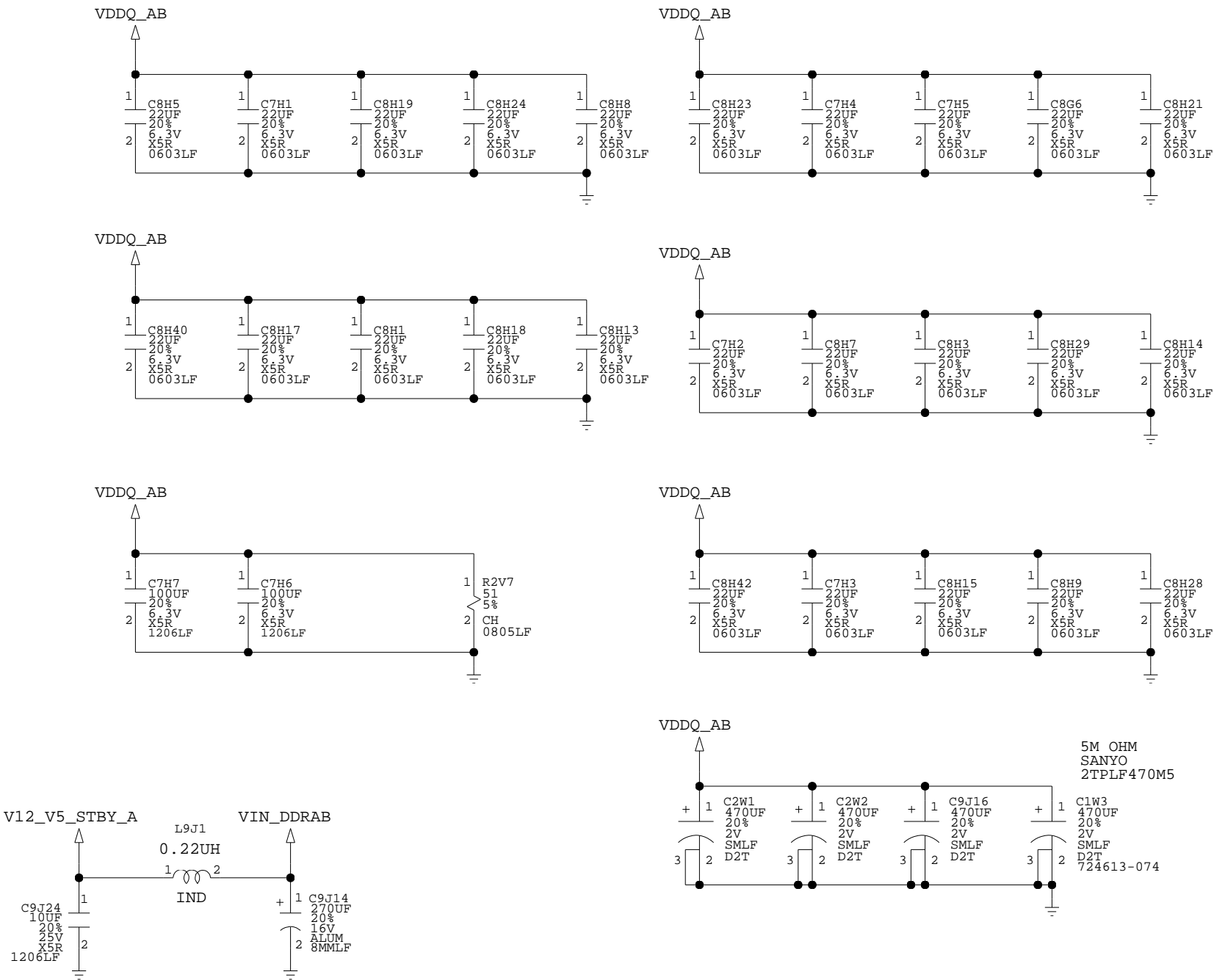
DOCUMENT NUMBER

E97822-100

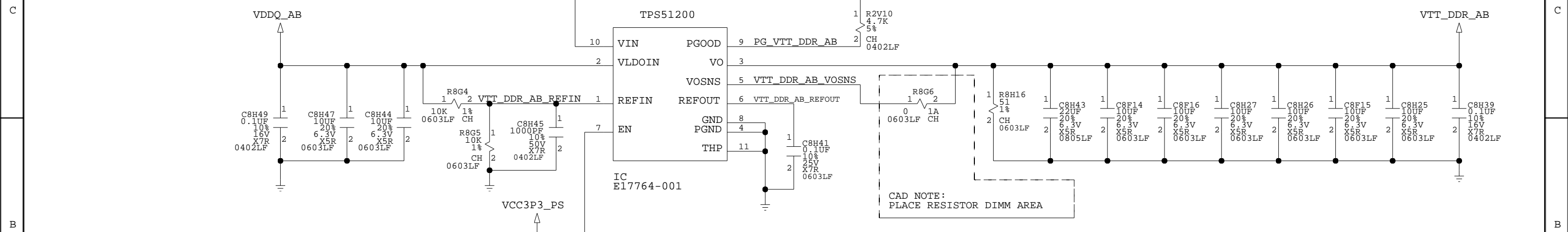
REV	
1.0	

SHEET 238 OF 315

DDR3 CHANNEL AB 5/5 - CPU0

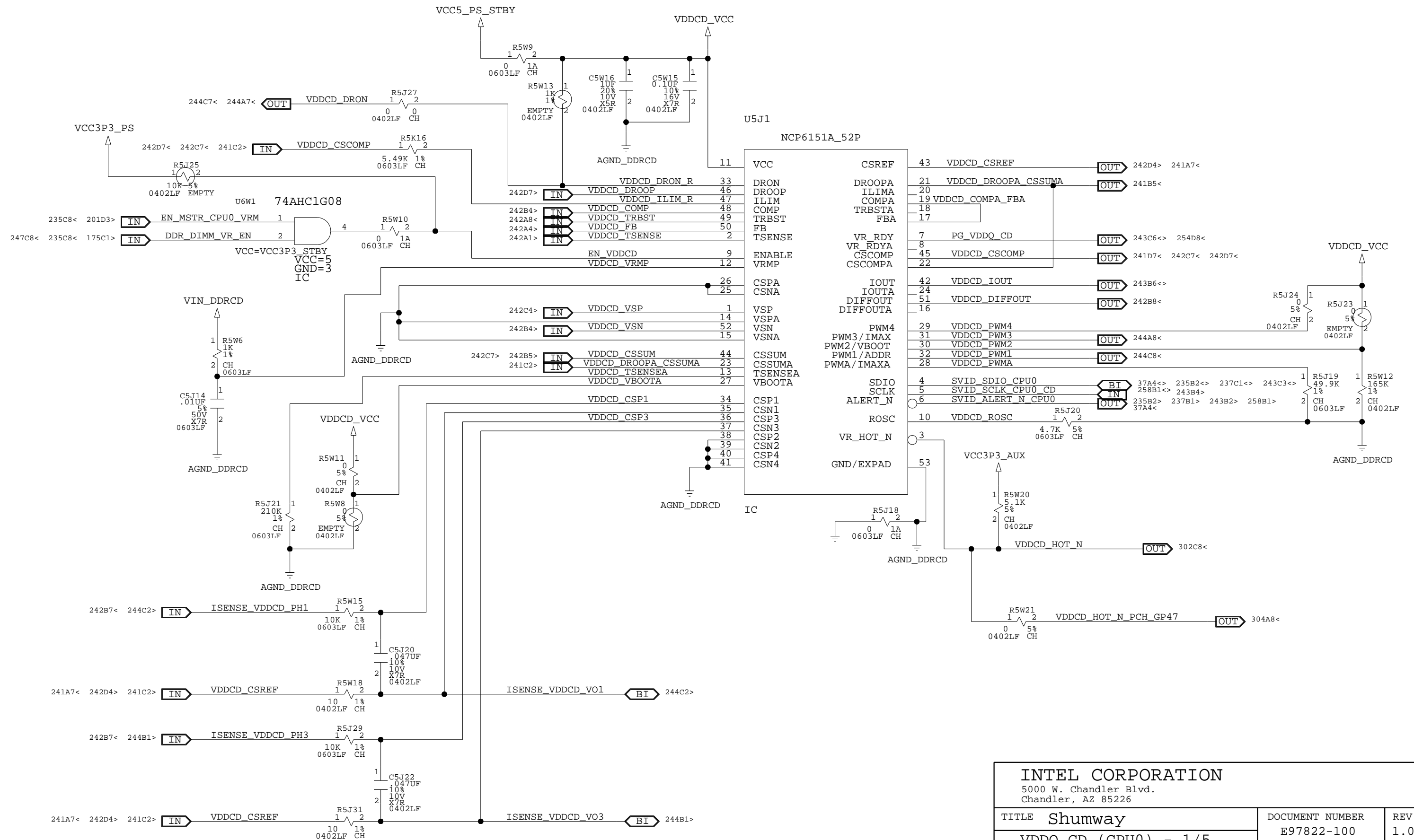


INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VDDQ_AB (CPU0) - 5/5 Intel Confidential	SHEET 239 OF 315	



<div>INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226</div>																							
TITLE    Shumway												DOCUMENT NUMBER E97822-100		REV 1.0									
VTT_DDR_AB (CPU0) Intel Confidential												SHEET 240 OF 315											
8			7			6			5			4			3			2			1		

## DDR3 CHANNEL CD 1/5 - CPU0



INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE	Shumway
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VDDQ\_CD (CPU0) - 1/5  
Intel Confidential

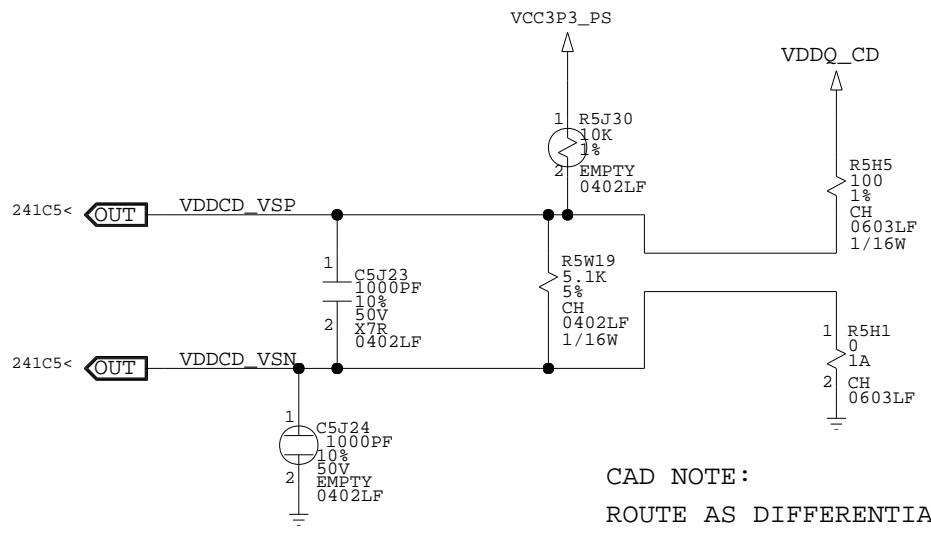
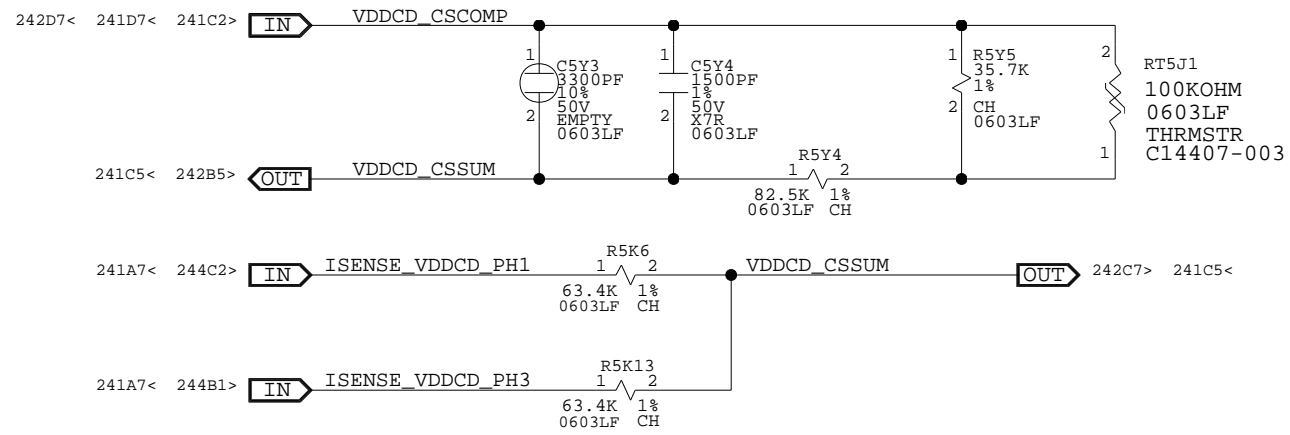
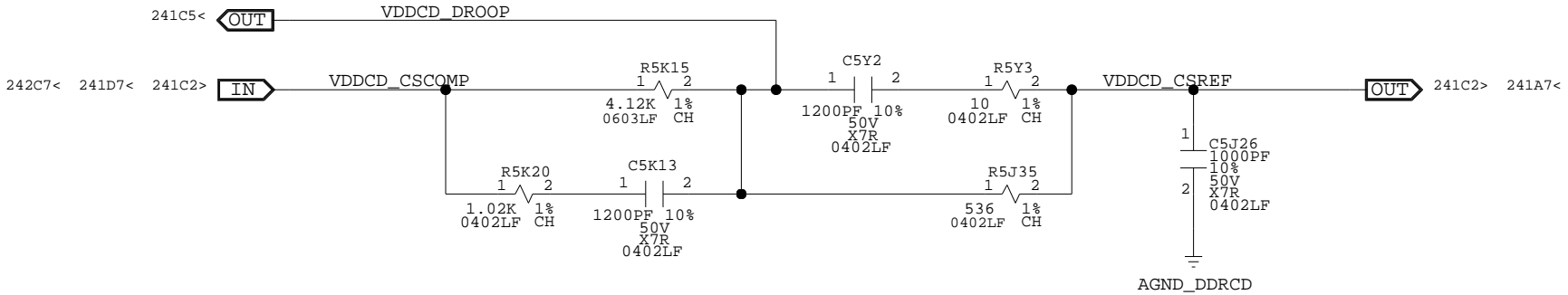
DOCUMENT NUMBER
-----------------

E97822-100

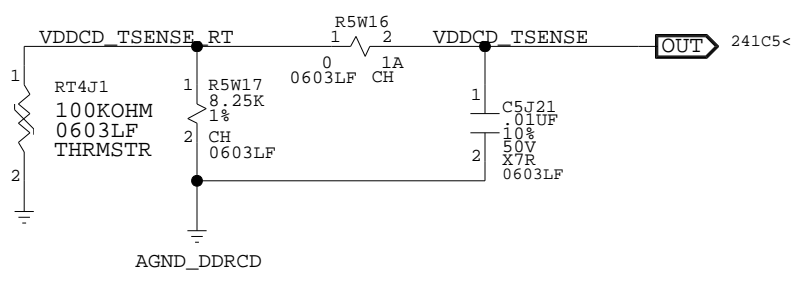
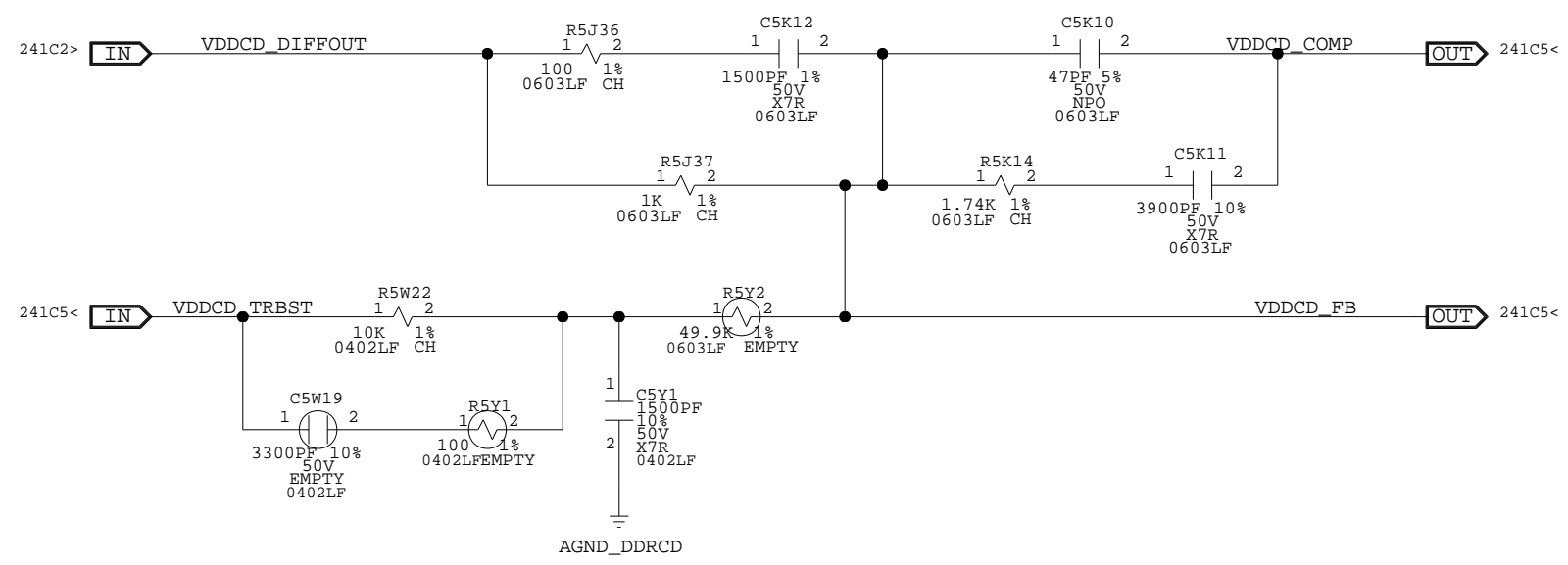
REV	
1.0	

SHEET 241 OF 315

DDR3 CHANNEL CD 2/5 - CPU0



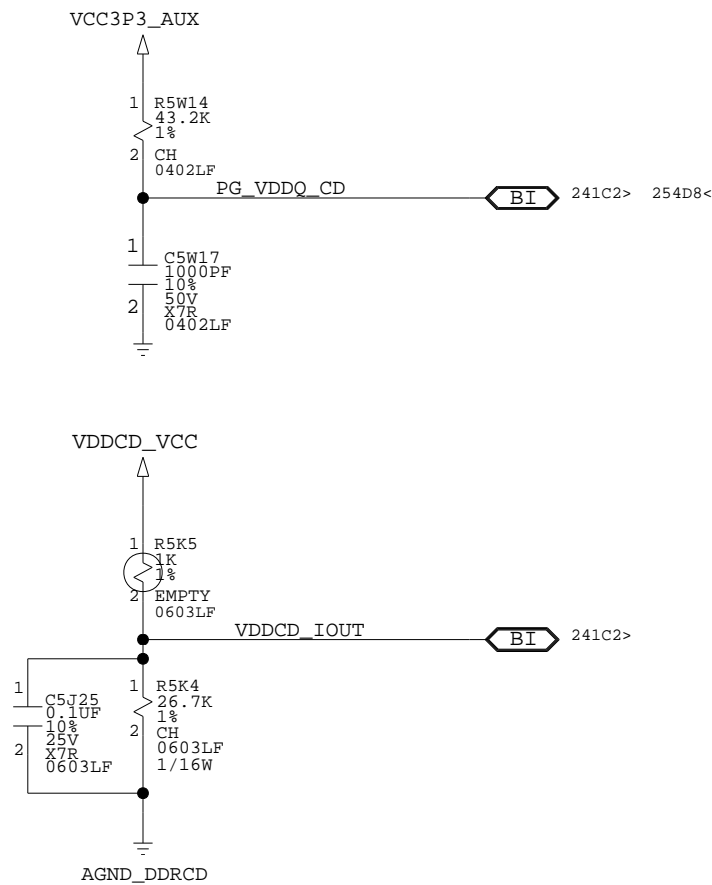
CAD NOTE:  
ROUTE AS DIFFERENTIAL PAIR



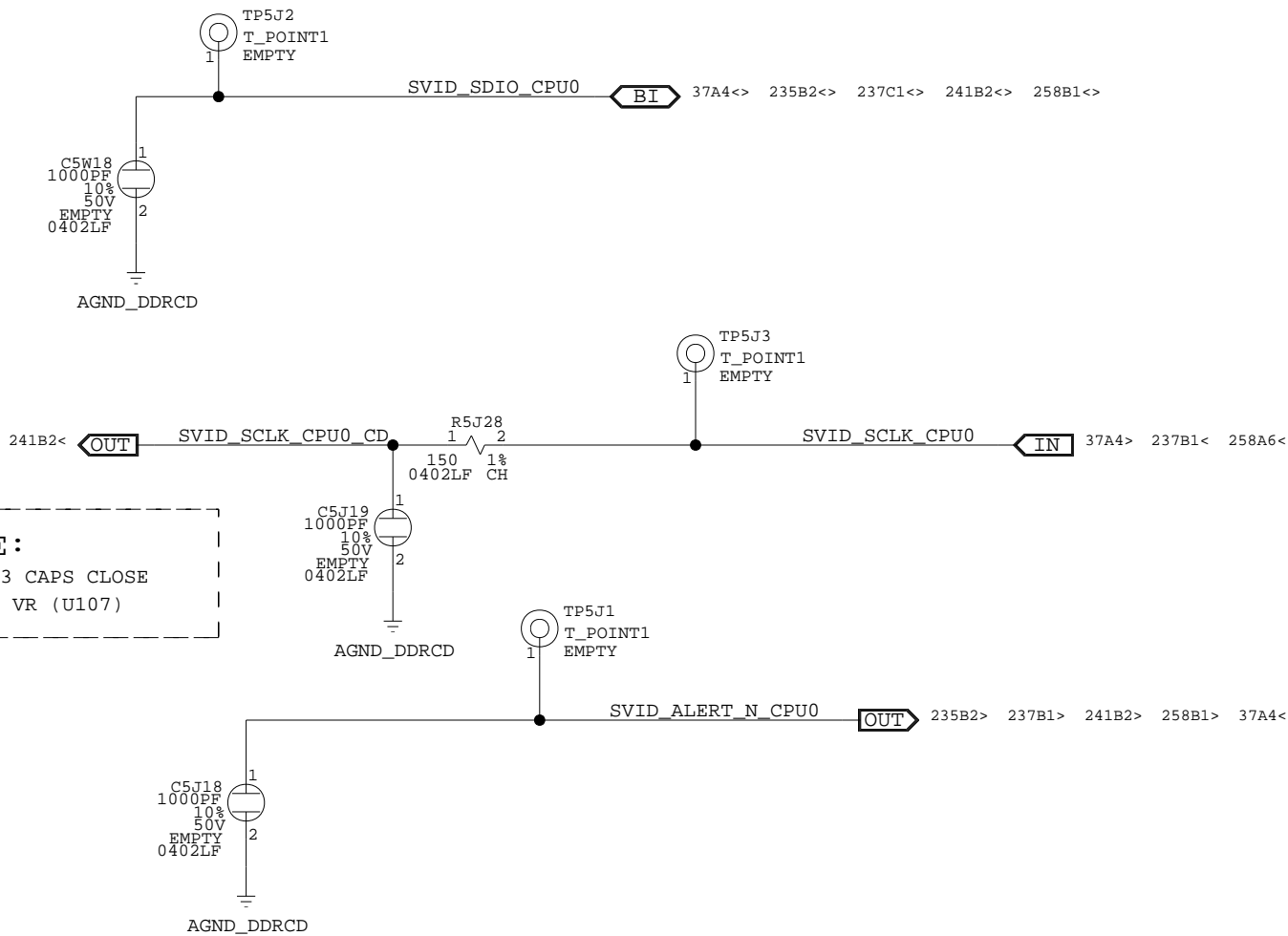
INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VDDQ_CD (CPU0) - 2/5 Intel Confidential	SHEET 242 OF 315	



DDR3 CHANNEL CD 3/5 - CPU0



CAD NOTE:  
PLACE THESE 3 CAPS CLOSE  
TO THE DDRCD VR (U107)



INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

VDDQ\_CD (CPU0) - 3/5  
Intel Confidential

DOCUMENT NUMBER

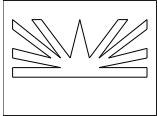
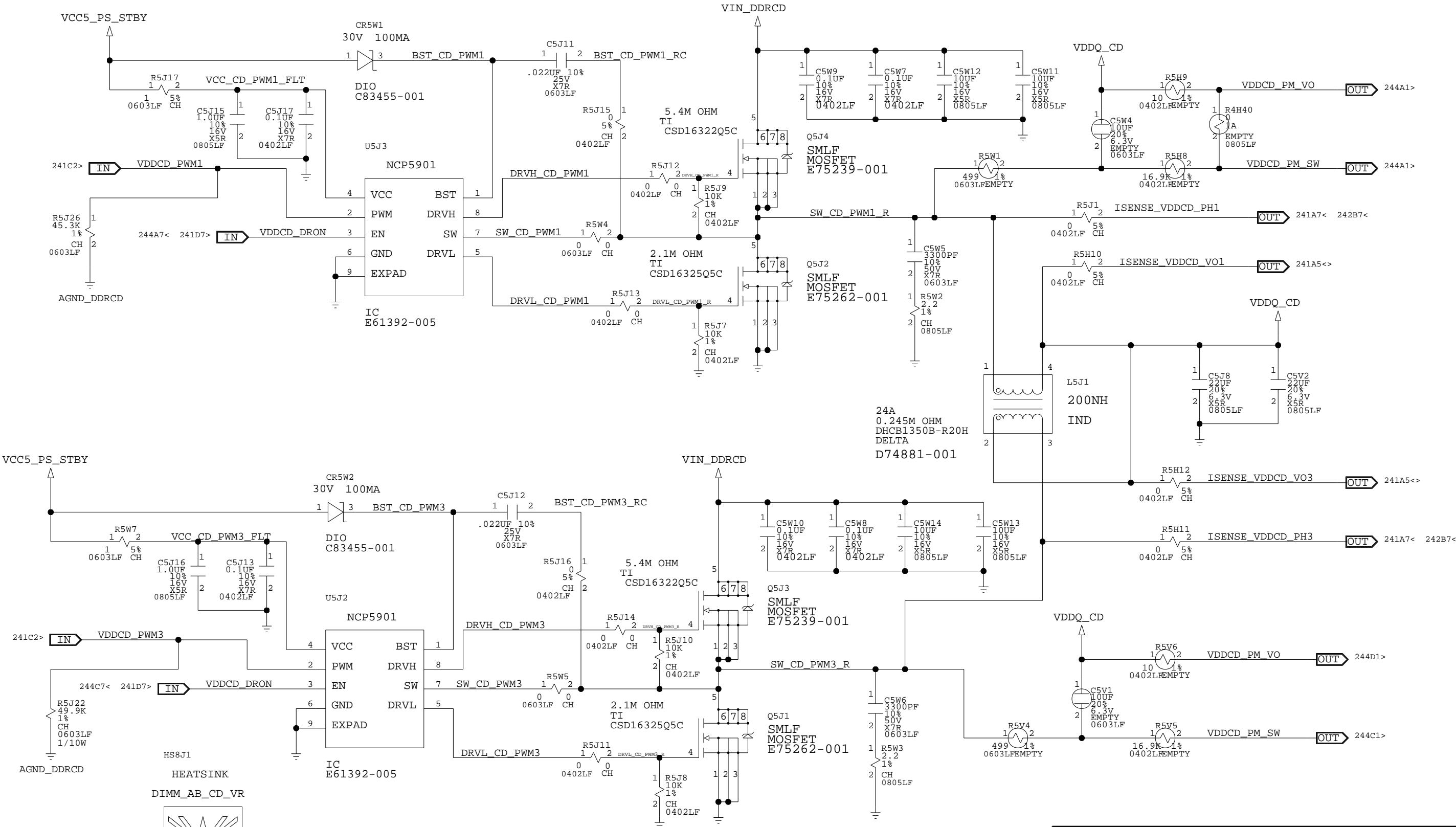
E97822-100

REV

1.0

SHEET 243 OF 315

DDR3 CHANNEL CD 4/5 - CPU0



HTSK  
E66260-001

INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

VDDQ\_CD (CPU0) - 4/5  
Intel Confidential

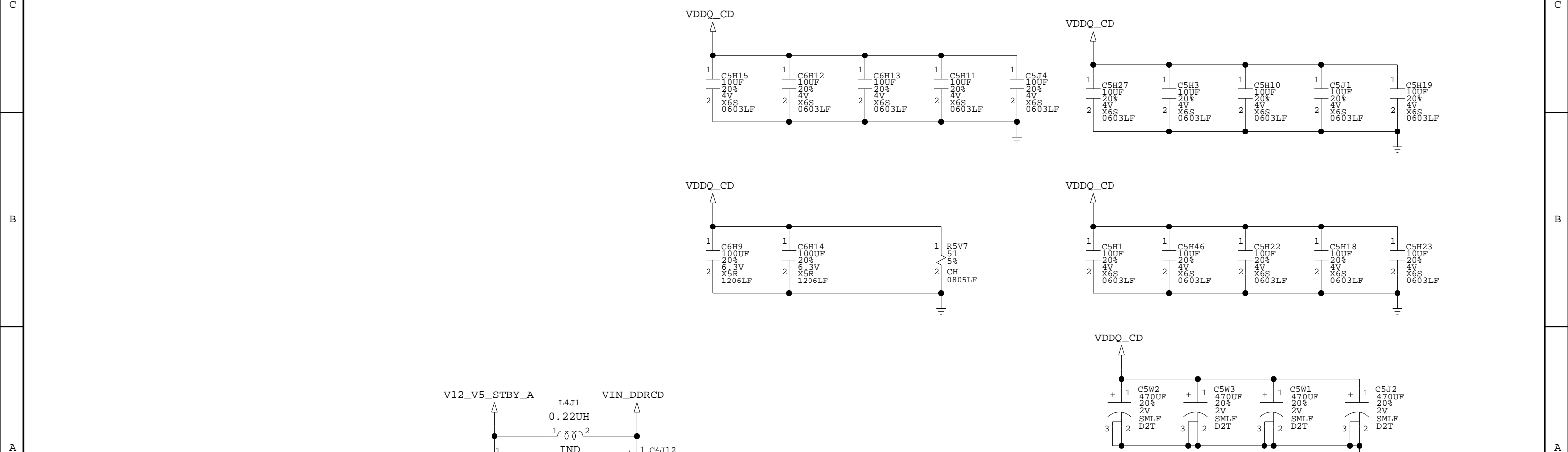
DOCUMENT NUMBER  
E97822-100

SHEET 244 OF 315

REV  
1.0

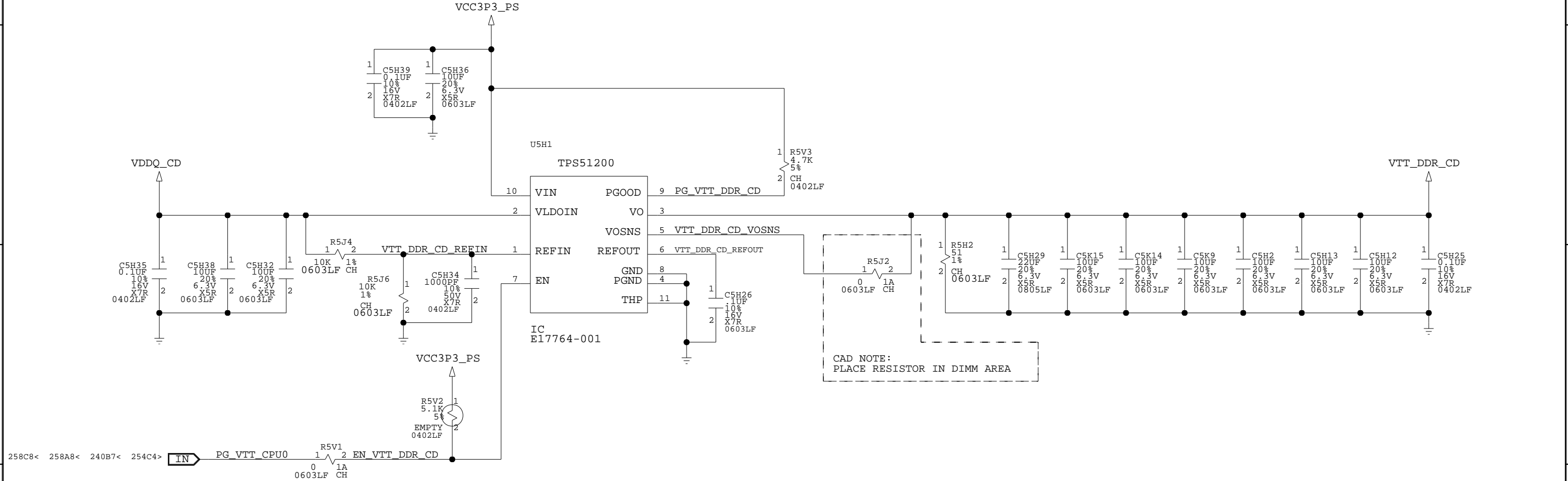
HEAT SINK REQUIRED ON FETS

D	DDRS3 CHANNEL CD 3/3 - CFB00	D
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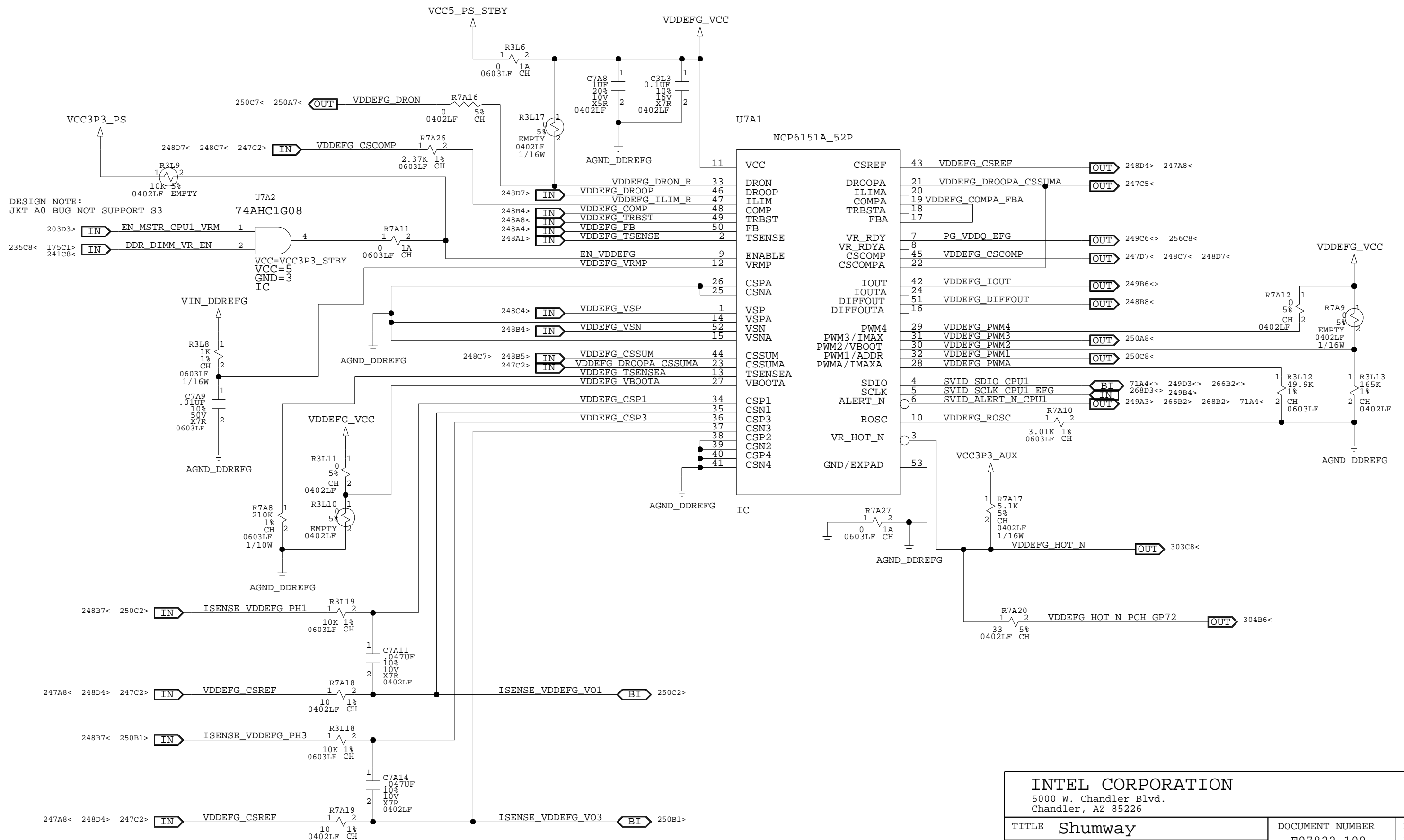
TITLE	Shumway	DOCUMENT NUMBER	REV
VDDQ_CD (CPU0) - 5/5		E97822-100	1.0
Intel Confidential		SHEET 245 OF 315	

VTT DDR CHANNEL CD - CPU0



INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE	Shumway	DOCUMENT NUMBER
VTT_DDR_CD (CPU0) Intel Confidential		E97822-100
		REV
		1.0
SHEET 246 OF 315		

DDR3 CHANNEL EFG 1/5 - CPU1



INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE	Shumway
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VDDQ\_EFG (CPU1) - 1/5  
Intel Confidential

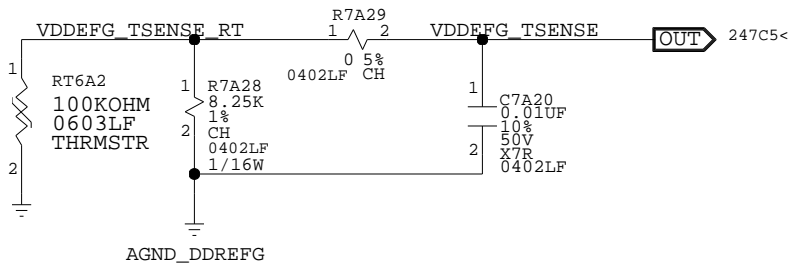
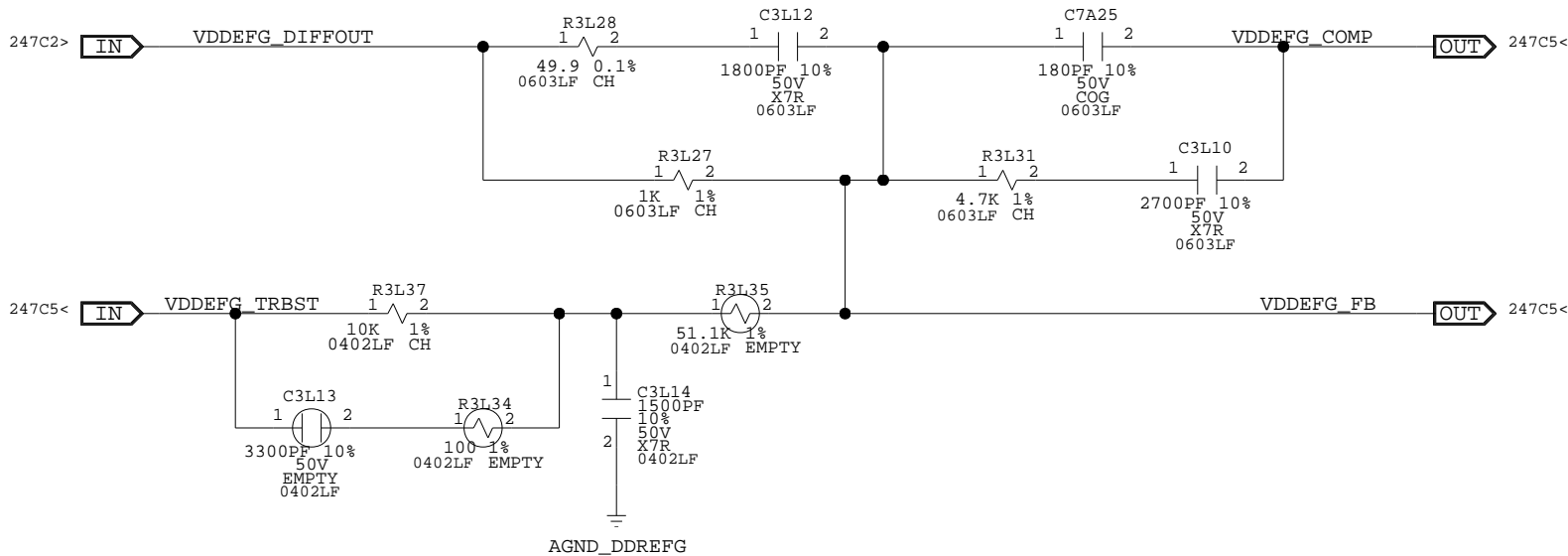
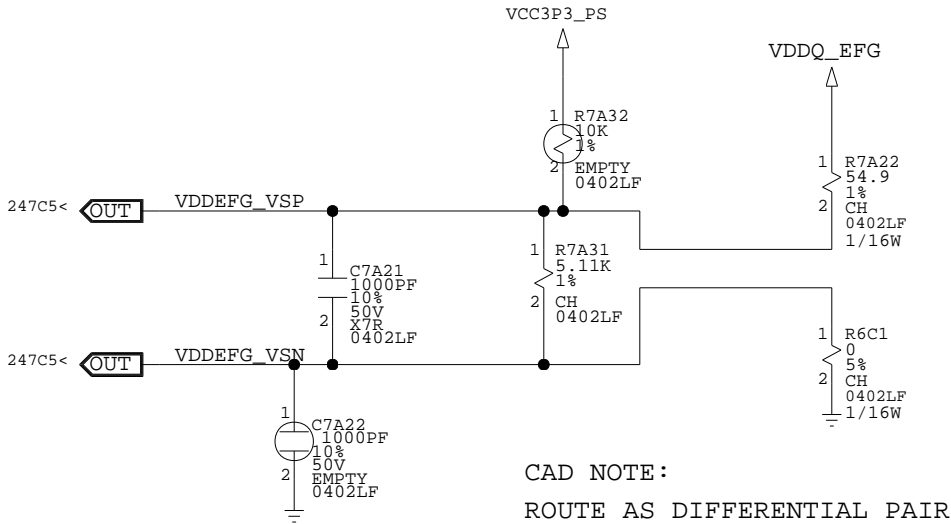
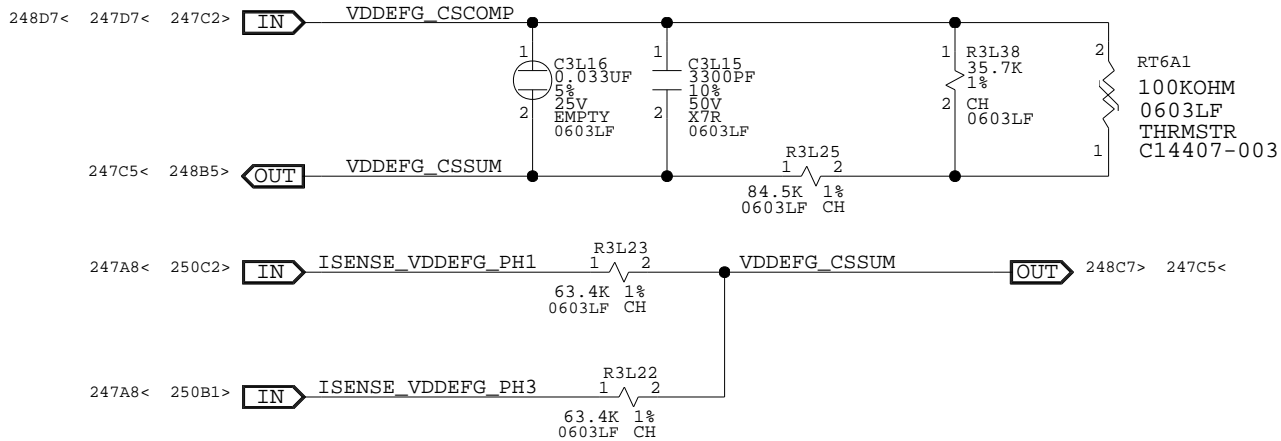
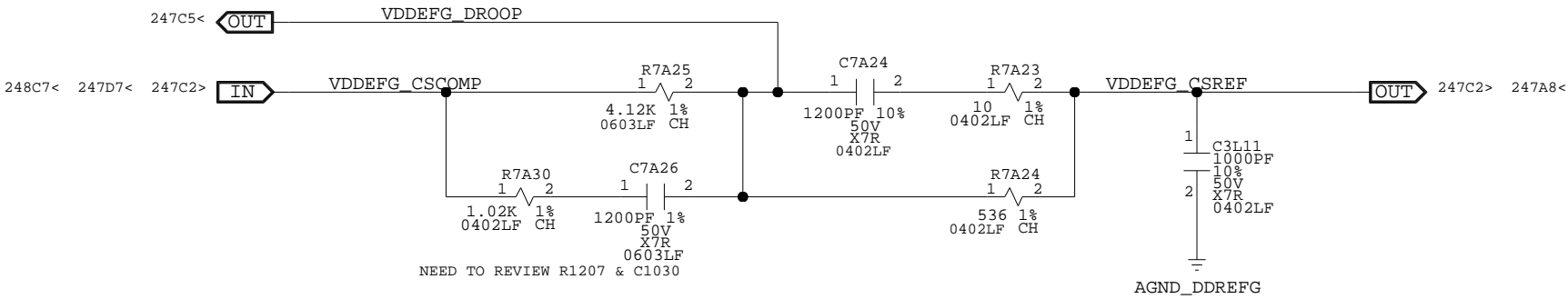
DOCUMENT NUMBER
-----------------

E97822-100

SHEET 247 OF 315

REV	
1.0	

DDR3 CHANNEL EFG 2/5 - CPU1



INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

VDDQ\_EFG (CPU1) - 2/5  
Intel Confidential

DOCUMENT NUMBER

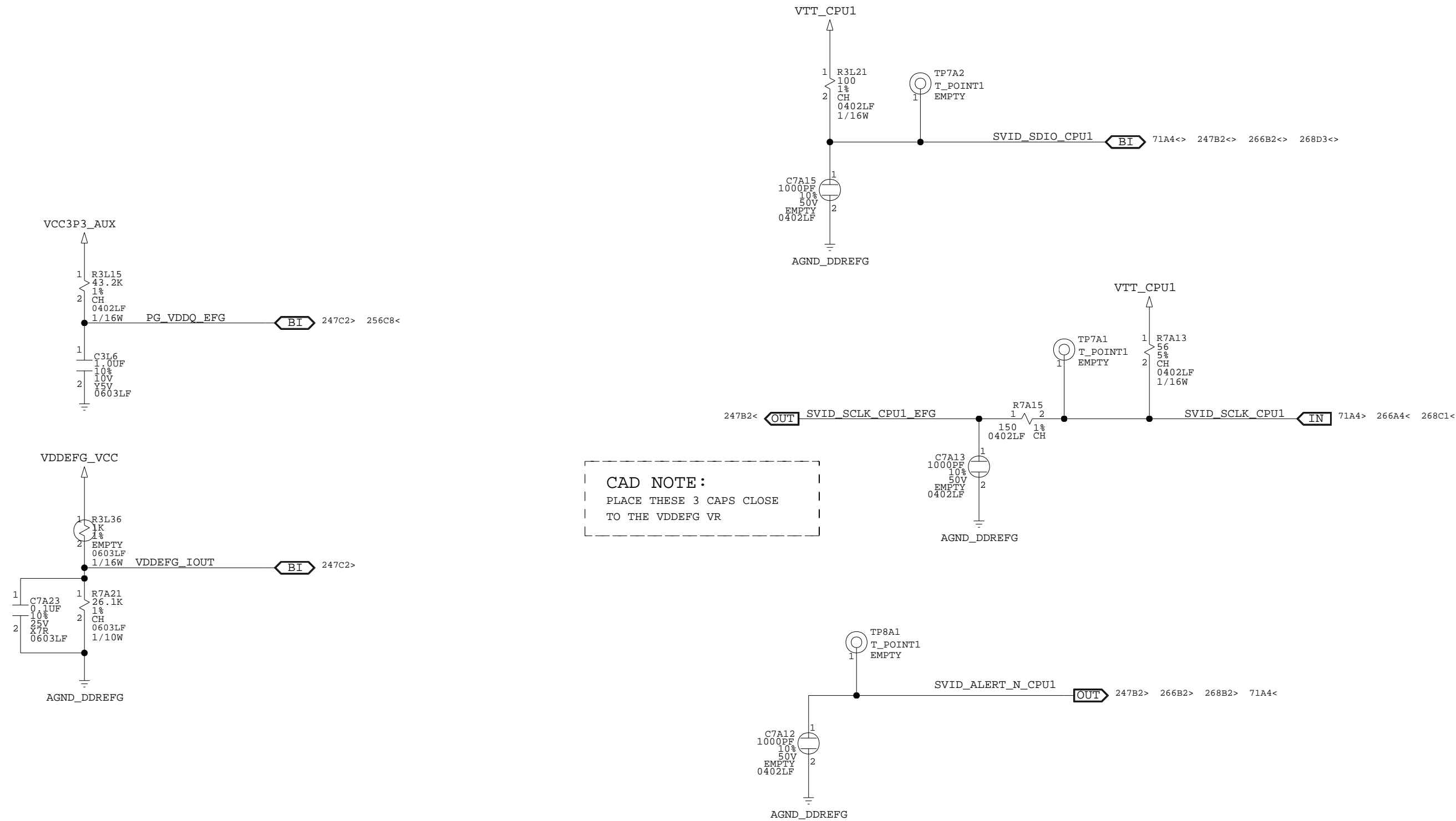
E97822-100

REV

1.0

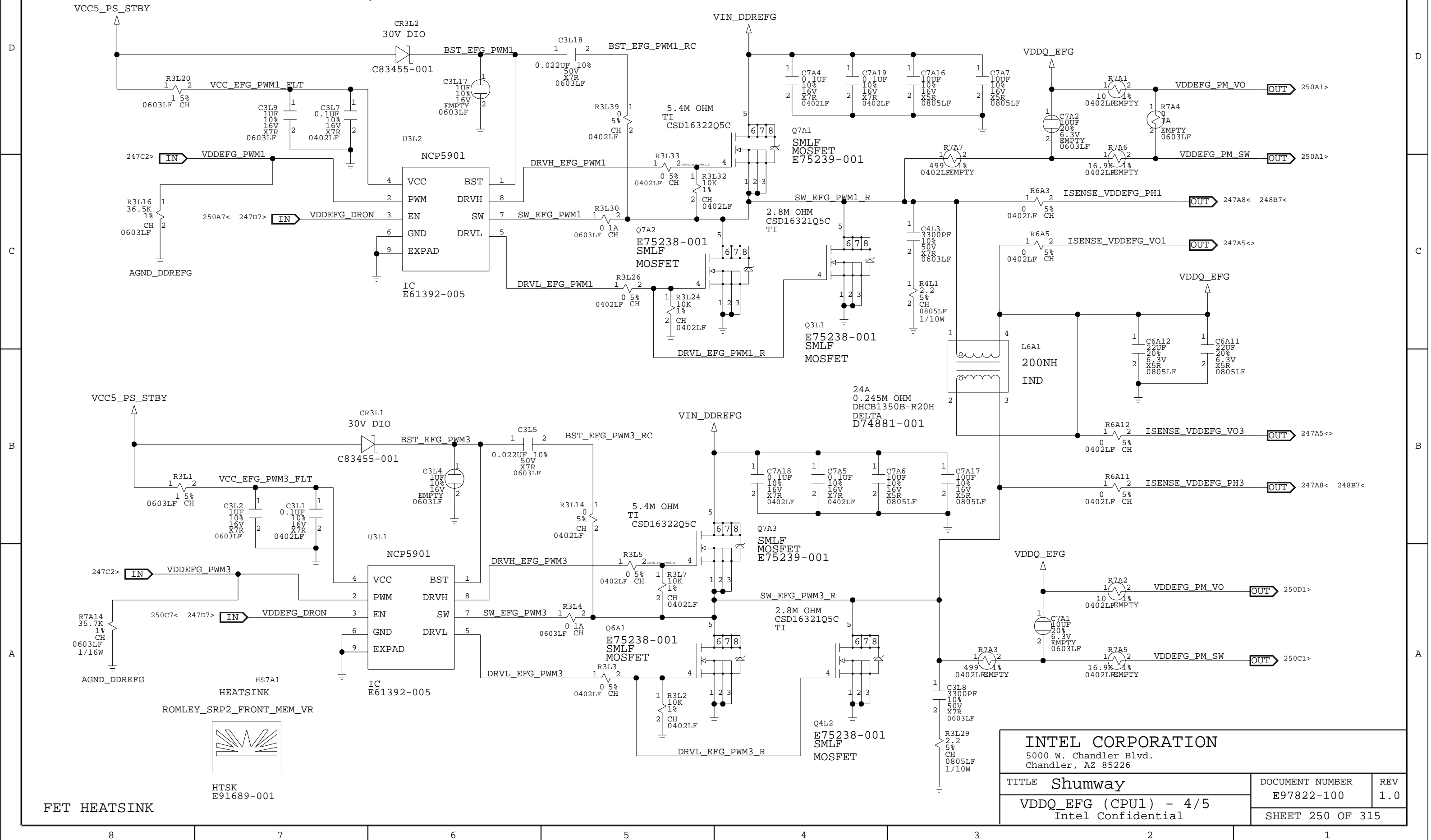
SHEET 248 OF 315

DDR3 CHANNEL EFG 3/5 - CPU1



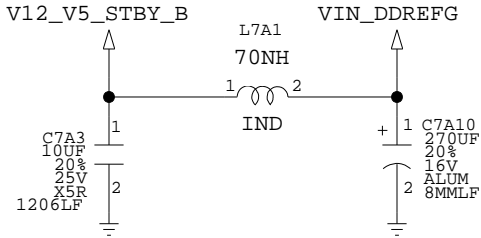
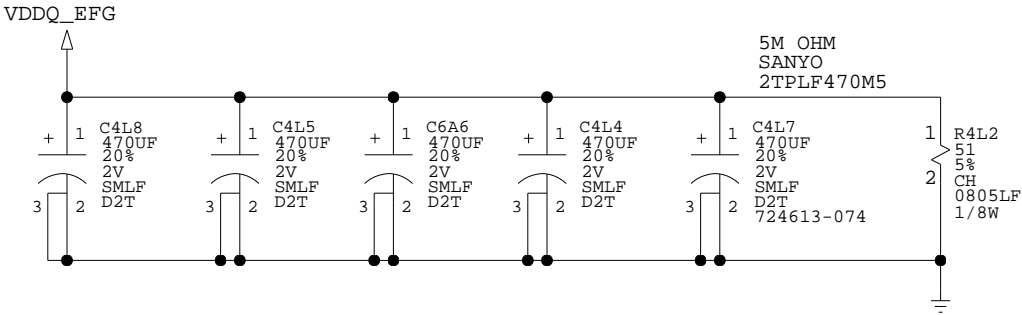
INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VDDQ_EFG (CPU1) - 3/5 Intel Confidential	SHEET 249 OF 315	

## DDR3 CHANNEL EFG 4/5 - CPU1

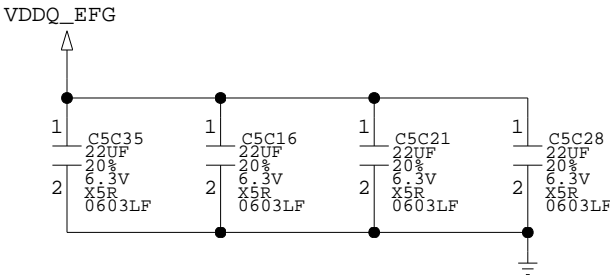




DDR3 CHANNEL EFG 5/5 - CPU1

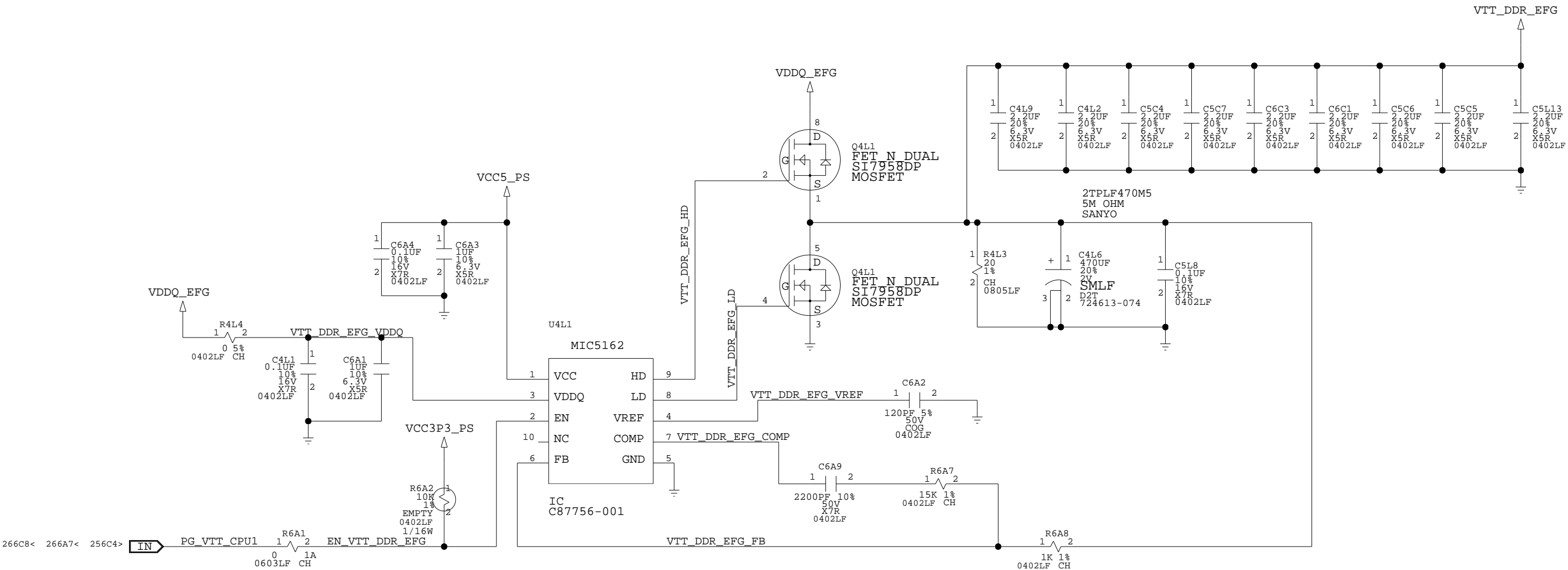


INPUT FILTER



INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VDDQ_EFG (CPU1) - 5/5 Intel Confidential	SHEET 251 OF 315	

VTT\_DDR\_CHANNEL\_EFG - CPU1



INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE Shumway

VTT\_DDR\_EFG (CPU1)  
Intel Confidential

DOCUMENT NUMBER

E97822-100

REV

1.0

SHEET 252 OF 315

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

# CPU0 AND CPU1 POWER SUPPLY

INTEL CORPORATION

5000 W. Chandler Blvd.  
Chandler, AZ 85226

TITLE	Shumway
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DOCUMENT NUMBER  
E97822-100

REV
1.0

PAGE TITLE  
Intel Confidential

SHEET 253 OF 315

8

7

6

5

4

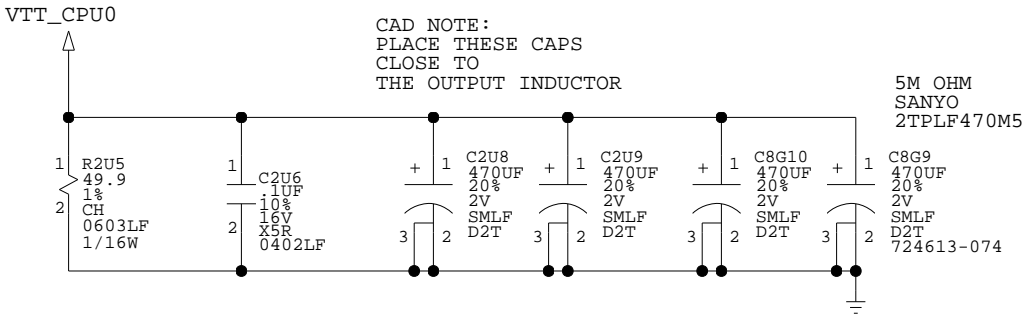
3

2

1

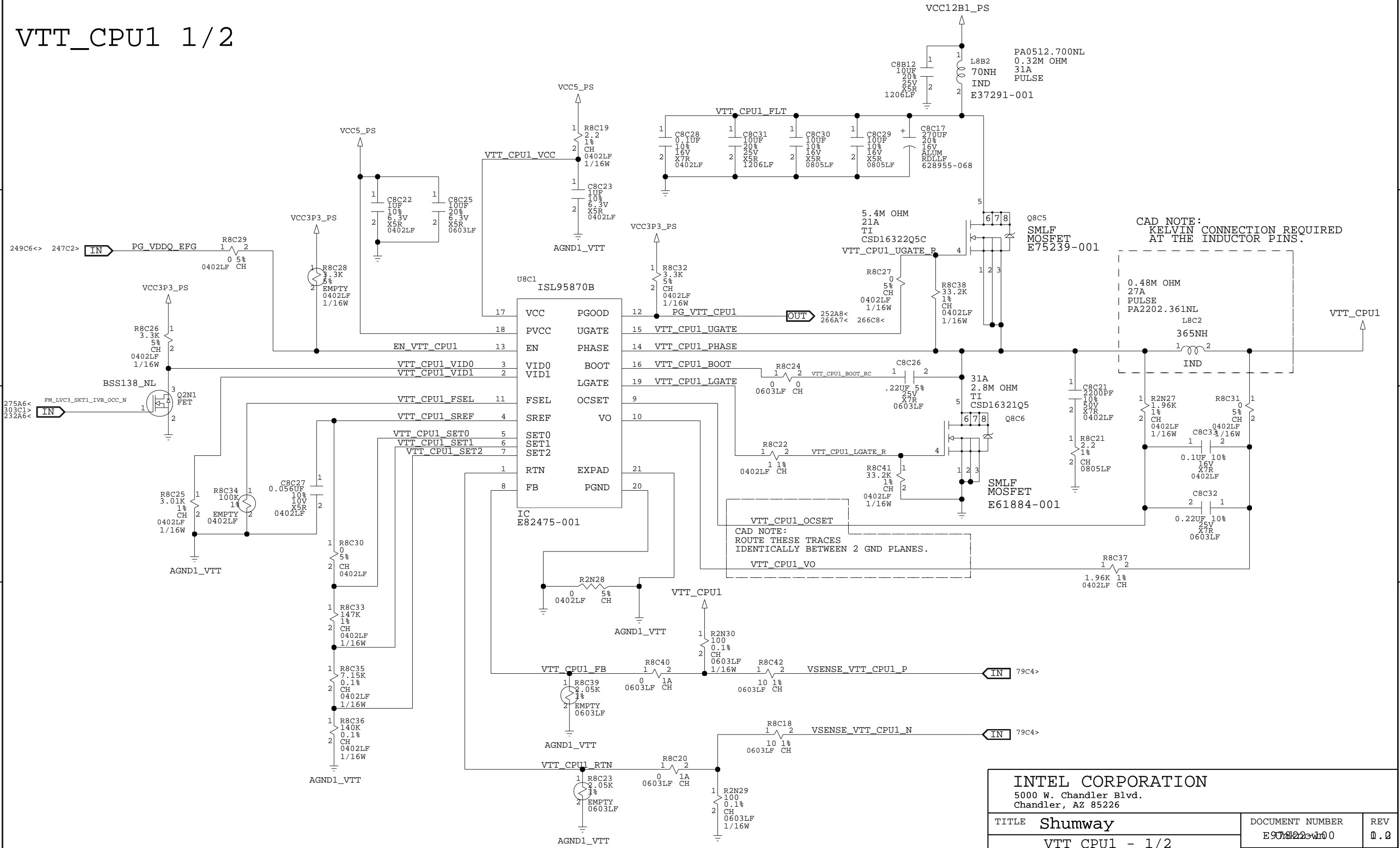


VTT\_CPU0 2 / 2

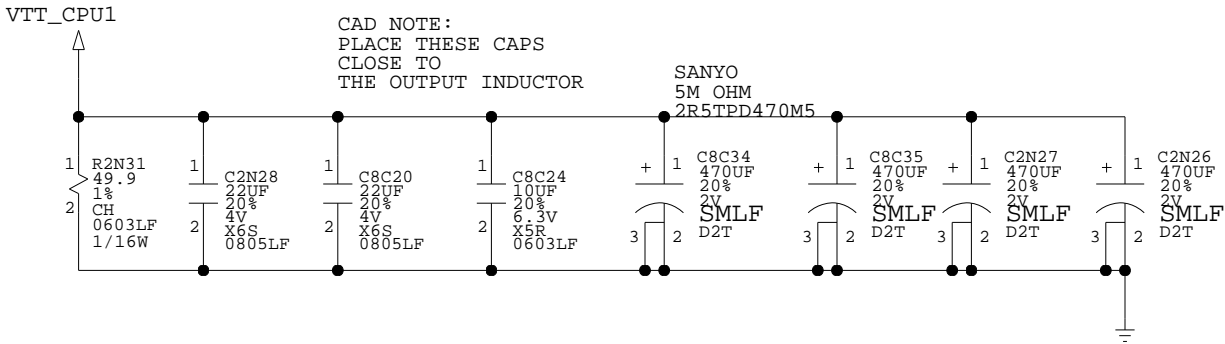


INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VTT_CPU0 - 2/2 Intel Confidential		SHEET 255 OF 315

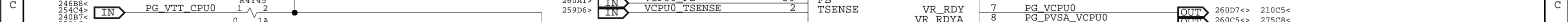
VTT\_CPU1 1/2



VTT\_CPU1 2/2



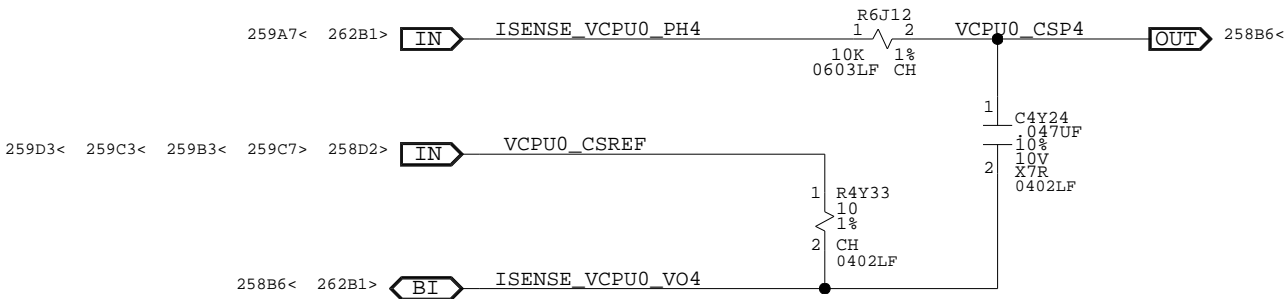
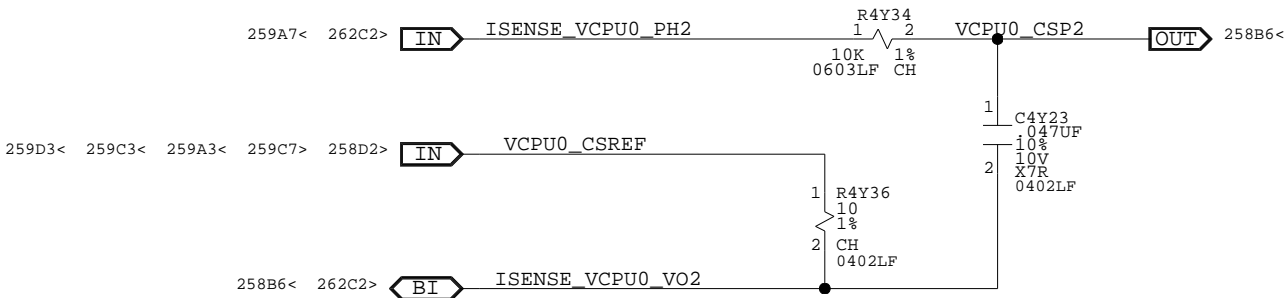
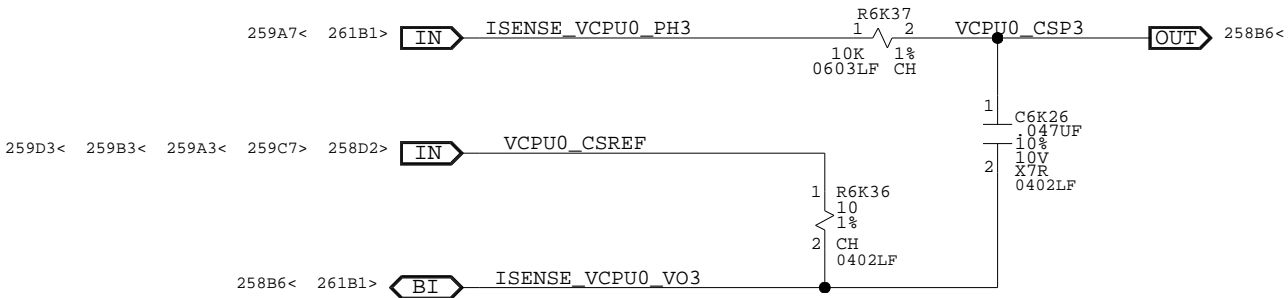
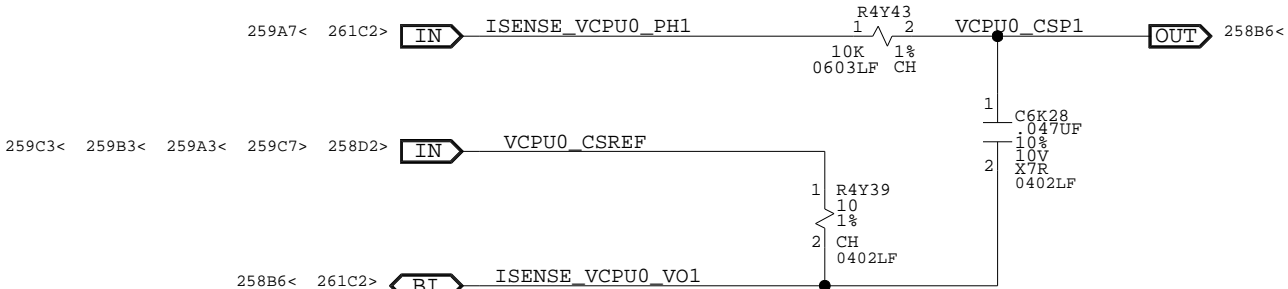
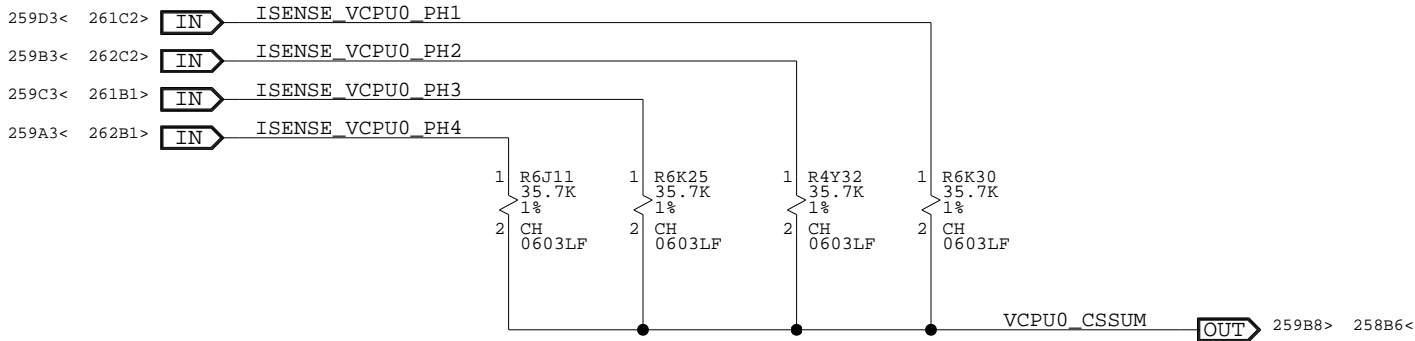
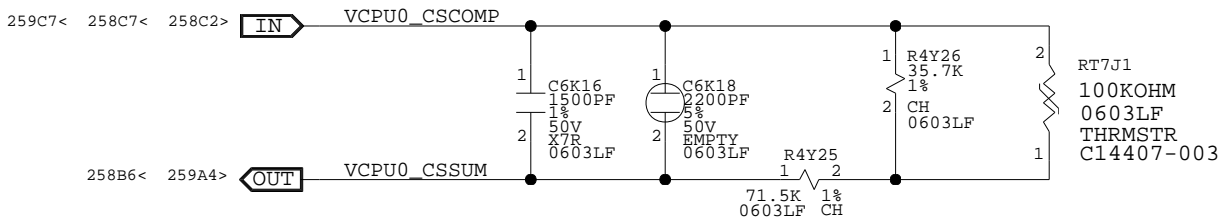
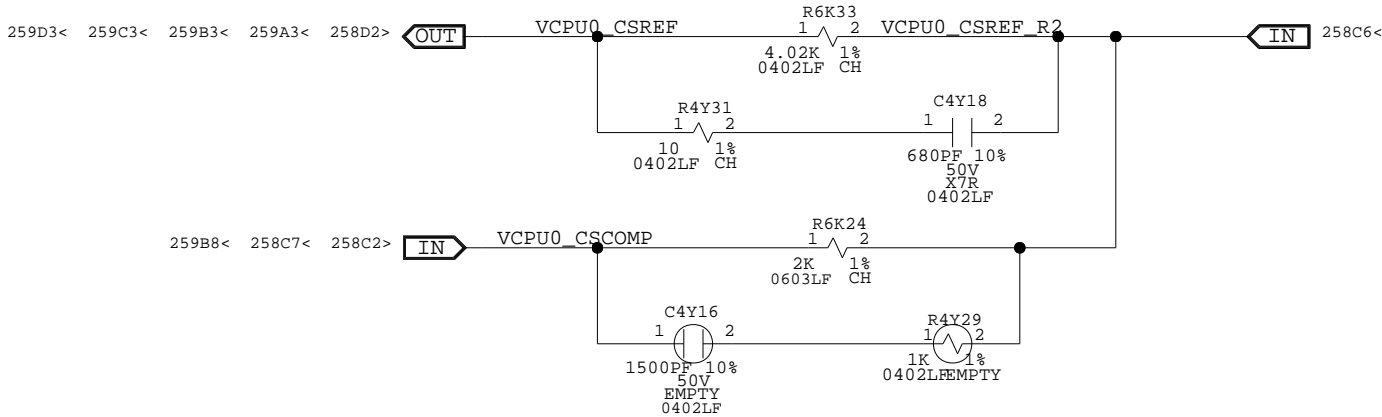
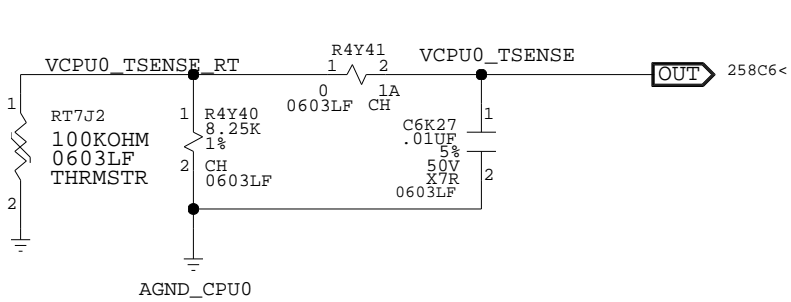
INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE	Shumway	DOCUMENT NUMBER
VTT_CPU1 - 2/2 Intel Confidential		REV
		0.2
		SHEET 257 OF 315



TITLE	Shumway	DOCUMENT NUMBER	REV
VCC_CPU0/VCCSA_CPU0-1/8		E97822-100	1.0
Intel Confidential	SHEET 258 OF 315		

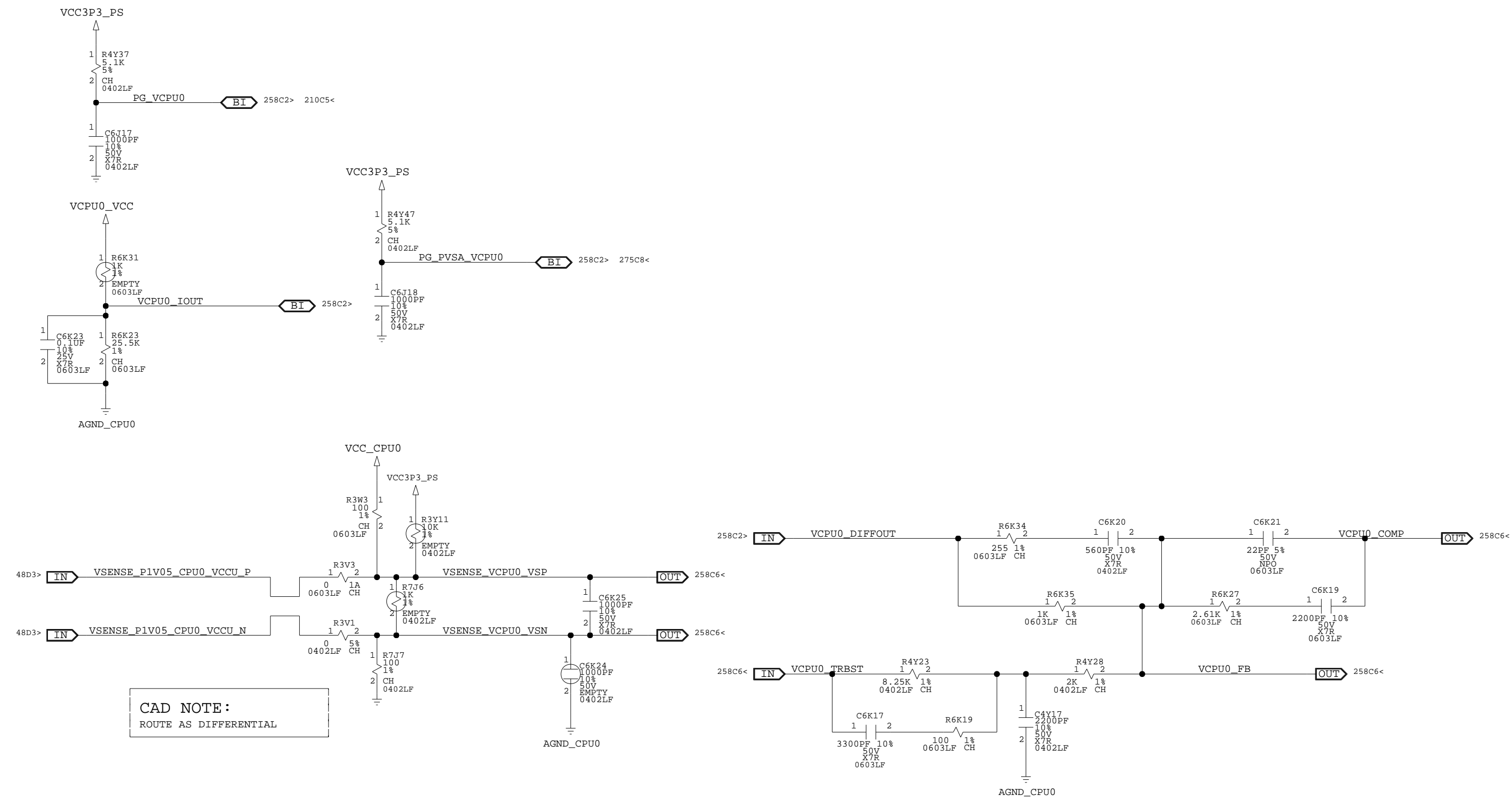


VCC\_CPU0 AND VCCSA\_CPU0 2/8

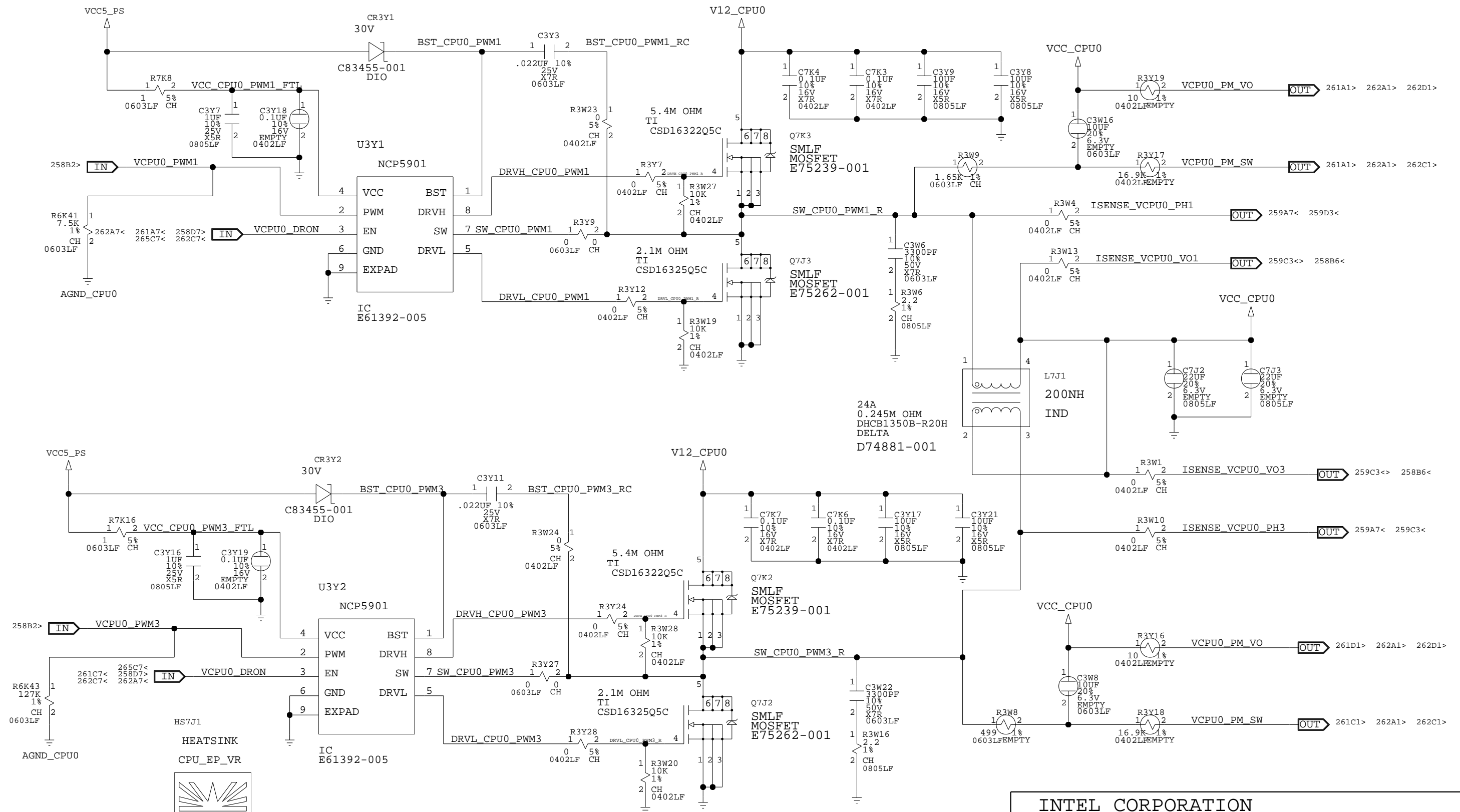


INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VCC_CPU0/VCCSA_CPU0-2/8 Intel Confidential	SHEET 259 OF 315	

VCC\_CPU0 AND VCCSA\_CPU0 3/8



VCC\_CPU0 AND VCCSA\_CPU0 4 / 8



HEAT SINK REQUIRED ON FETS

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VCC\_CPU0/VCCSA\_CPU0-4/8  
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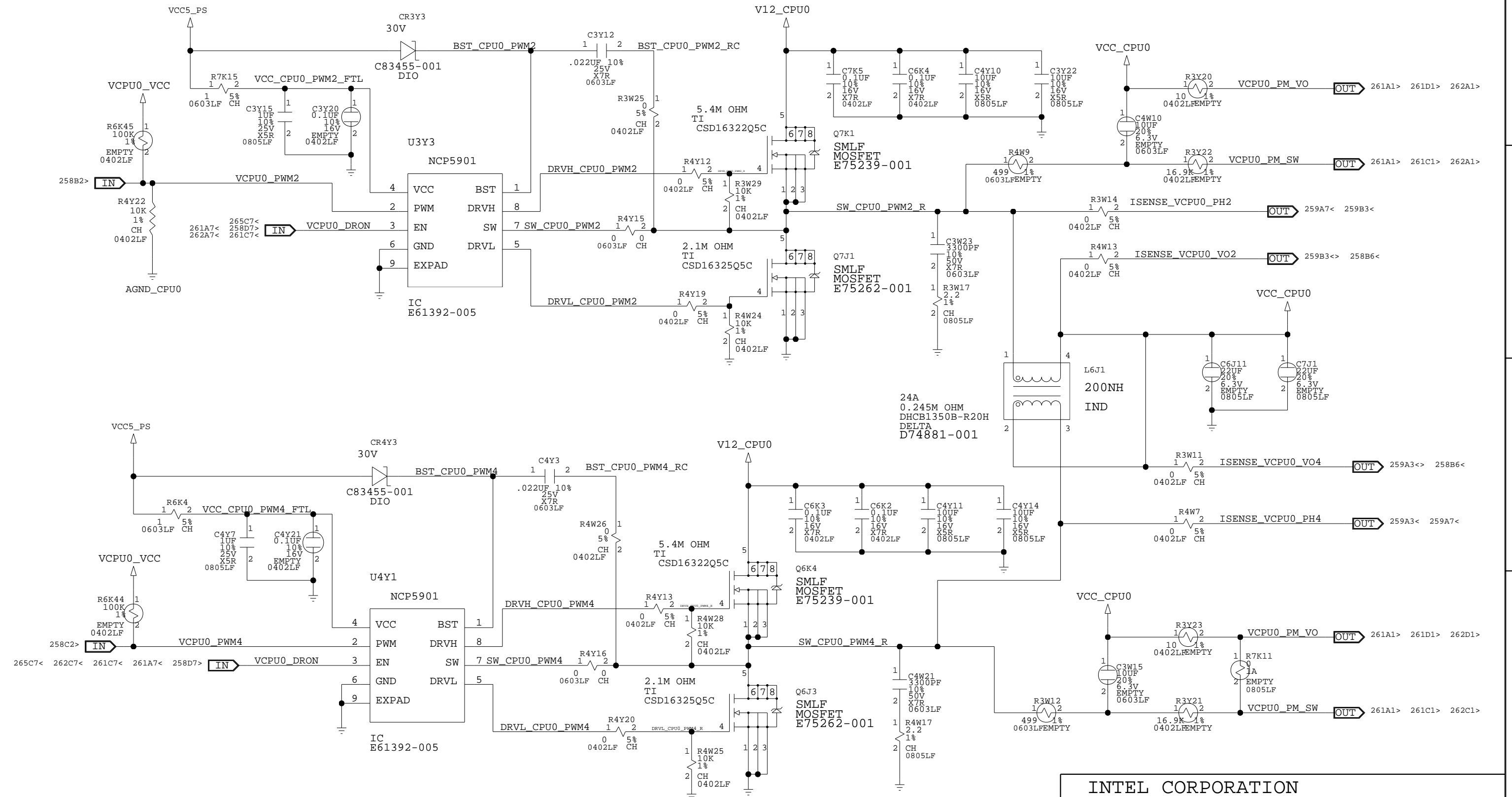
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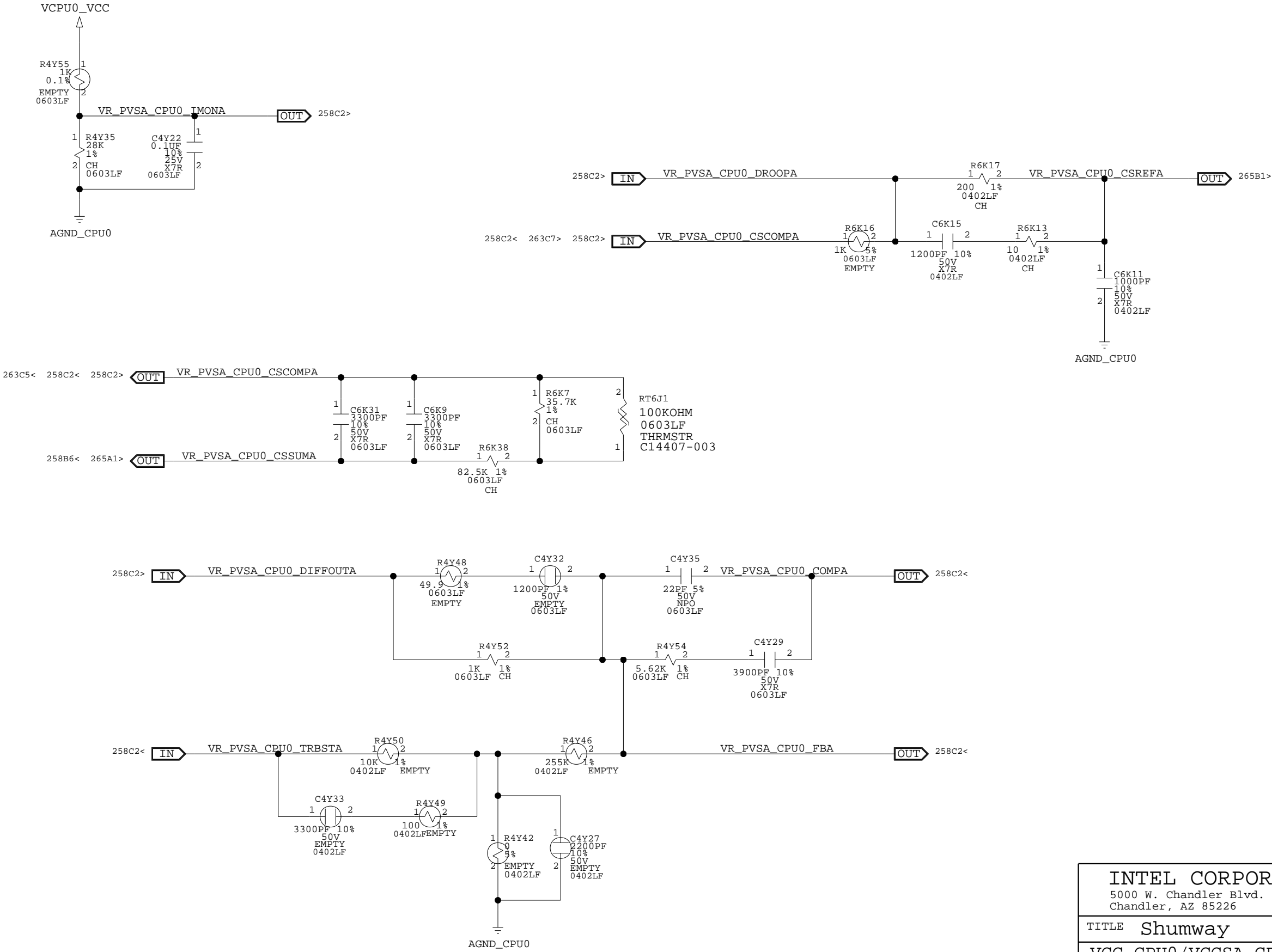
SHEET 261 OF 315
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VCC\_CPU0 AND VCCSA\_CPU0 5/8



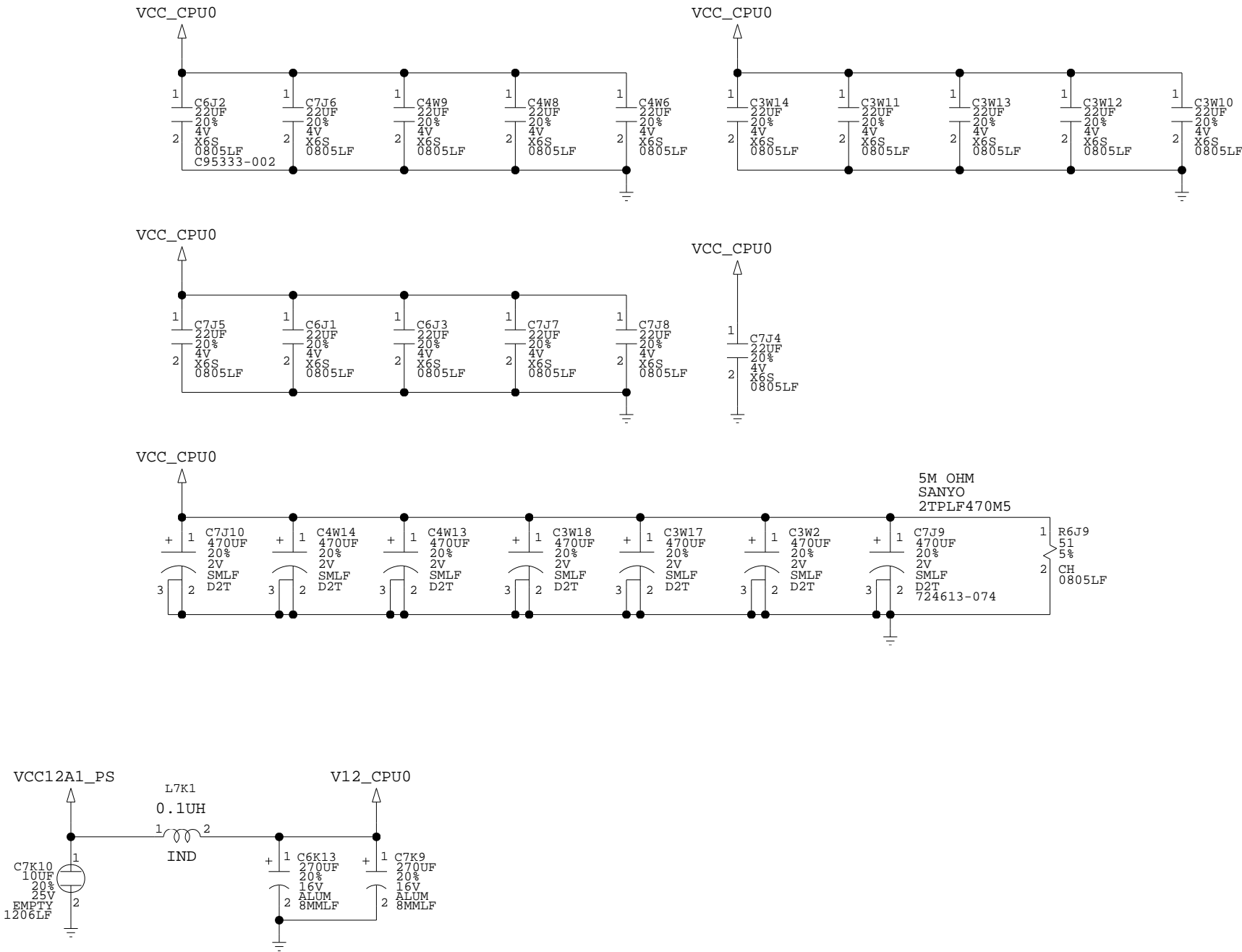
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VCC_CPU0/VCCSA_CPU0-5/8 Intel Confidential	SHEET 262 OF 315	

VCC\_CPU0 AND VCCSA\_CPU0 6/8

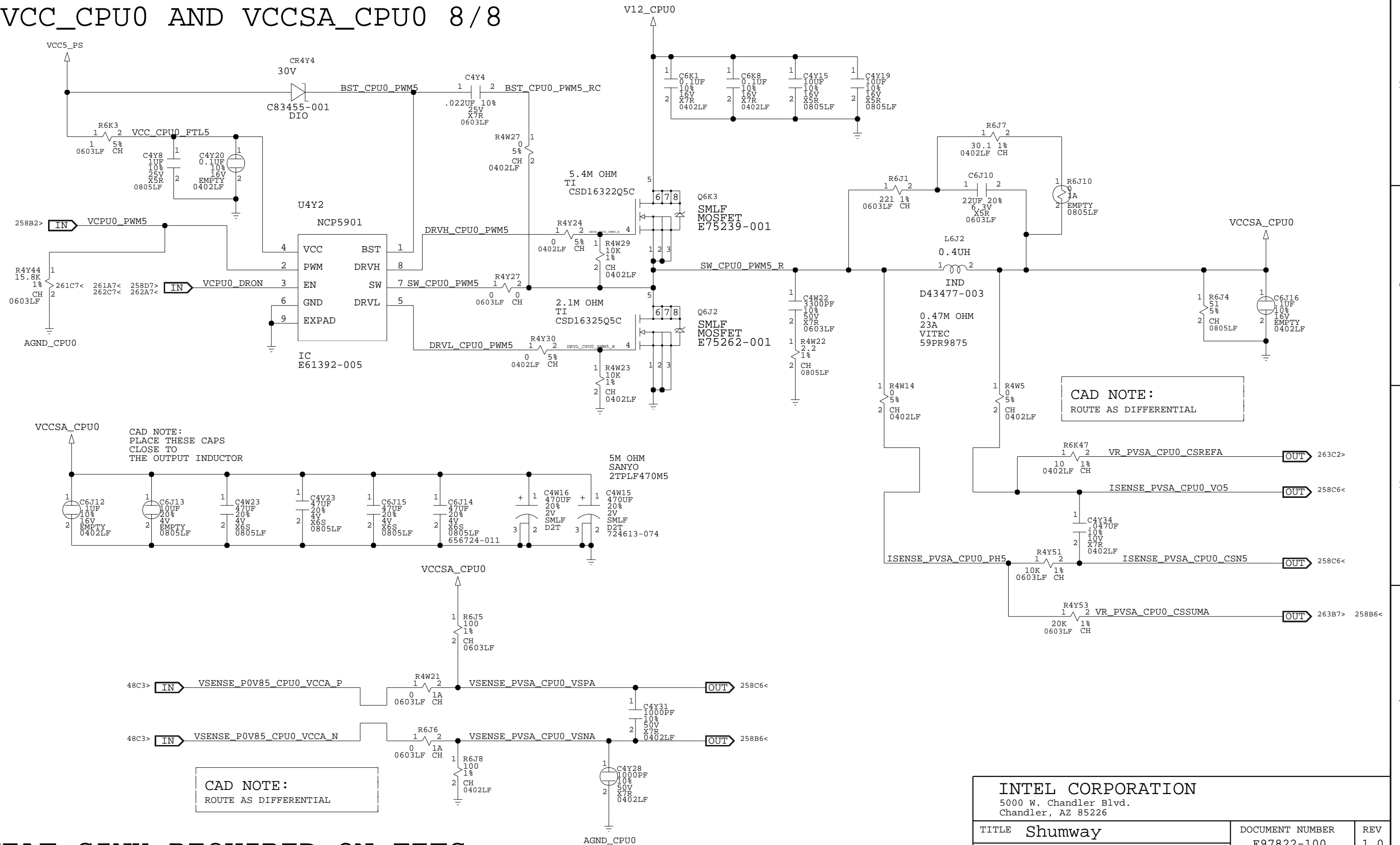


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TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VCC_CPU0/VCCSA_CPU0-6/8 Intel Confidential	SHEET 263 OF 315	

VCC\_CPU0 AND VCCSA\_CPU0 7/8



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VCC_CPU0/VCCSA_CPU0-7/8 Intel Confidential	SHEET 264 OF 315	



## HEAT SINK REQUIRED ON FETS

INTEL CORPORATION

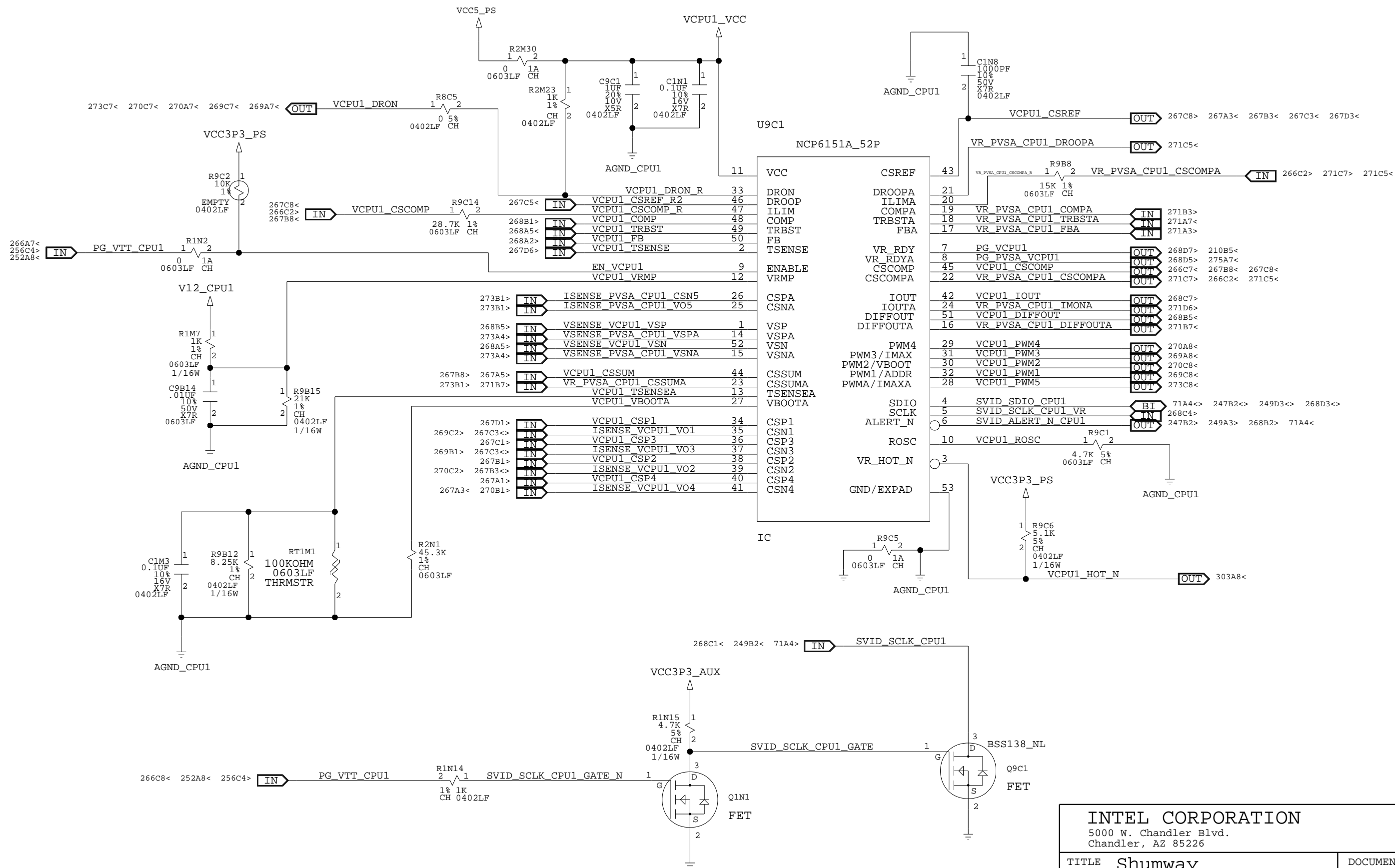
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VCC\_CPU1 AND VCCSA\_CPU1 1/8



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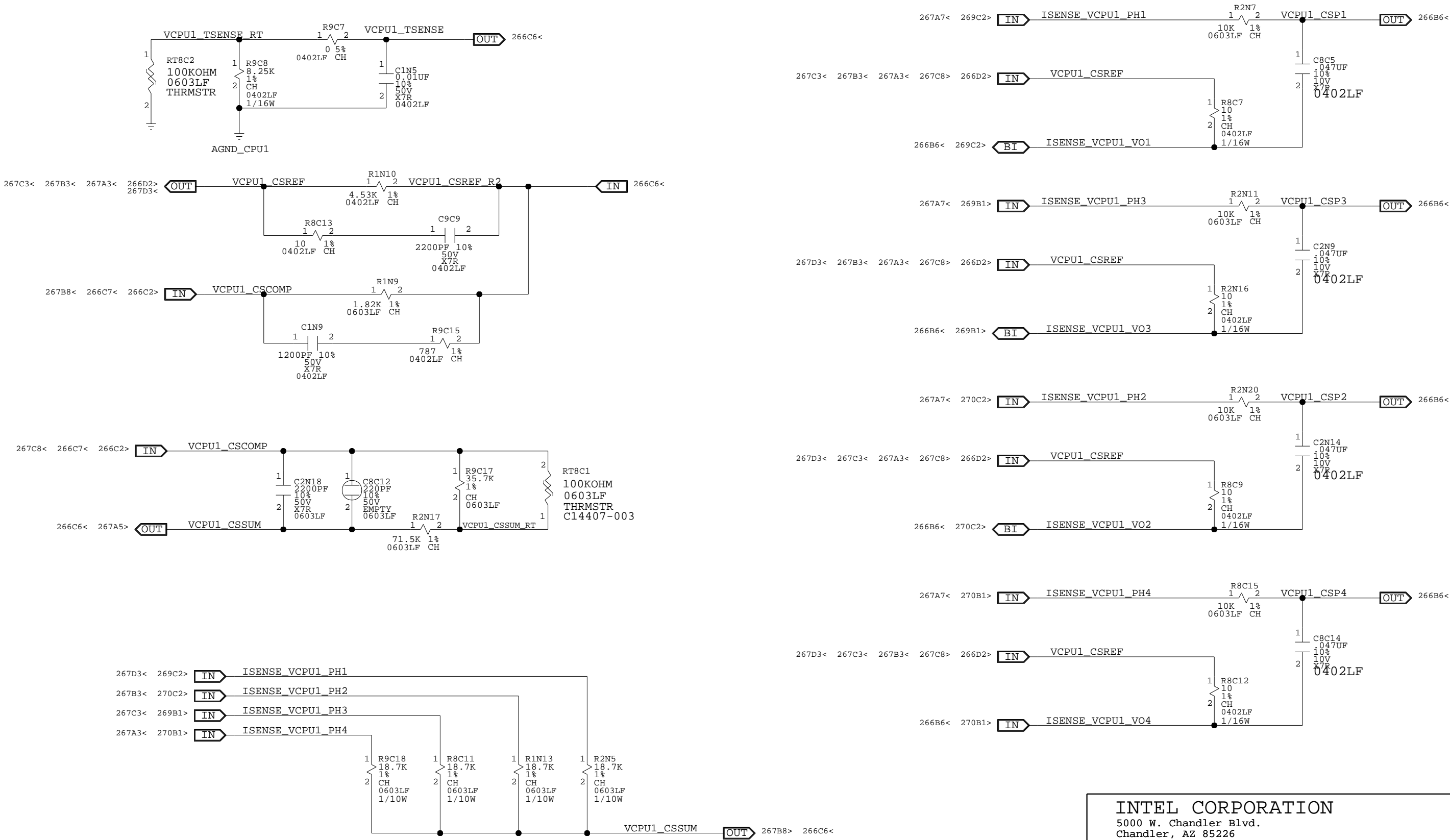
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VCC\_CPU1/VCCSA\_CPU1-1/8  
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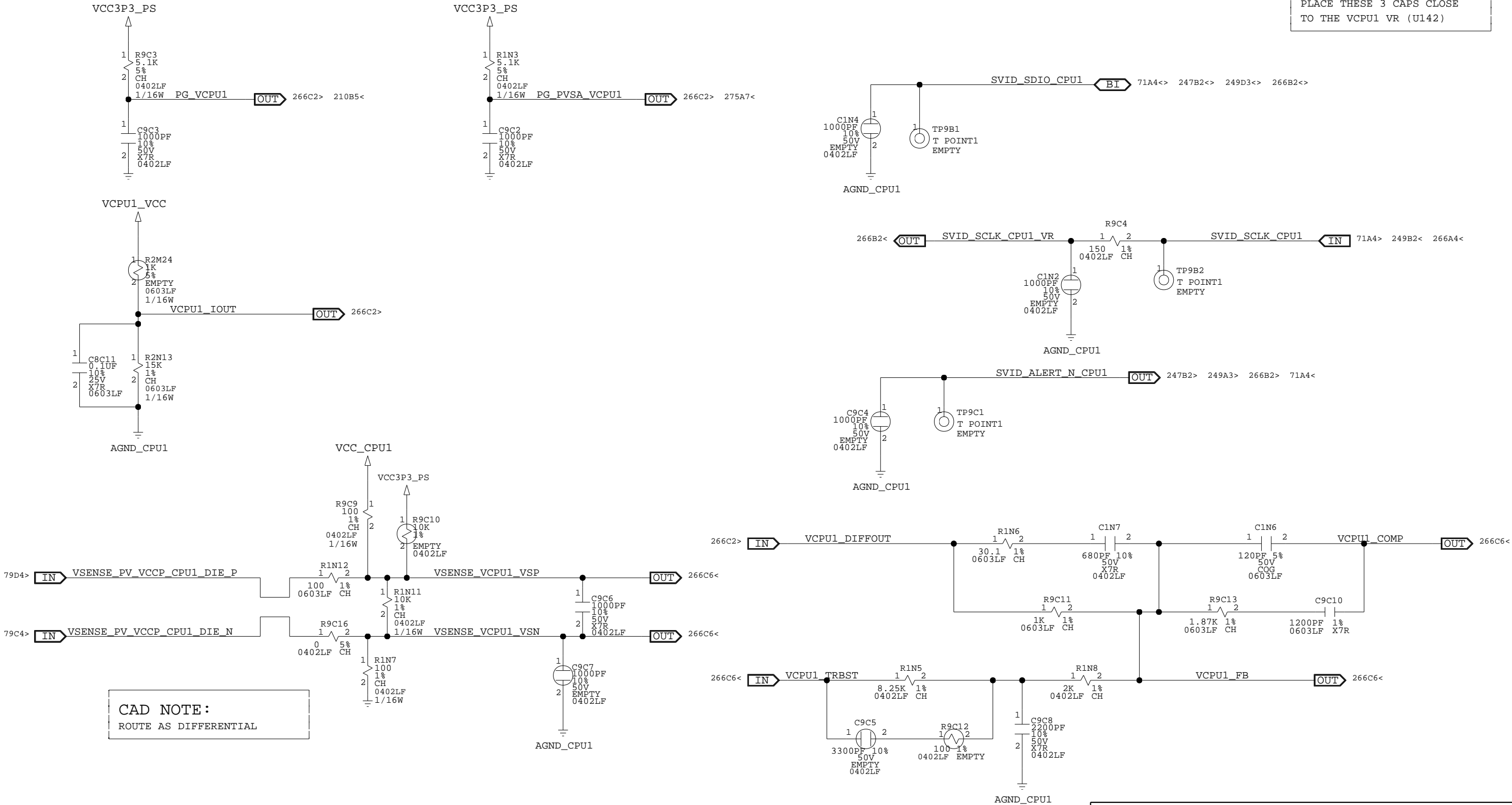


VCC\_CPU1 AND VCCSA\_CPU1 2/8



VCC\_CPU1 AND VCCSA\_CPU1 3/8

CAD NOTE :  
PLACE THESE 3 CAPS CLOSE  
TO THE VCPU1 VR (U142)



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VCC\_CPU1/VCCSA\_CPU1-3/8  
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VCC\_CPU1 AND VCCSA\_CPU1 4/8

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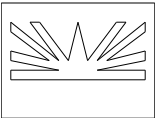
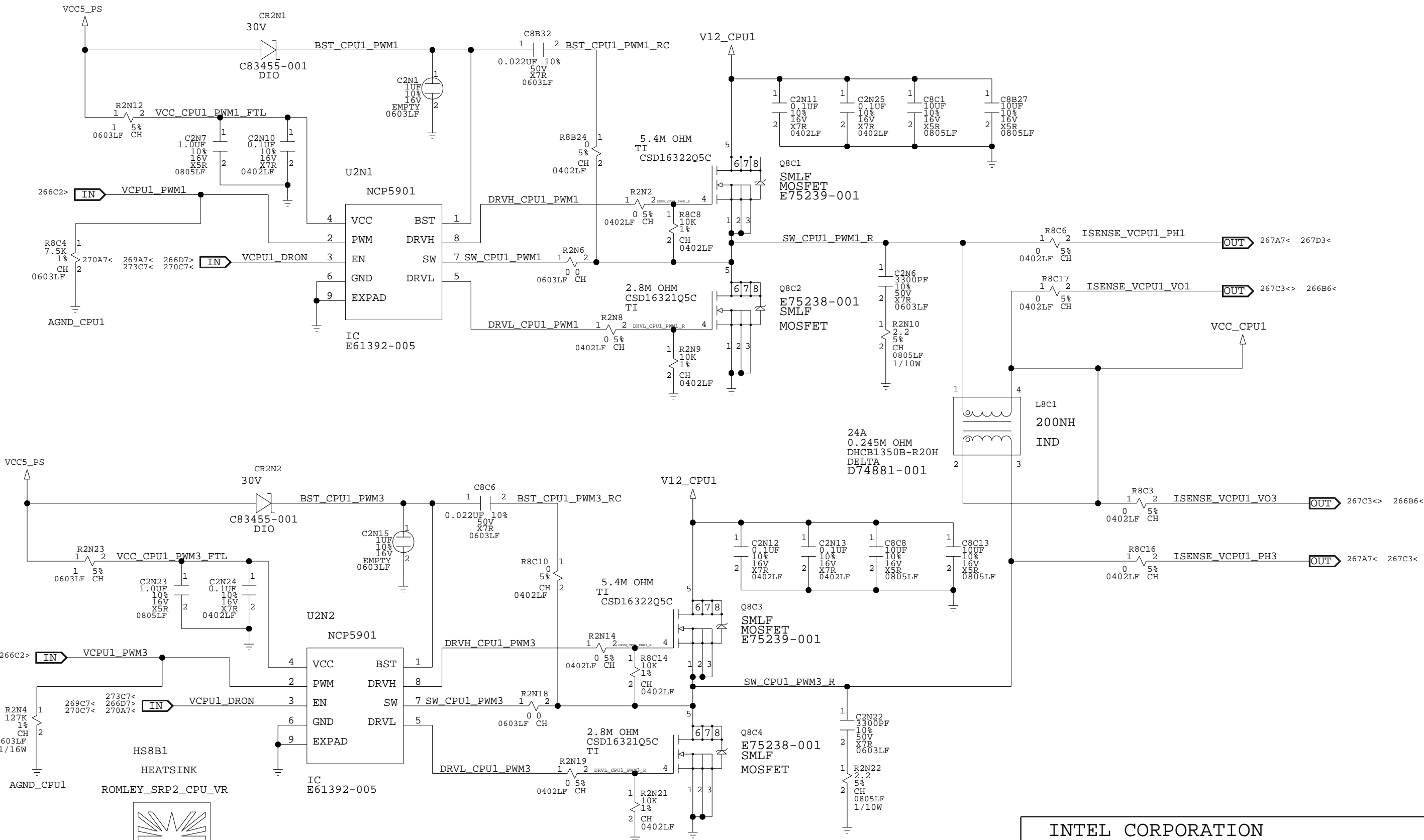
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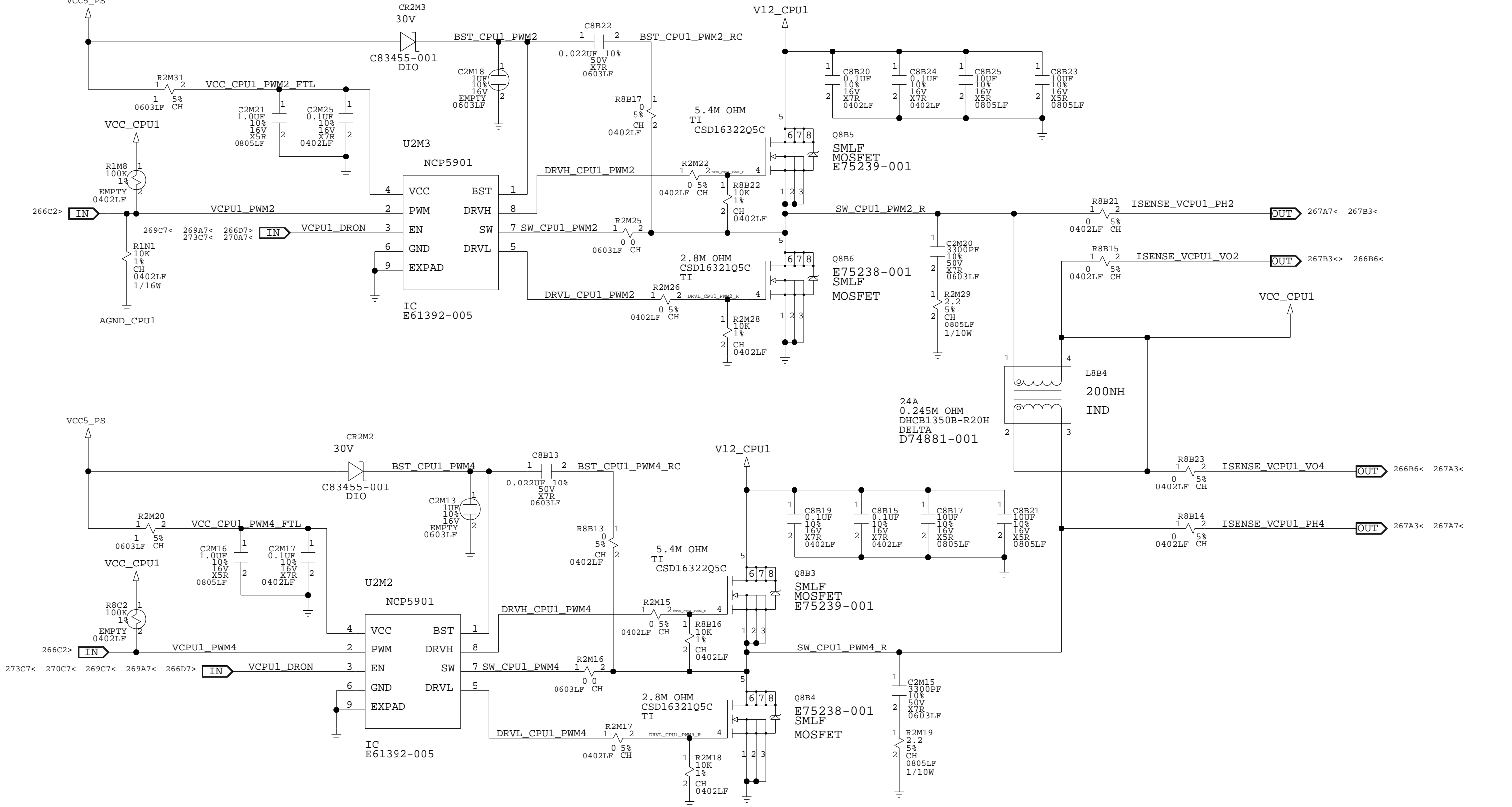


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HEAT SINK REQUIRED ON FETS

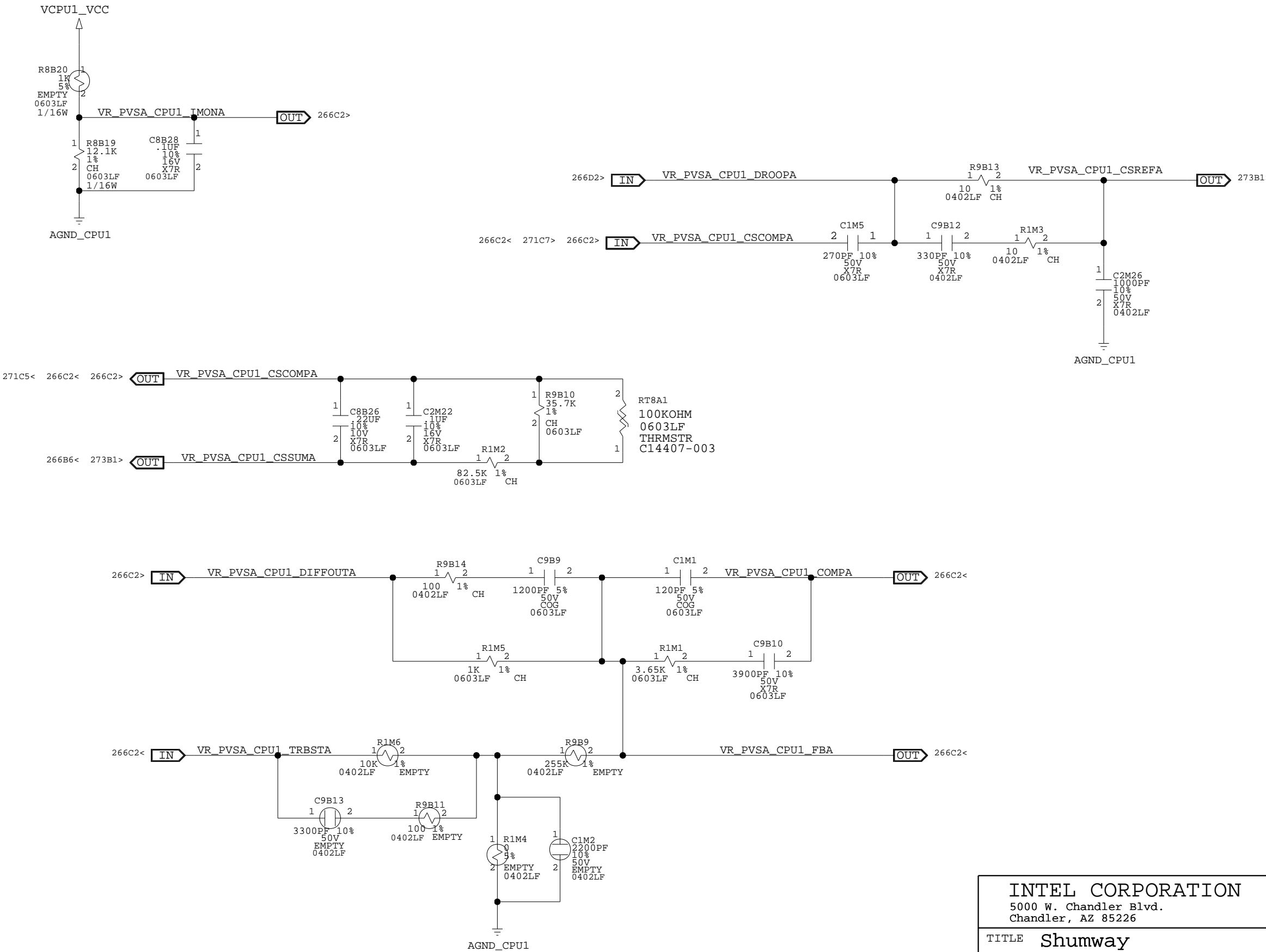
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TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VCC_CPU1/VCCSA_CPU1-4/8 Intel Confidential	SHEET 269 OF 315	

VCC\_CPU1 AND VCCSA\_CPU1 5/8

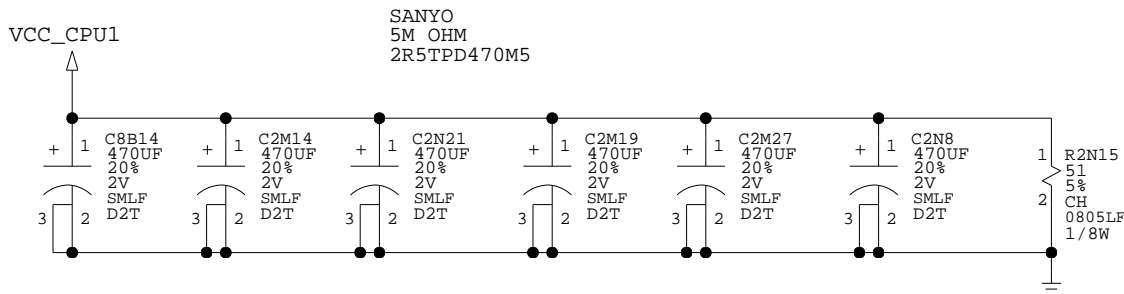
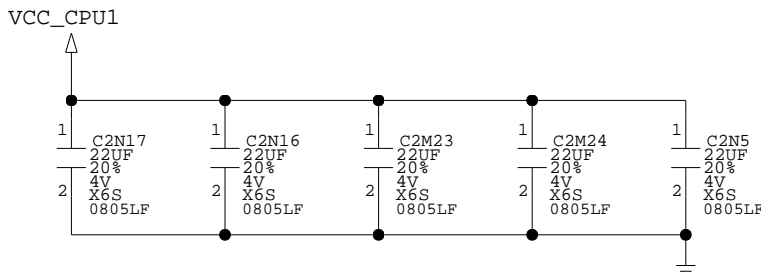
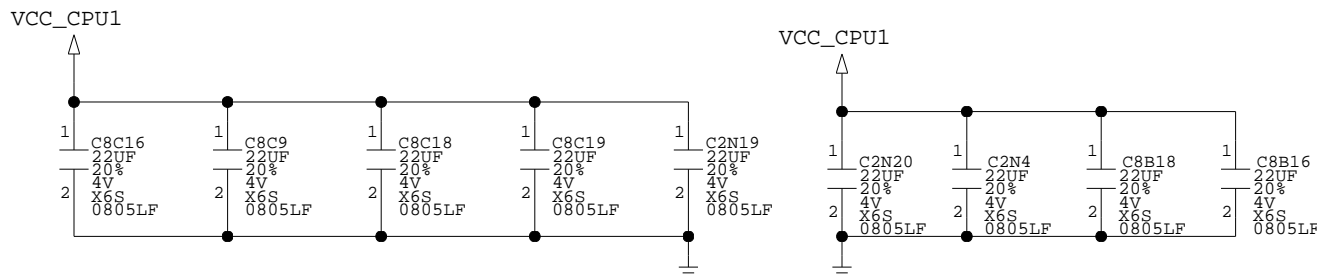
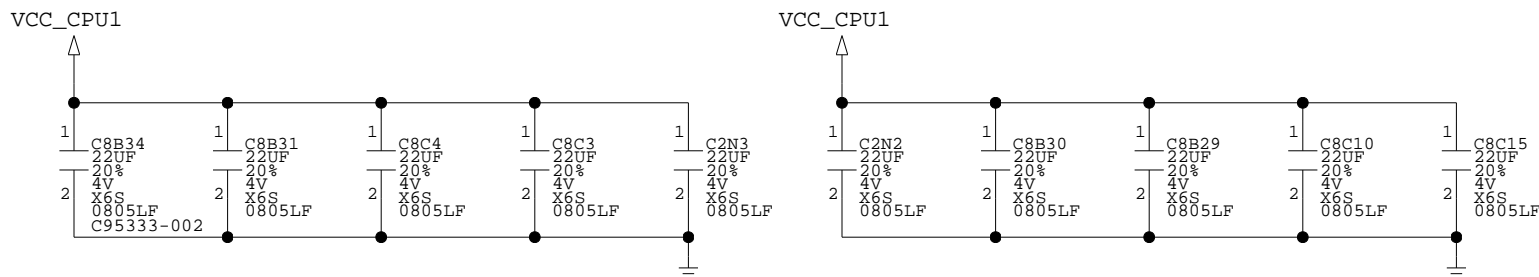
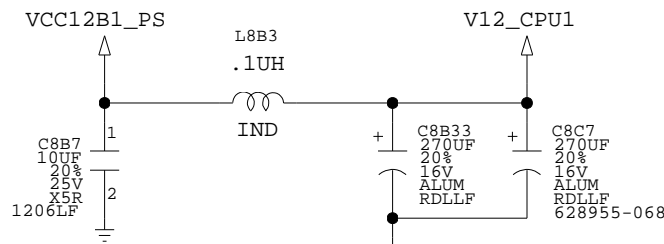


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TITLE Shumway	DOCUMENT NUMBER E97822-100	REV 1.0
VCC_CPU1/VCCSA_CPU1-5/8 Intel Confidential	SHEET 270 OF 315	

VCC\_CPU1 AND VCCSA\_CPU1 6/8



VCC\_CPU1 AND VCCSA\_CPU1 7/8



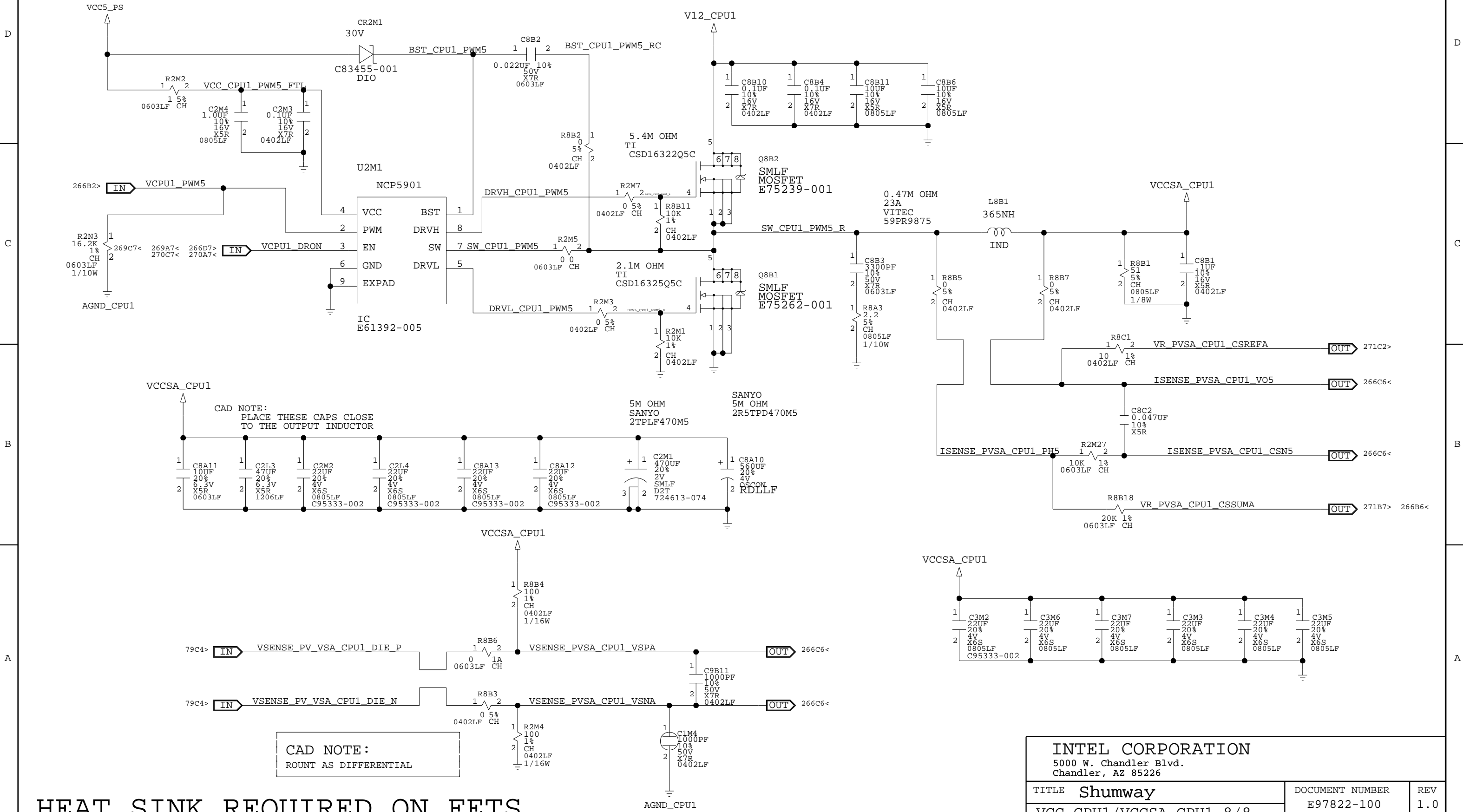
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VCC\_CPU1/VCCSA\_CPU1-7/8  
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VCC\_CPU1 AND VCCSA\_CPU1 8/8



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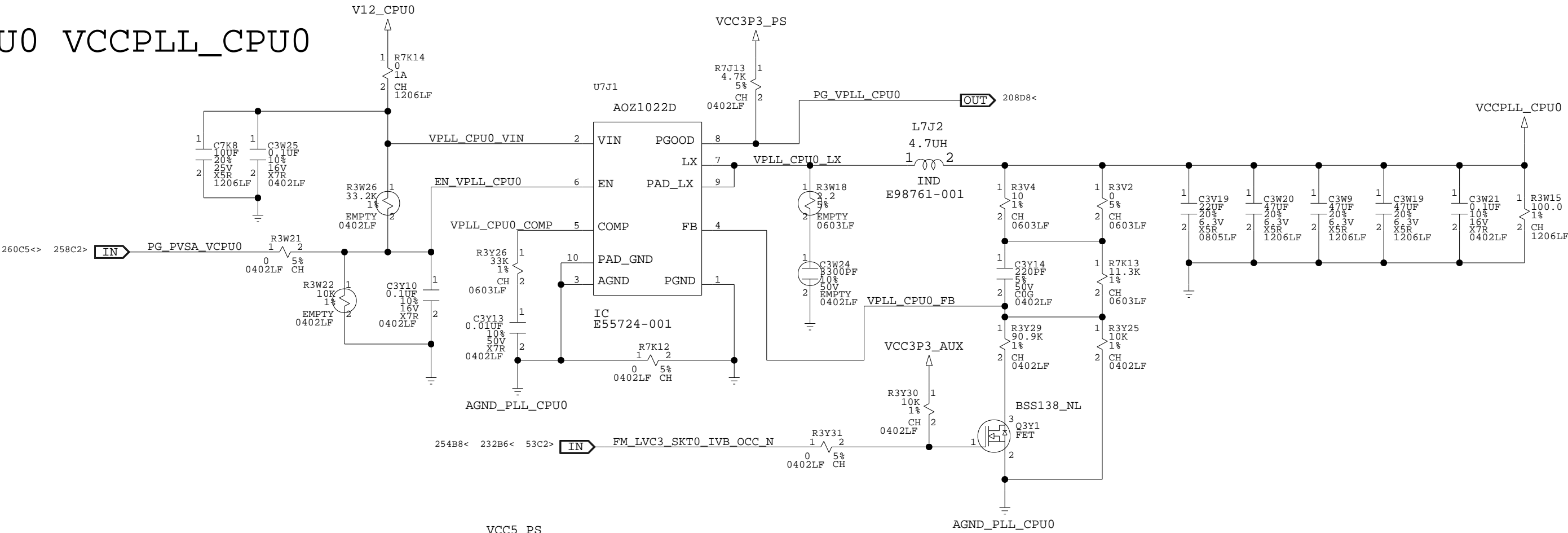
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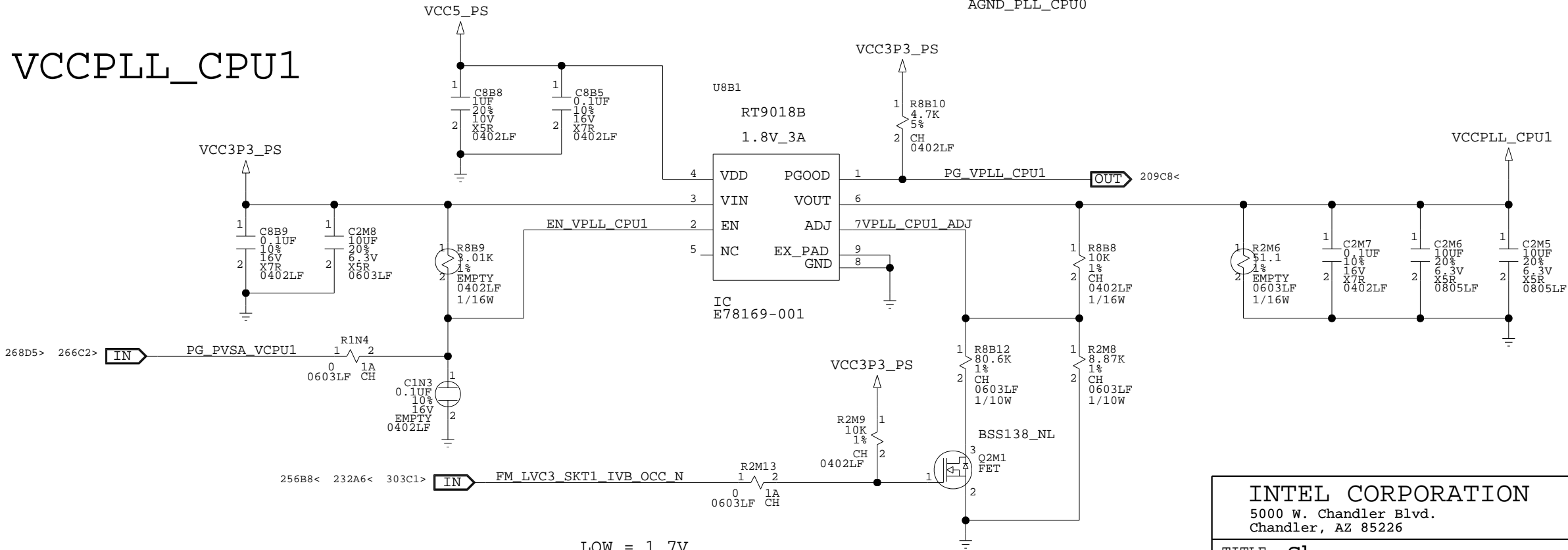
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CPU0 VCCPLL\_CPU0



CPU1 VCCPLL\_CPU1



LOW = 1.7V  
HIGH = 1.8V

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VCCPLL CPU0&1 Intel Confidential		E97822-100
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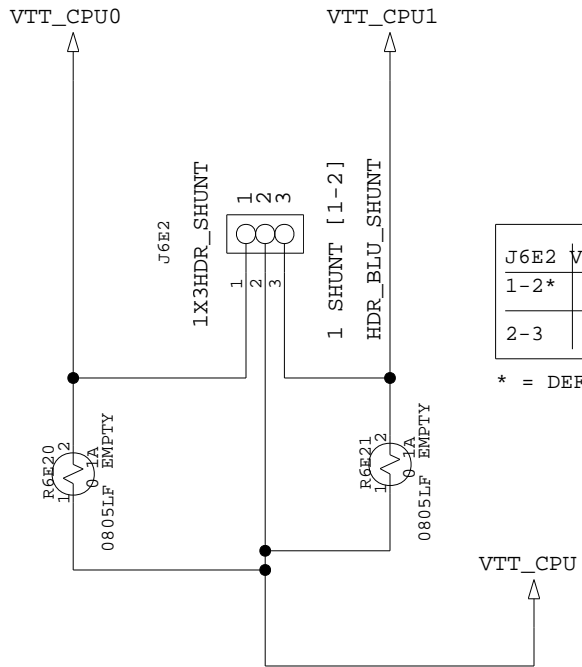
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ADR TEST LOGIC Intel Confidential		E97822-100	1.0
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D	<div>XDP0</div> <div>CPU0 (JKT EP)</div> <div>CPU1 (JKT EN)</div>								D
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A									A
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INTEL CORPORATION 5000 W. Chandler Blvd. Chandler, AZ 85226		
TITLE	Shumway	DOCUMENT NUMBER
(XDP0) XDP CPU SECTION Intel Confidential		REV
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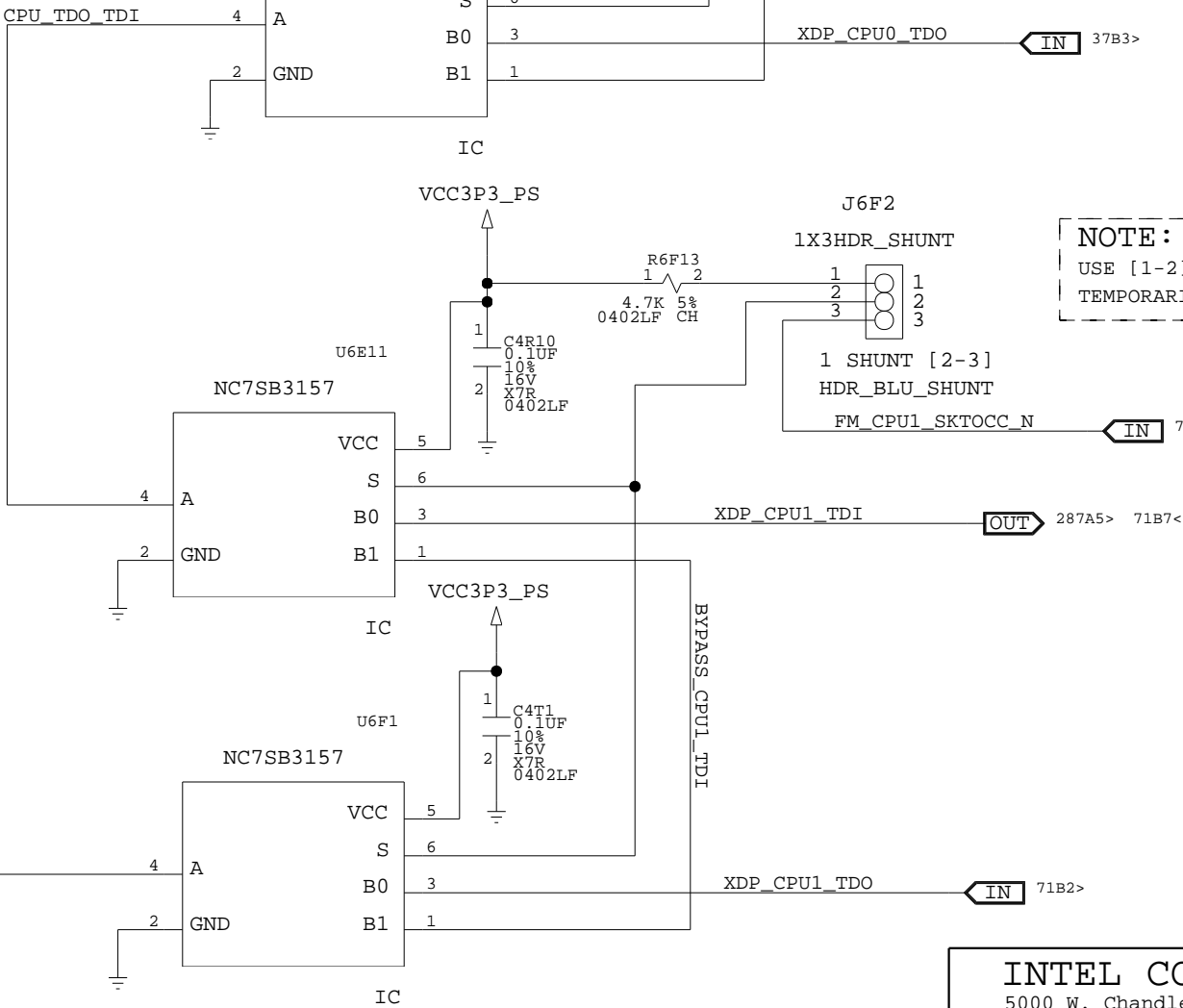
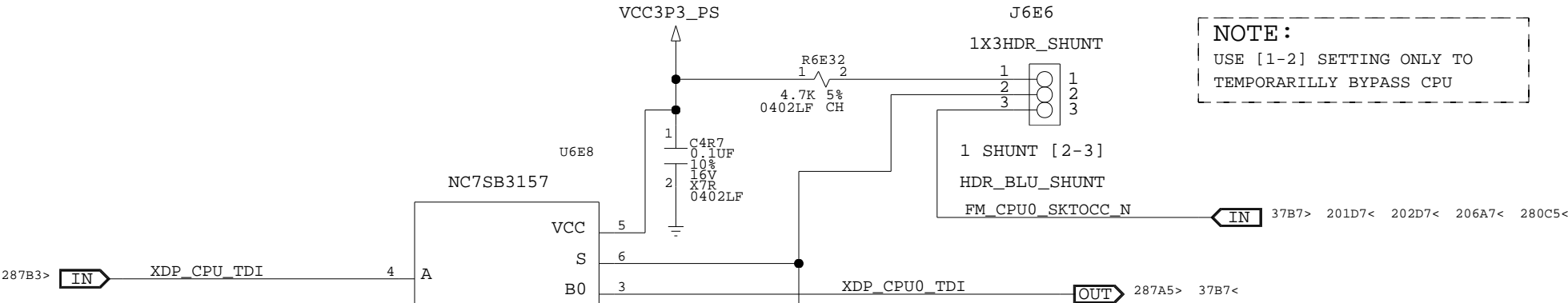
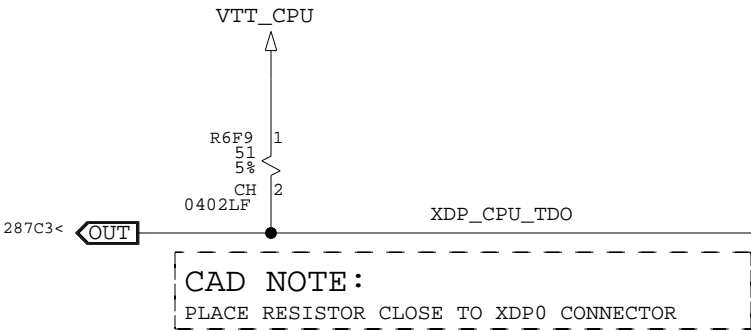
XDP0  
CPU0 AND CPU1 JTAG  
GLUE LOGIC



J6E2	VTT_CPU
1-2*	CPU0
2-3	CPU1

\* = DEFAULT

DESIGN NOTE:  
DEPOP HEADER FOR UP CONFIGS  
USE THE RESISTORS INSTEAD!



NOTE:  
USE [1-2] SETTING ONLY TO  
TEMPORARILLY BYPASS CPU

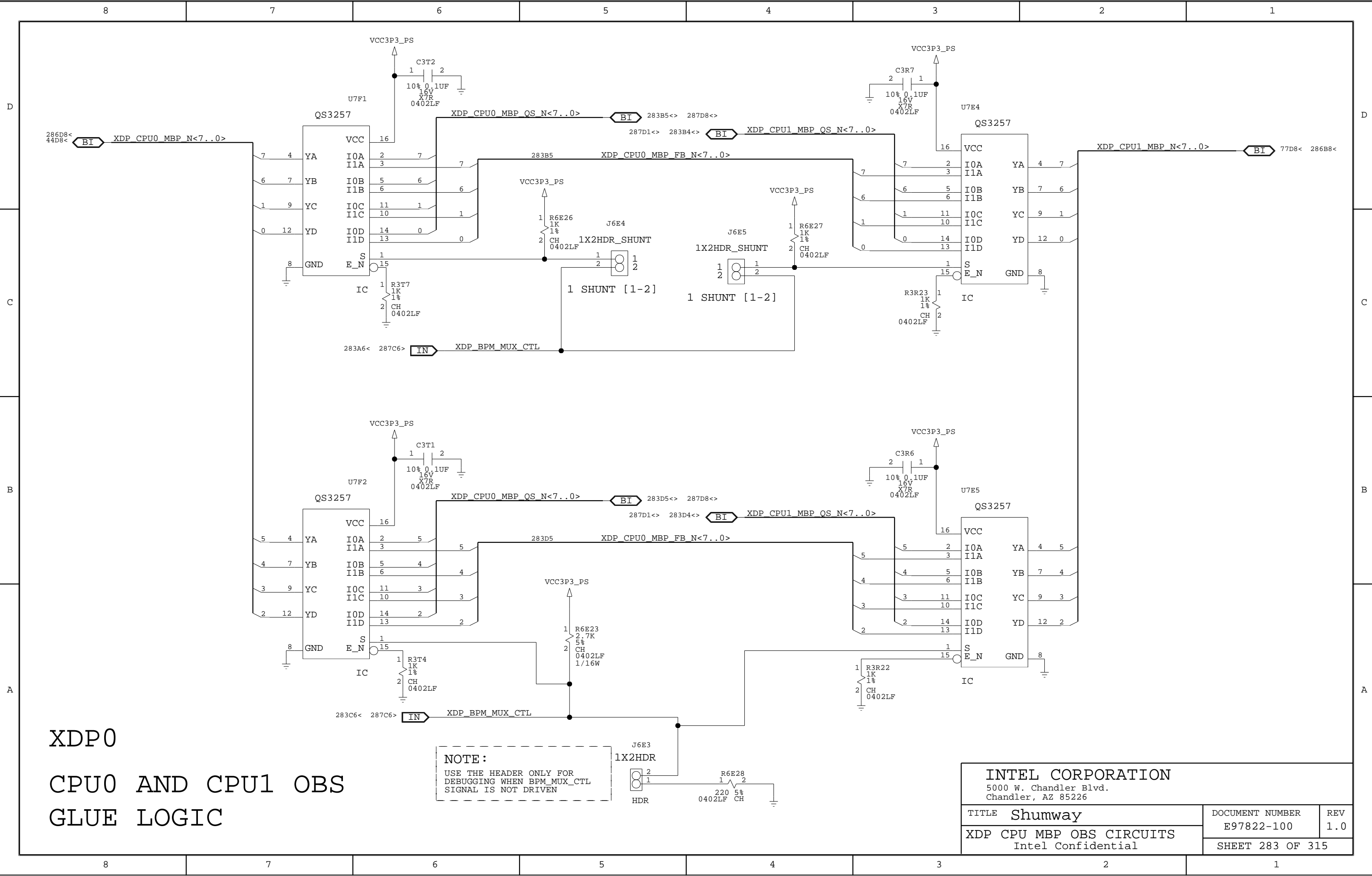
NOTE:  
USE [1-2] SETTING ONLY TO  
TEMPORARILLY BYPASS CPU

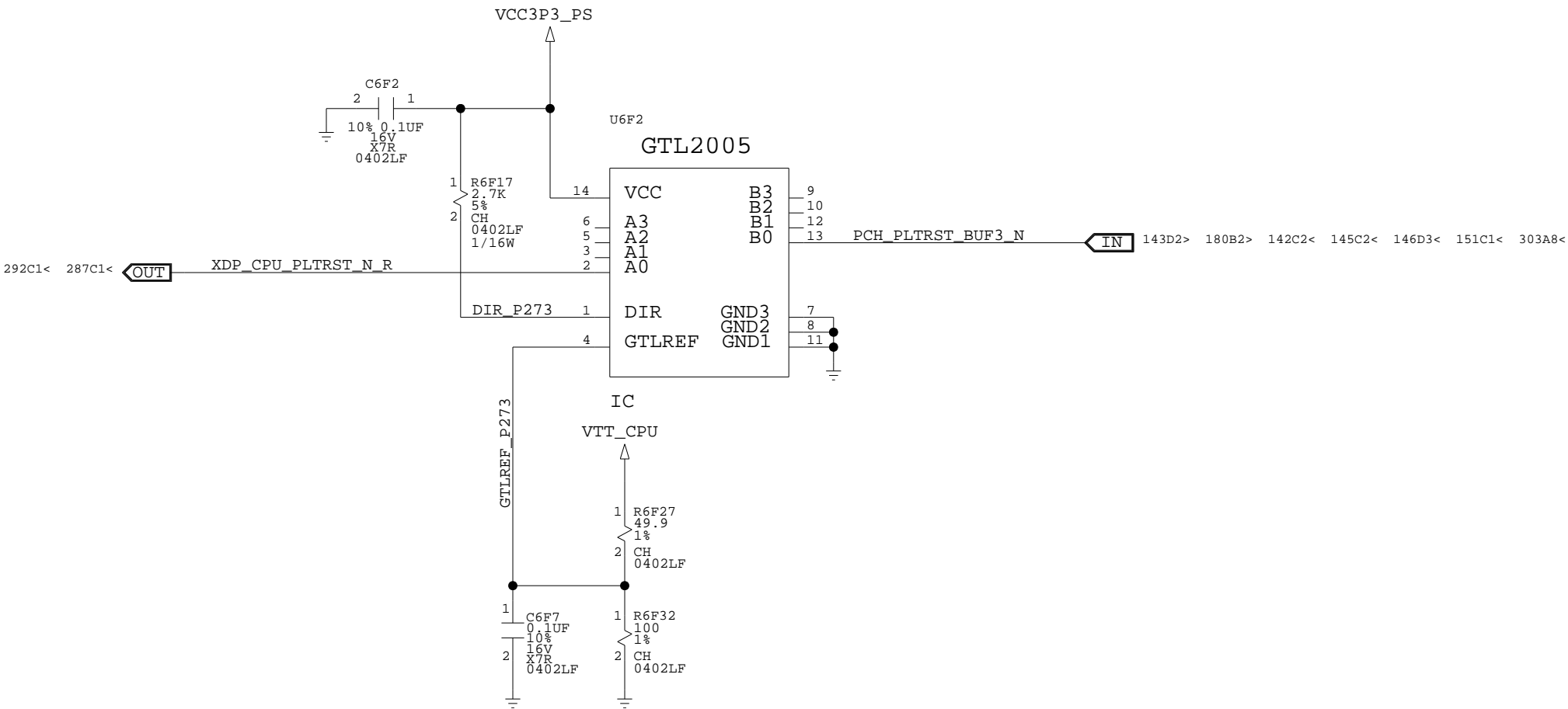
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TITLE Shumway  
XDP CPU JTAG BYPASS CKTS  
Intel Confidential

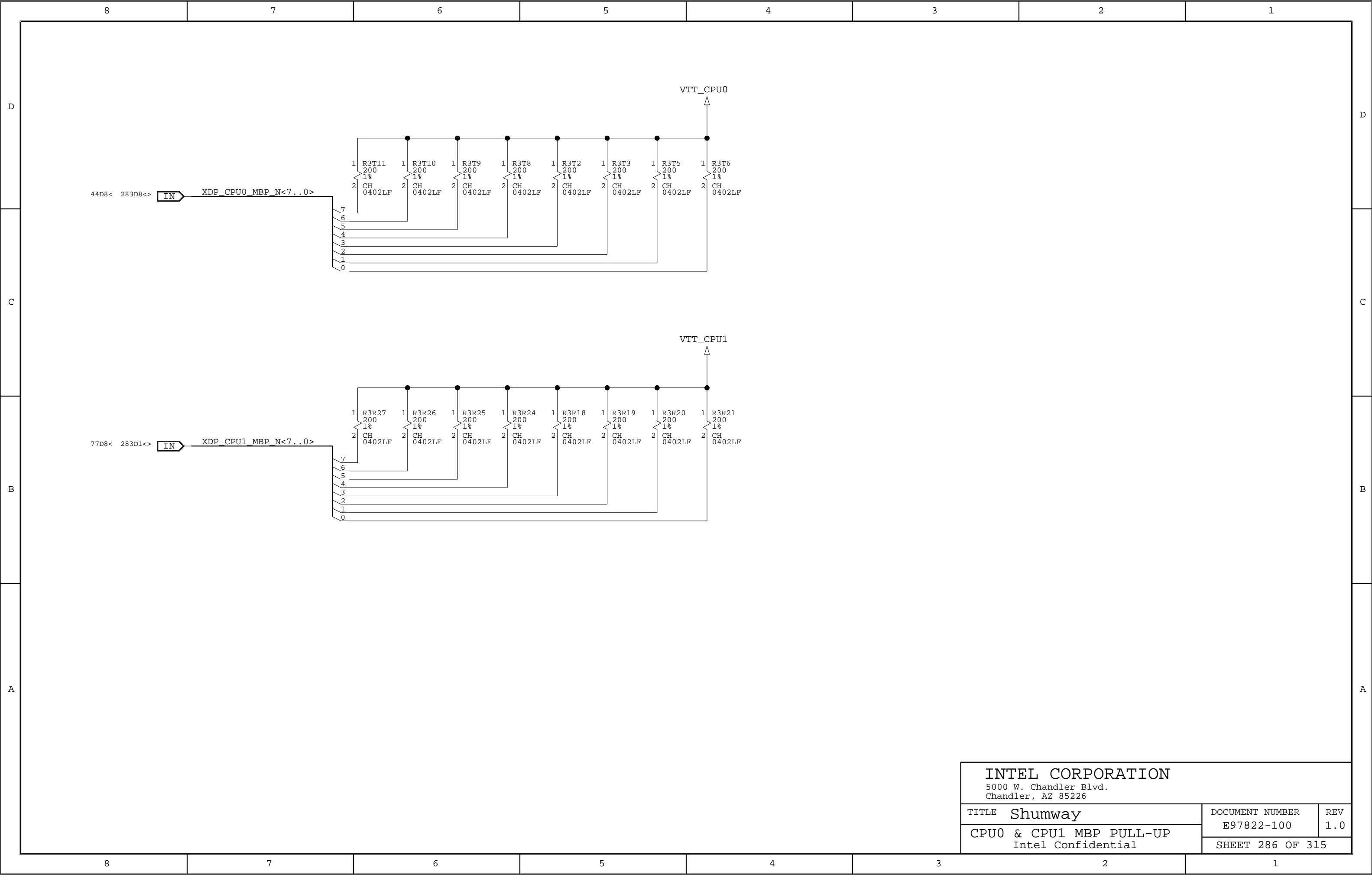
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## D



1. PLACE TDI PU TERM RESISTORS WITHIN 200 PSEC OFF THE CPUS
2. PLACE TMS PU AND TCK PD TERM RESISTORS WITHIN 200 PSEC OFF THE CPU1
3. ROUTE CPU\_TCK AND CPU\_TMS SIGNALS DAISY CHAIN WAY (XDP0 - CPU0 - CPU1 - TERM)

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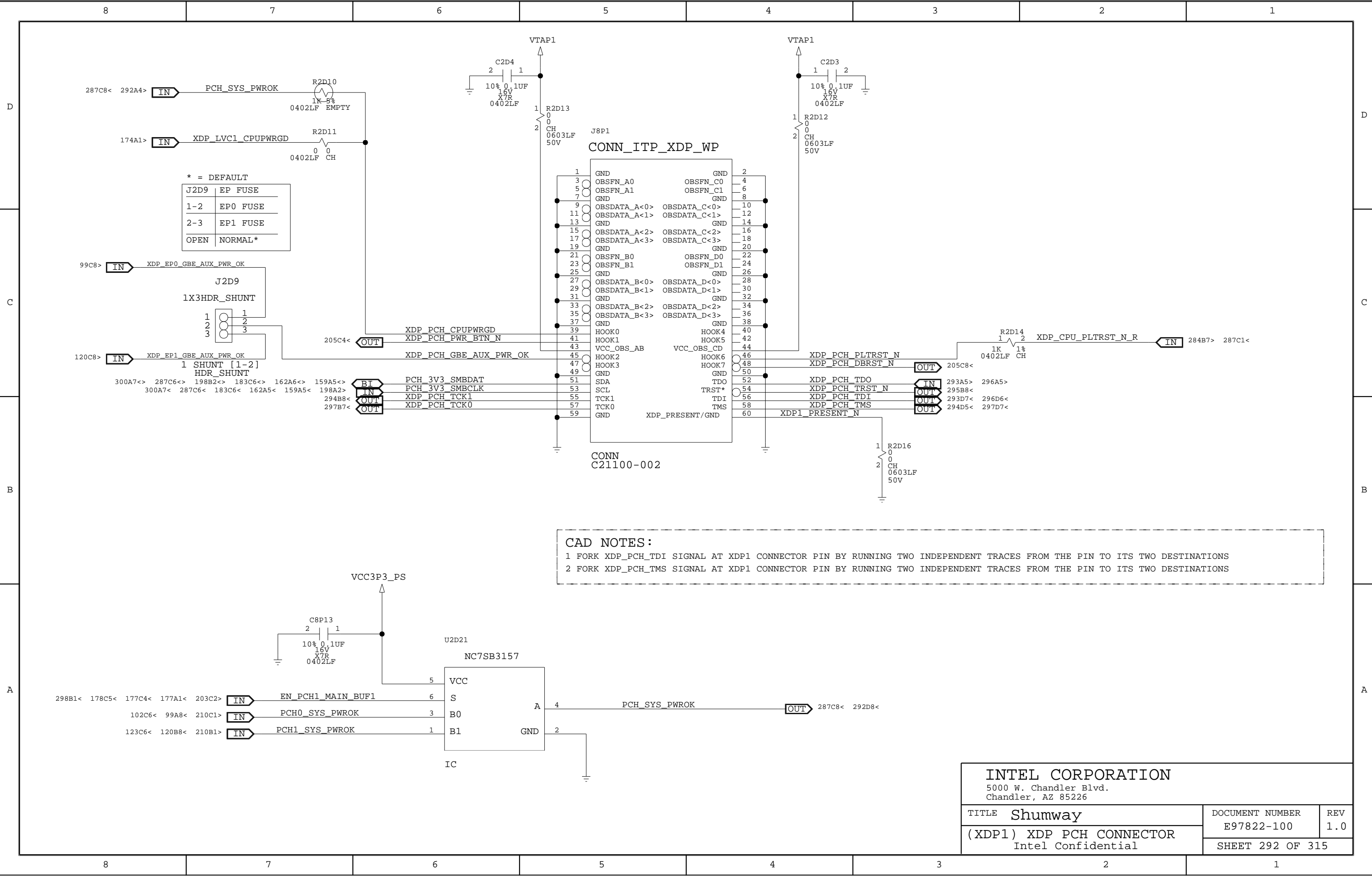
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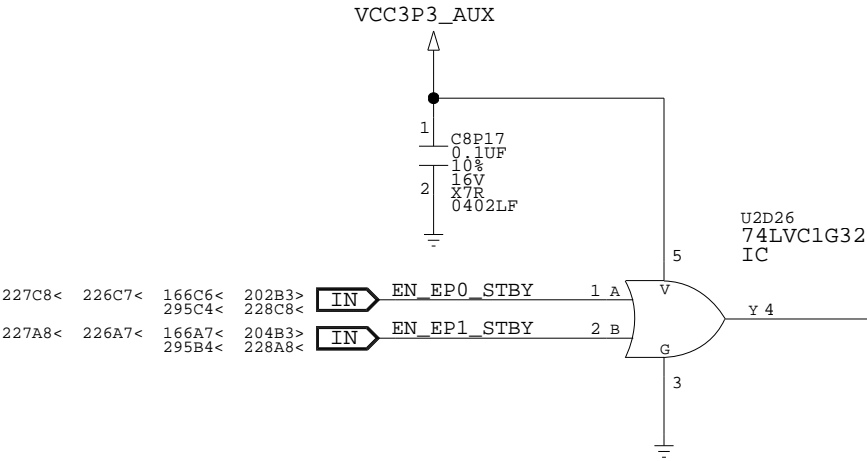
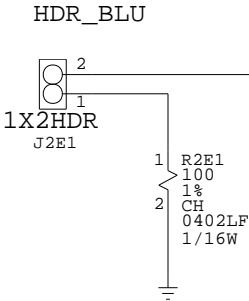
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(XDP1) XDP PCH SECTION Intel Confidential						SHEET 291 OF 315	
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CAD NOTE:  
PLACE IC CLOSE TO XDP1 CONN TO ASSURE  
XDP\_PCH\_TDI IS SHORTER THAN 200 PSEC

J46	EP1 JTAG
1-2	DISABLE (DEBUG ONLY)
OPEN*	ENABLE

\* DEFAULT



XDP1 (XDP\_PCH)

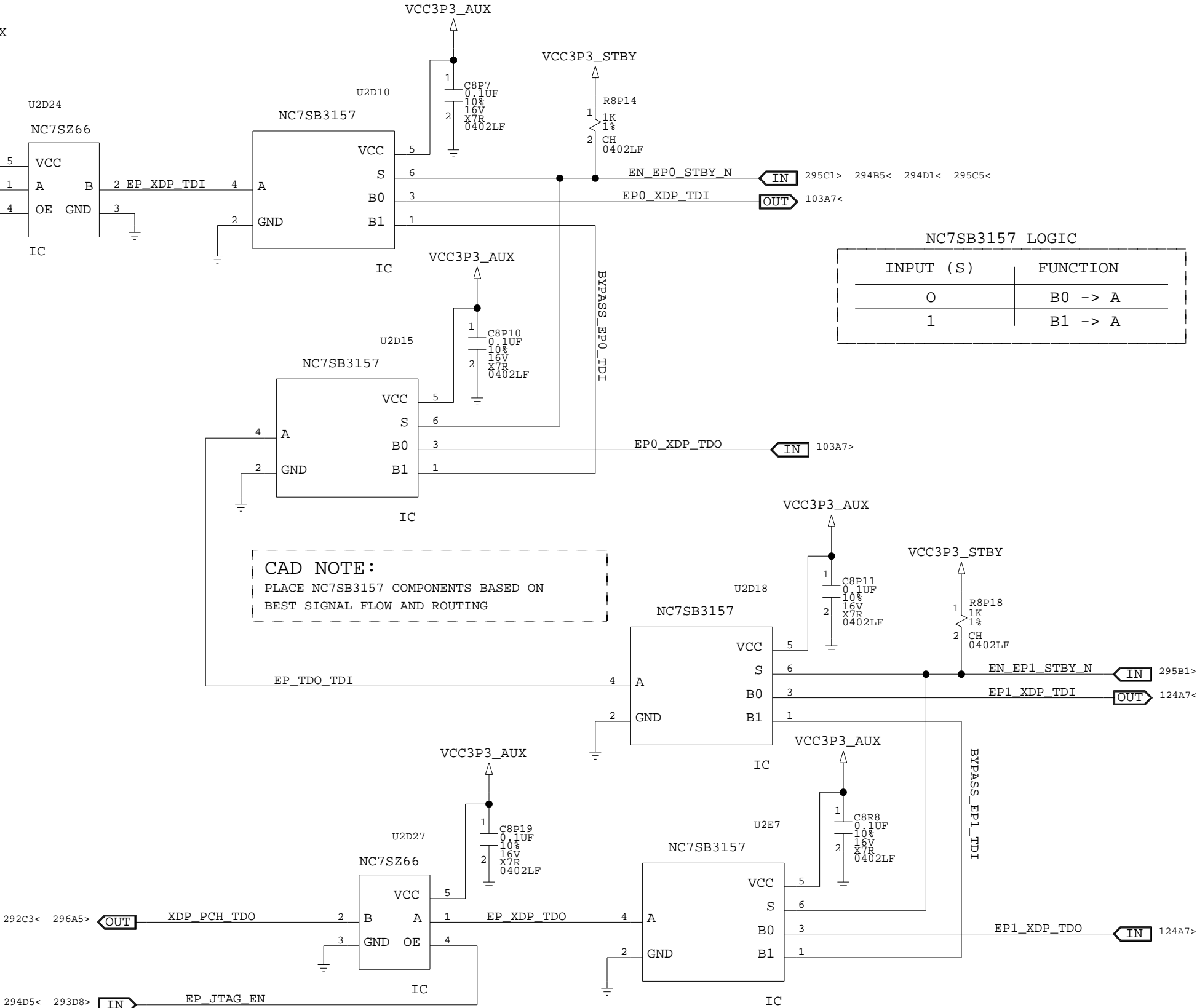
EP0 AND EP1 JTAG

BYPASS LOGIC (1)

CAD NOTE:  
PLACE IC CLOSE TO XDP1 CONN TO ASSURE  
XDP\_PCH\_TDI IS SHORTER THAN 200 PSEC

NC7SB3157 LOGIC

INPUT (S)	FUNCTION
0	B0 -> A
1	B1 -> A



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XDP PCH - EP BYPASS (1) Intel Confidential	SHEET 293 OF 315	

XDP1 (XDP\_PCH)  
EP0 AND EP1 JTAG  
BYPASS LOGIC (2)

NC7SB3157 LOGIC

INPUT (S)	FUNCTION
O	B0 -> A
1	B1 -> A

CAD NOTE:

PLACE IC CLOSE TO XDP1 CONN TO ASSURE  
XDP\_PCH\_TMS IS SHORTER THAN 200 PSEC

CAD NOTE:

PLACE CLOSE TO PCH0

CAD NOTES:

- 1 ROUTE EP0\_XDP\_TMS DAISY CHAIN WAY (U203 - EP0 - U204 - EP1)  
2 ROUTE EP0\_XDP\_TCK1 DAISY CHAIN WAY (U200 - EP0 - U201 - EP1)

CAD NOTE:

PLACE CLOSE TO PCH0

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XDP PCH - EP BYPASS (2)  
Intel Confidential

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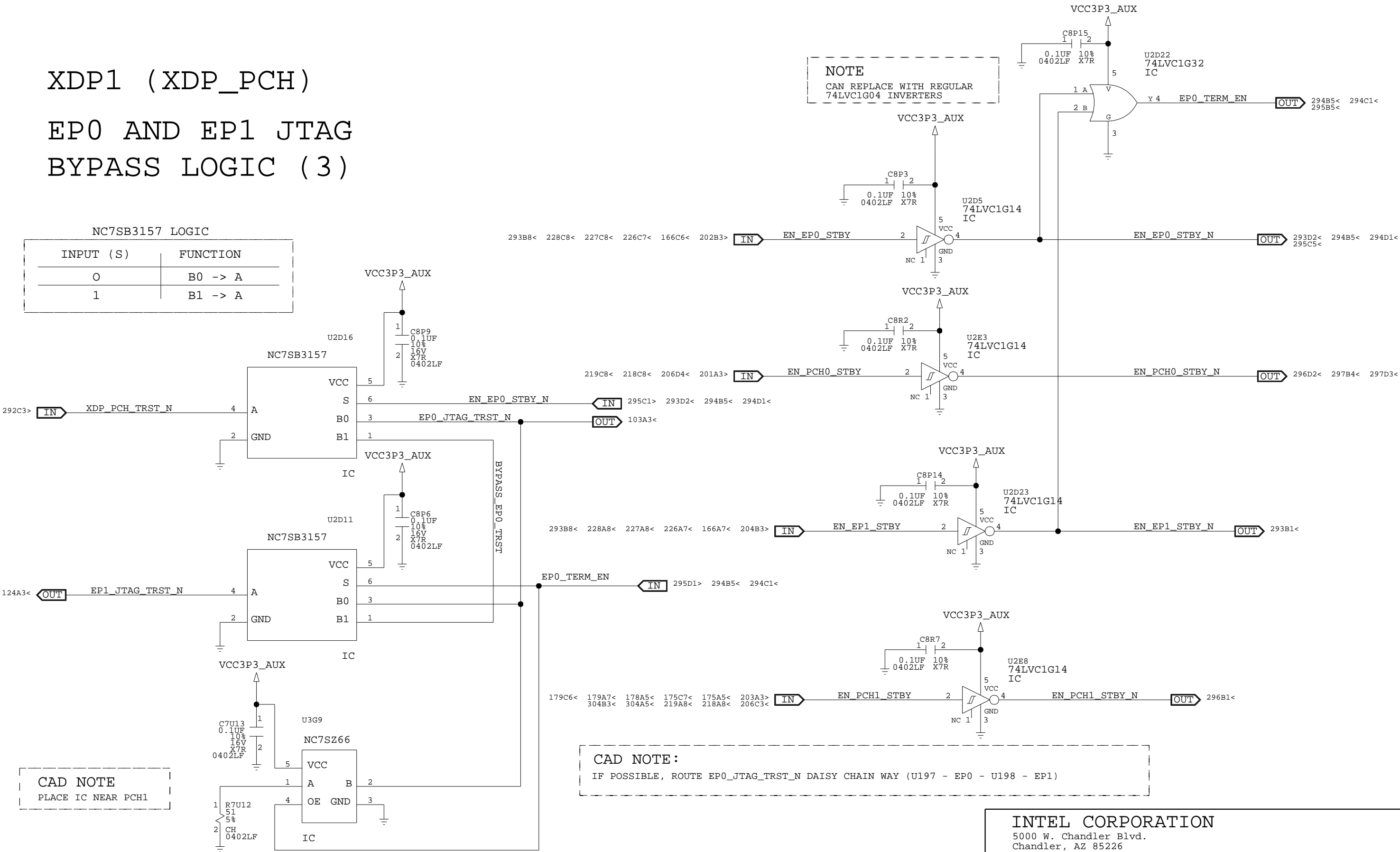
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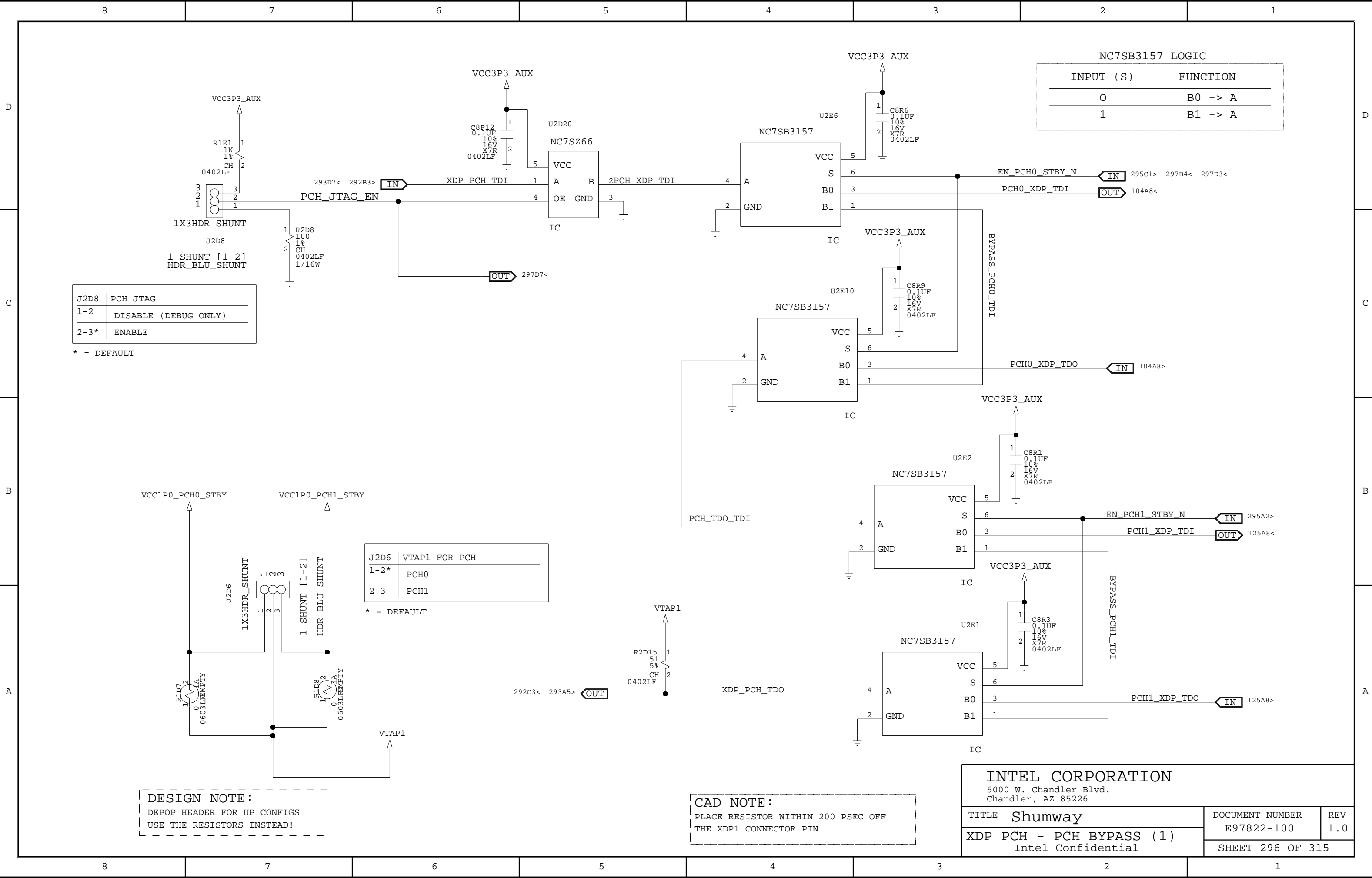
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XDP1 (XDP\_PCH)  
EP0 AND EP1 JTAG  
BYPASS LOGIC (3)

NC7SB3157 LOGIC

INPUT (S)	FUNCTION
0	B0 -> A
1	B1 -> A



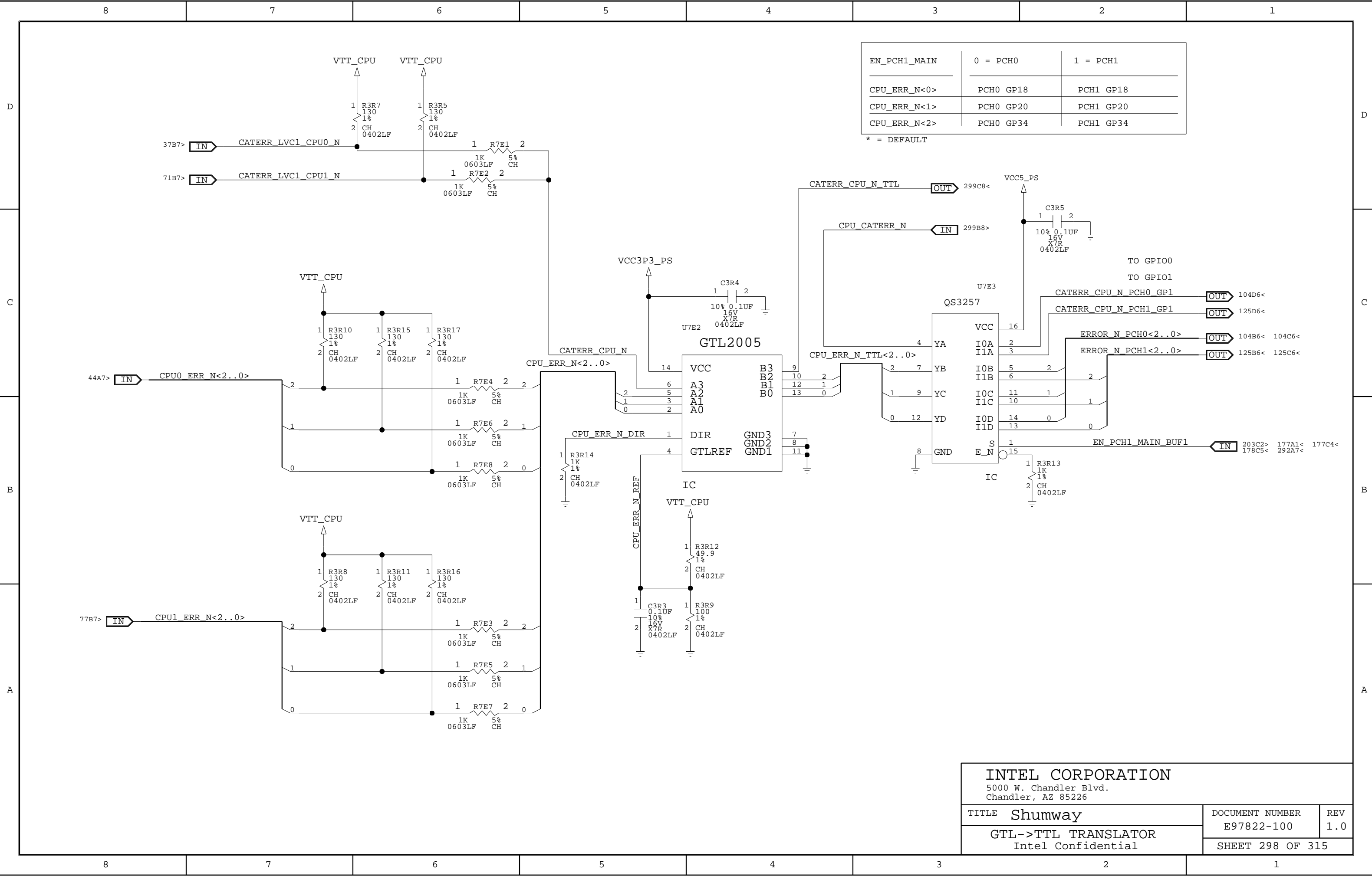




PLACE CLOSE TO ITP CONN

PLACE CLOSE TO ITP CONN

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GTL->TTL TRANSLATOR  
Intel Confidential

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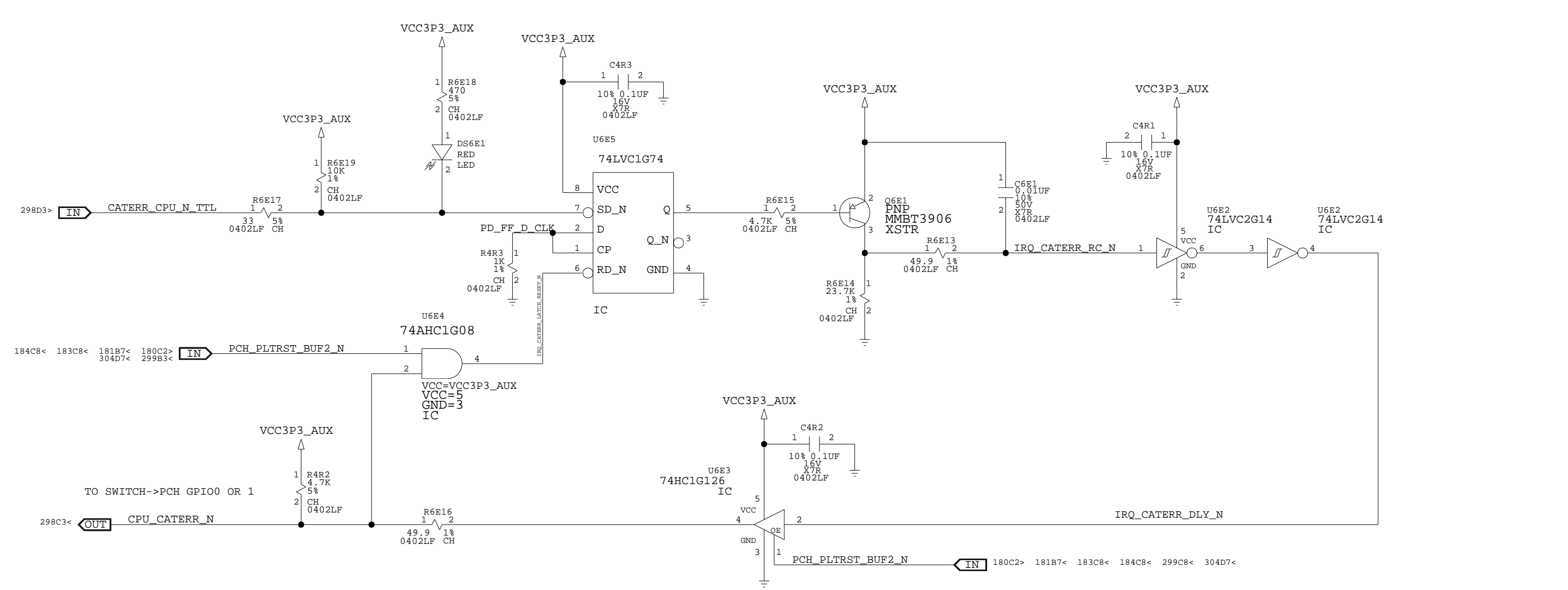
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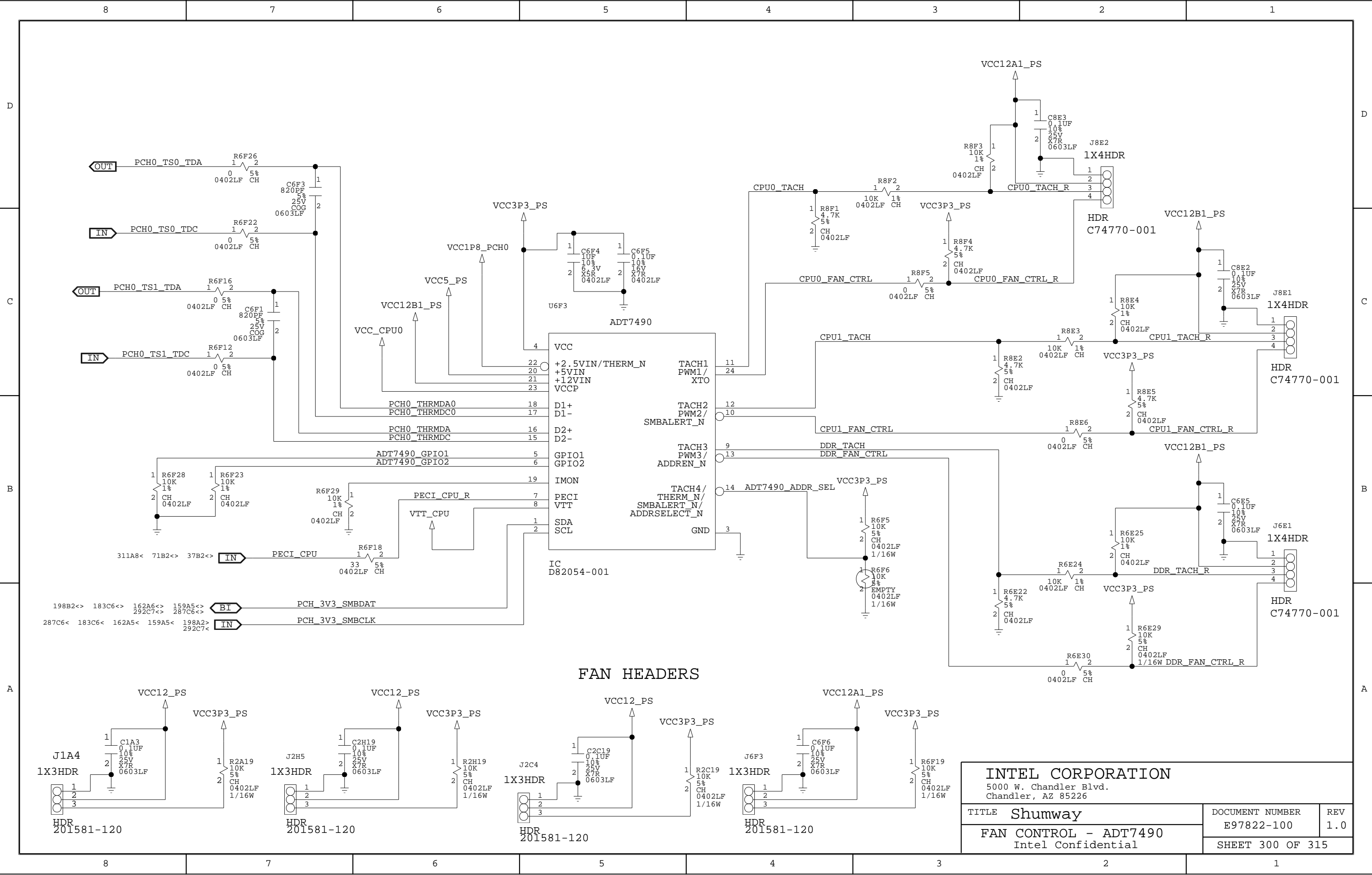
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FAN HEADERS

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FAN CONTROL - ADT7490  
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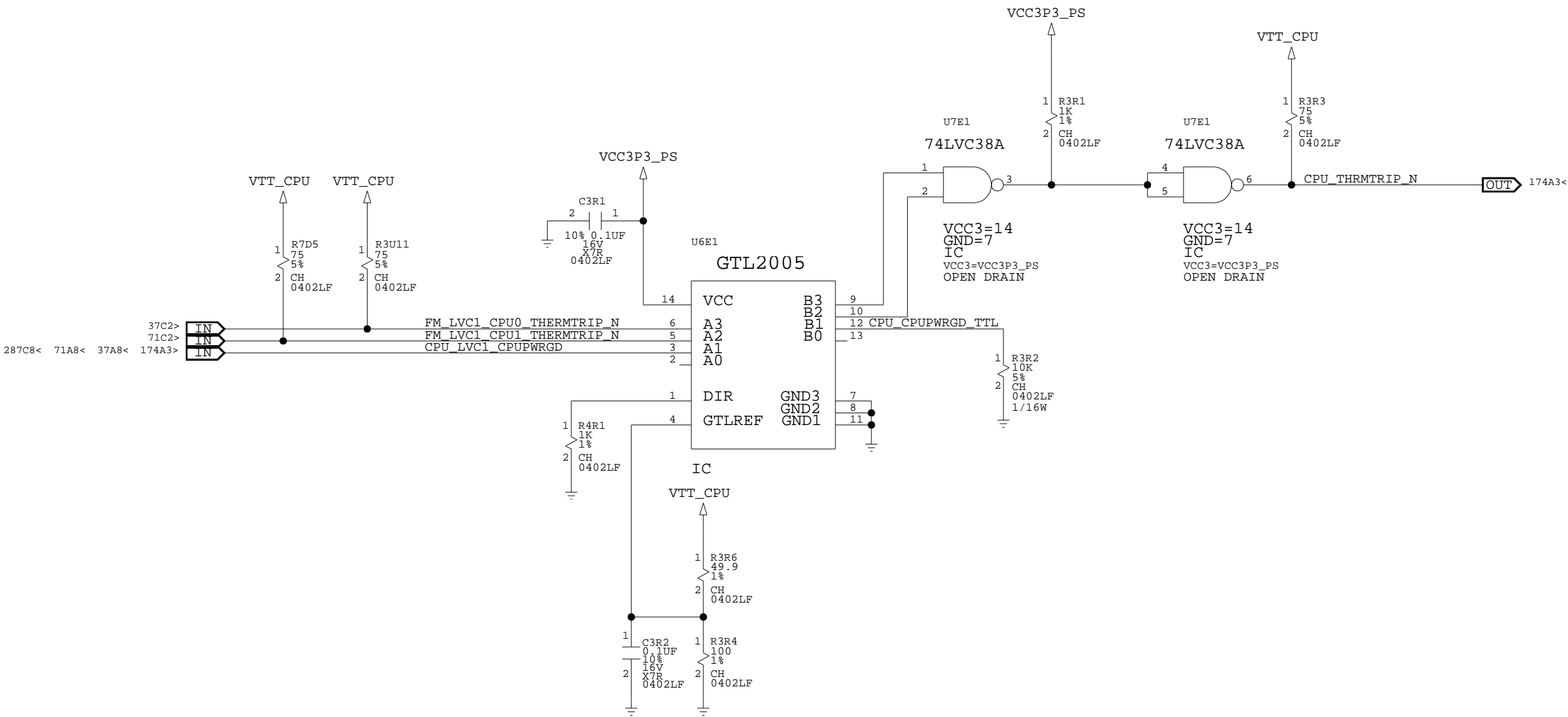
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THERMTRIP LOGIC  
Intel Confidential

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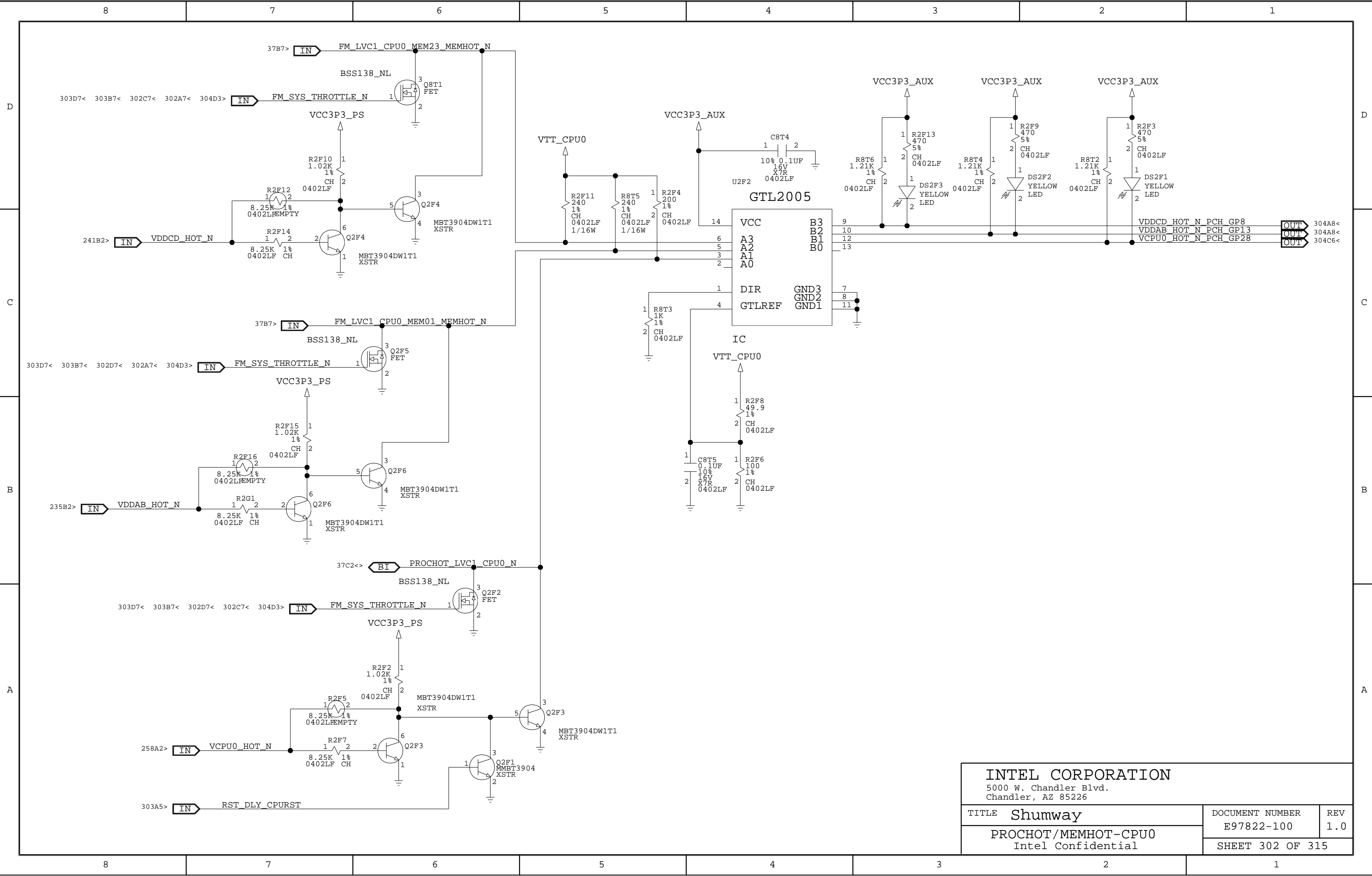
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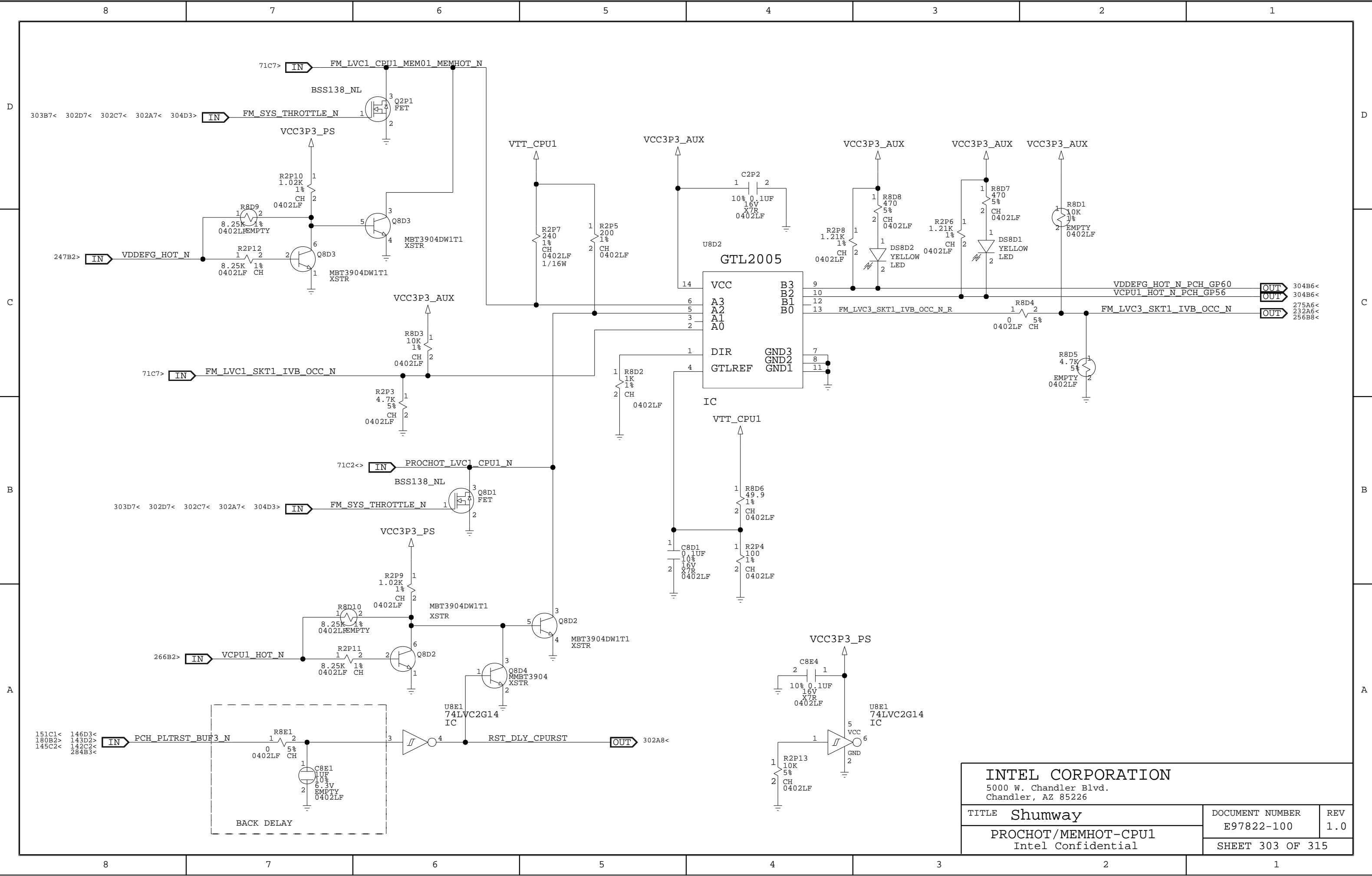
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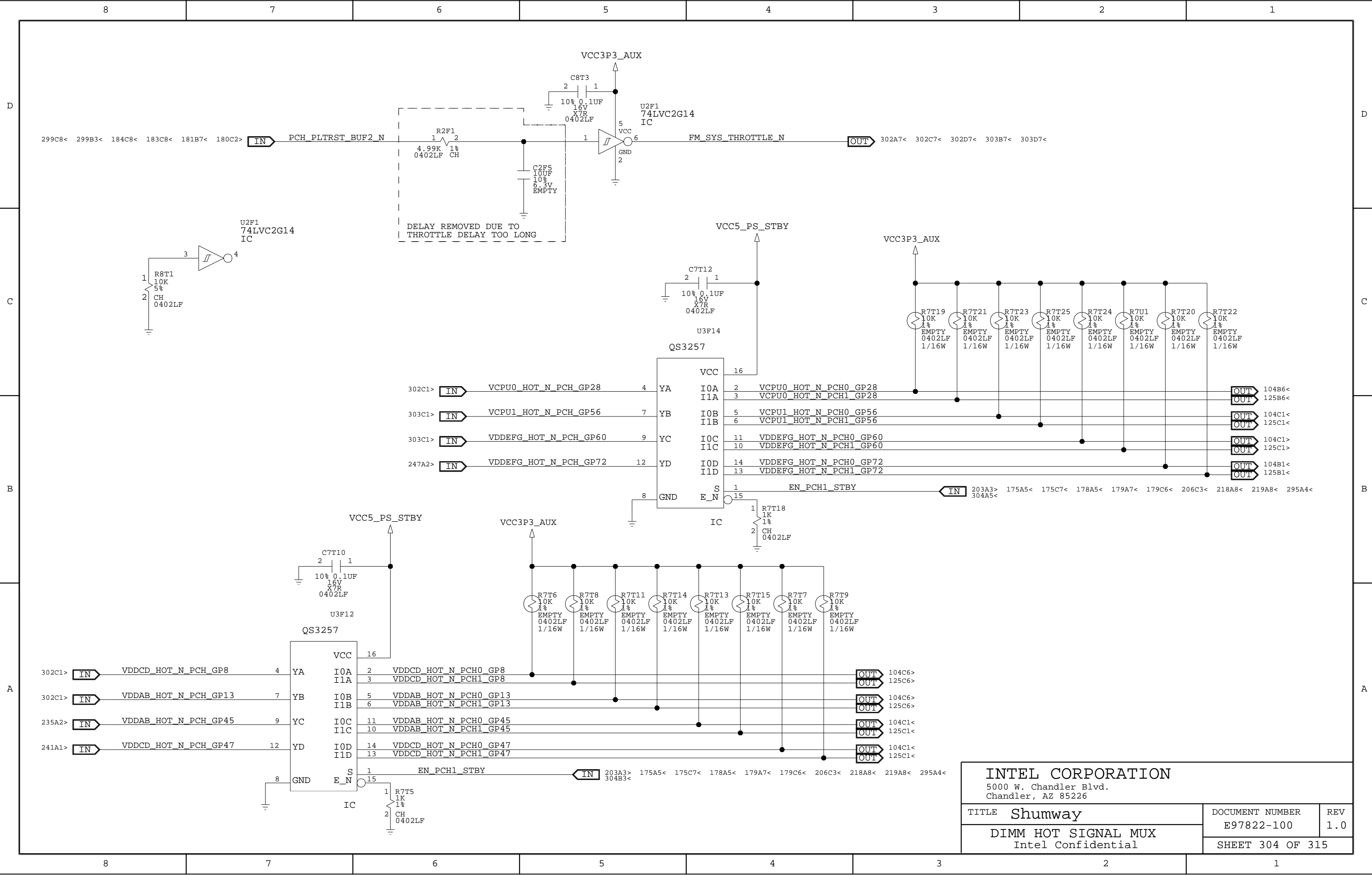
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## STATUS LEDs FOR POWER RAILS AND SIGNALS

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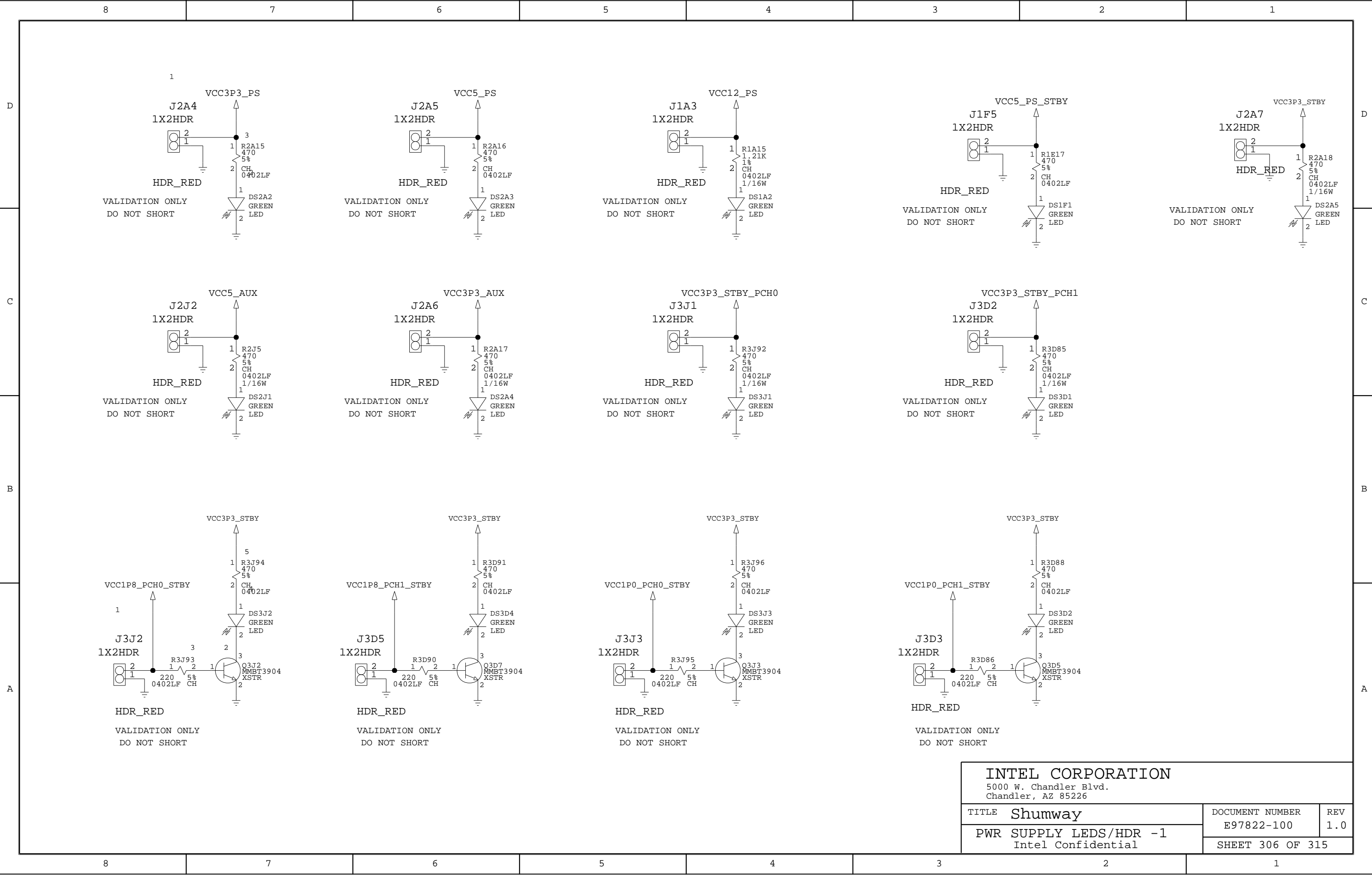
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DOCUMENT NUMBER

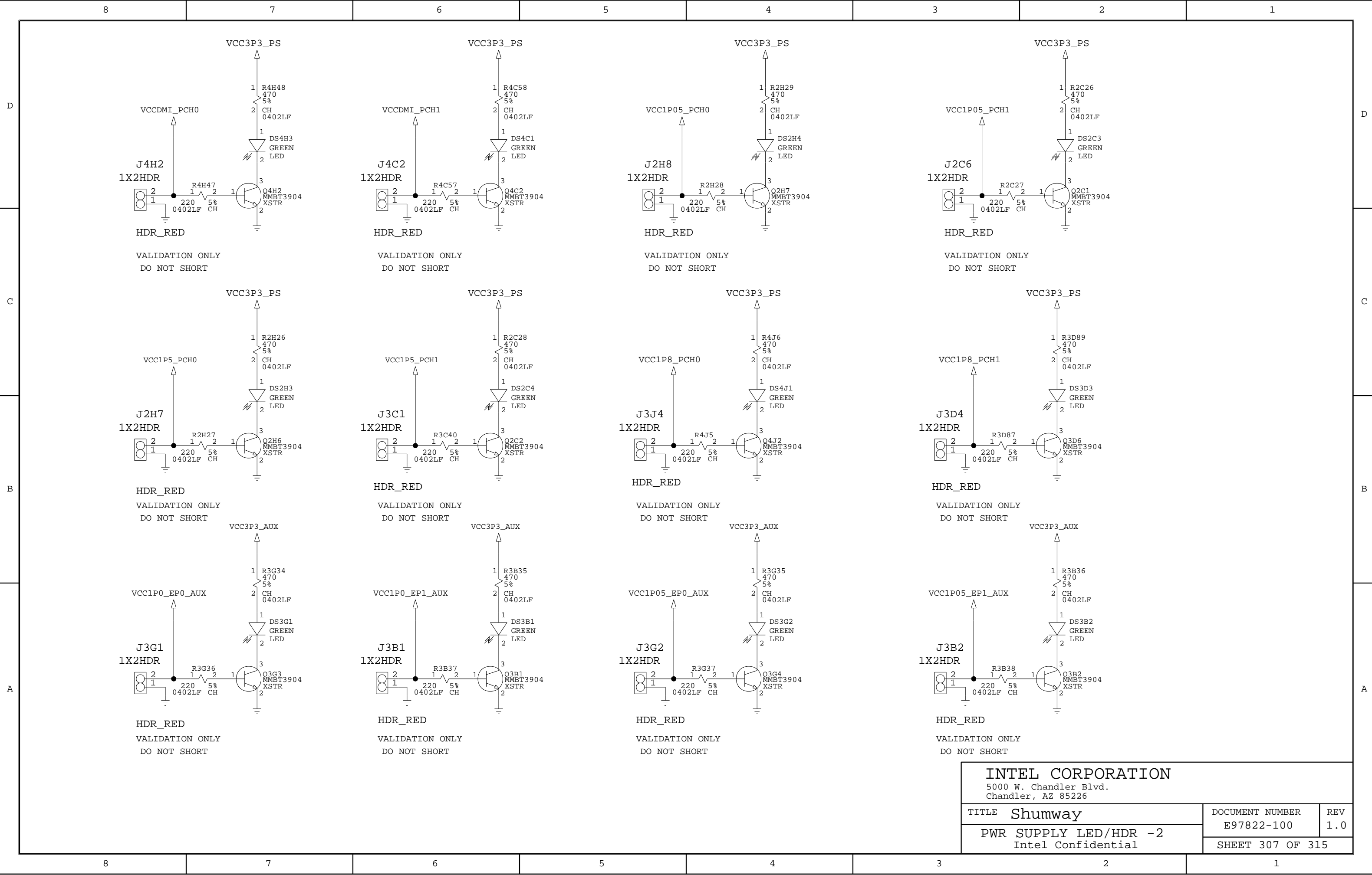
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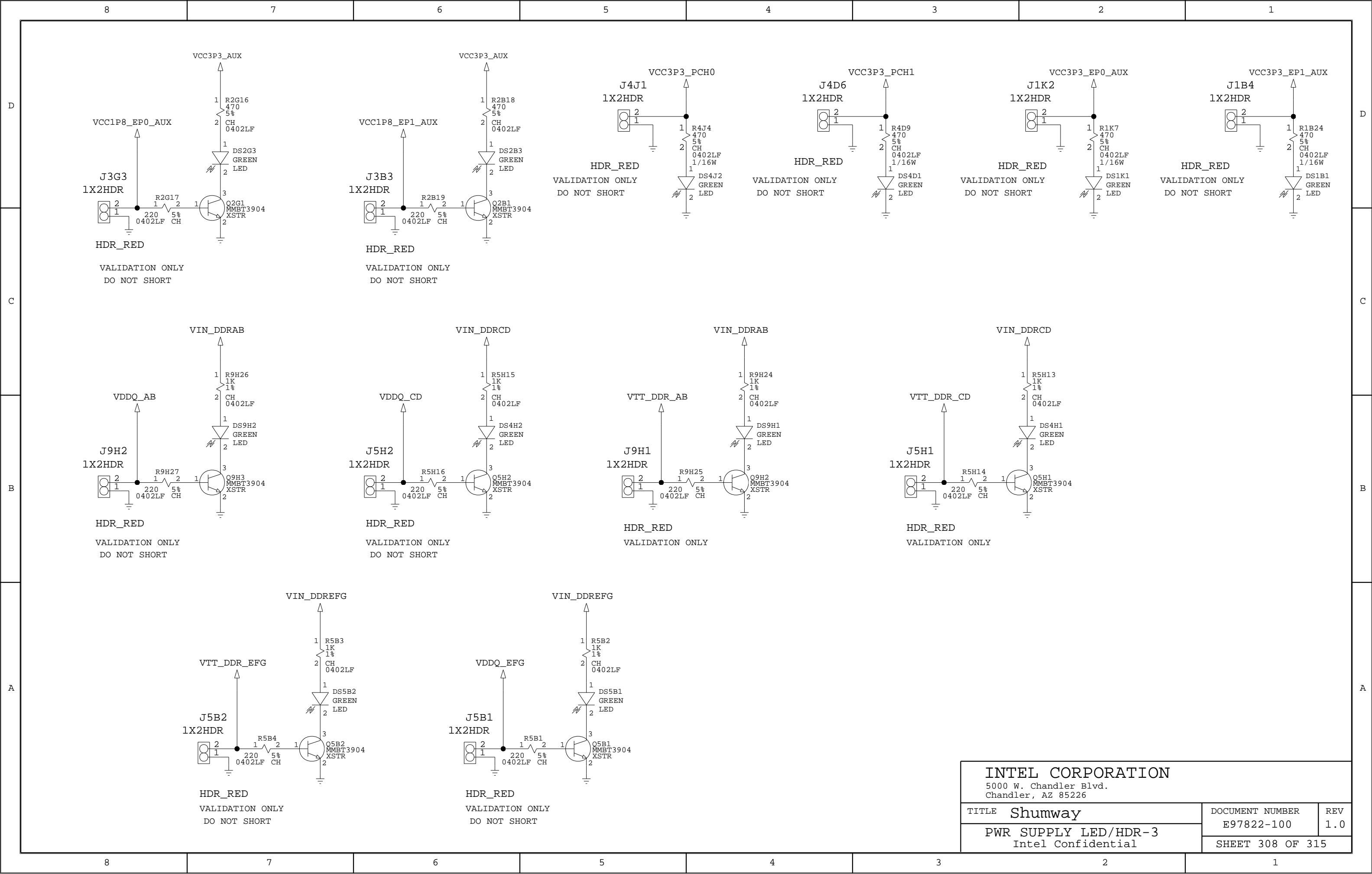
REV

1.0

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PWR SUPPLY LED/HDR-3 Intel Confidential		E97822-100
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C

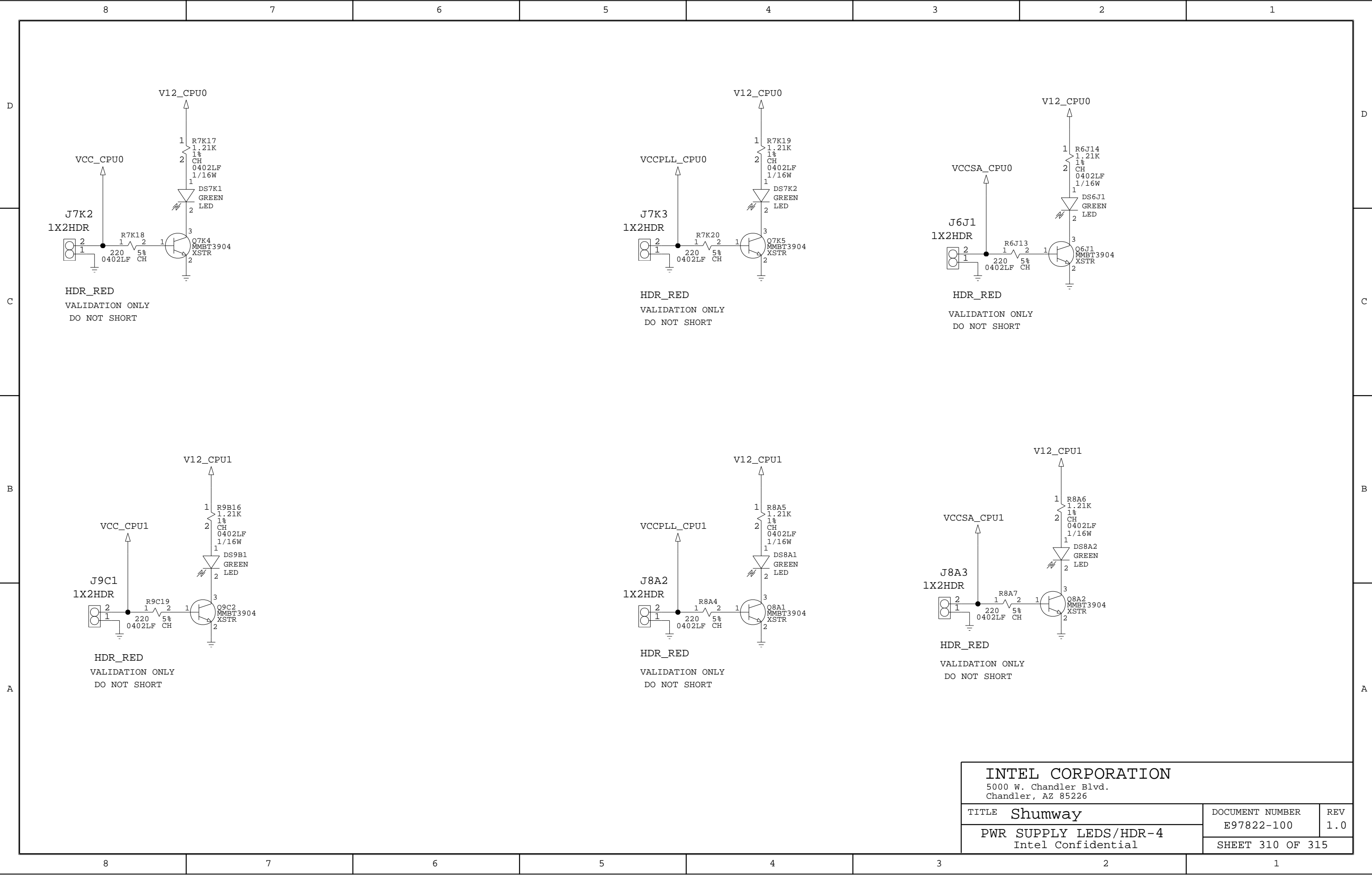


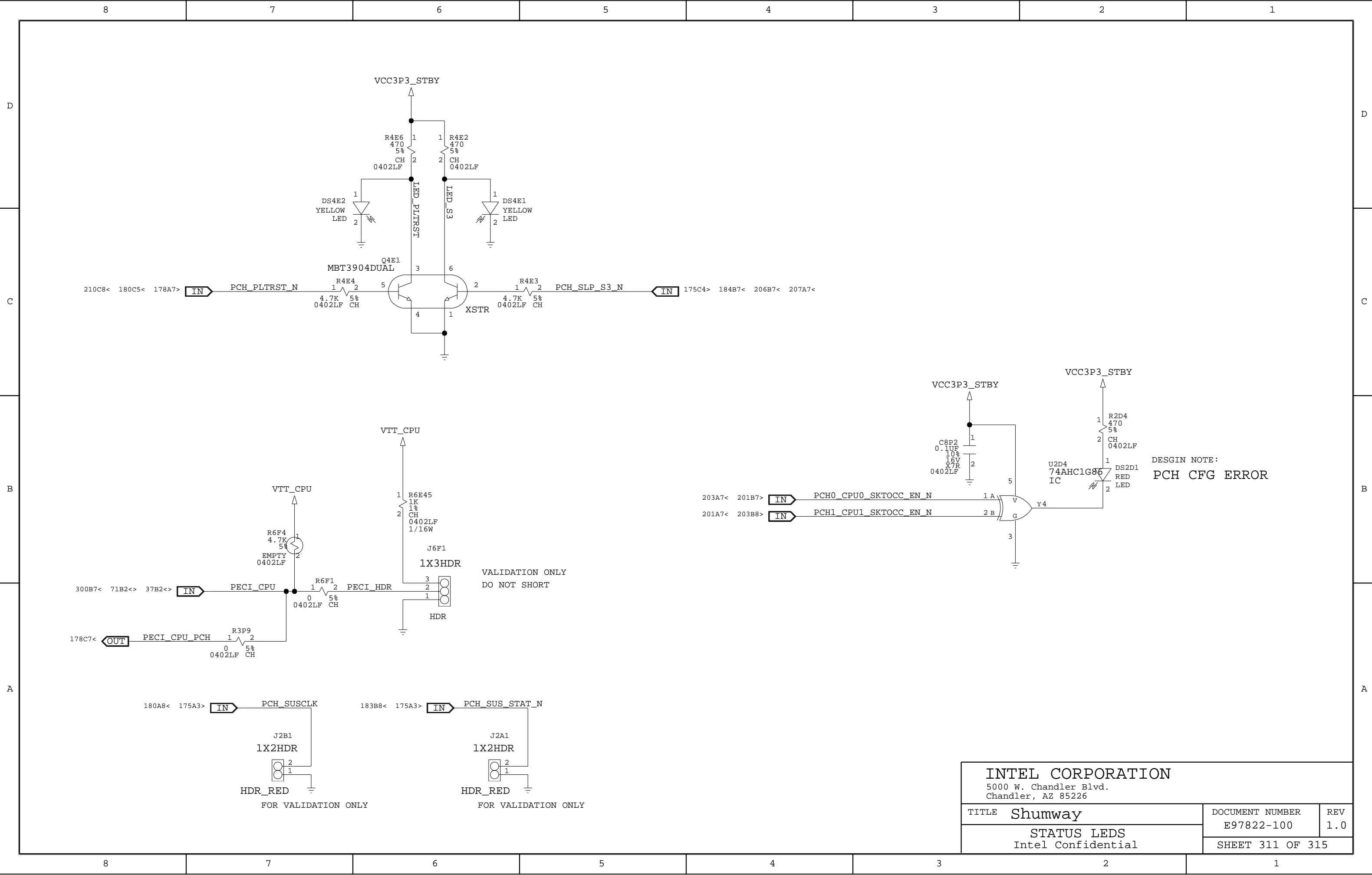
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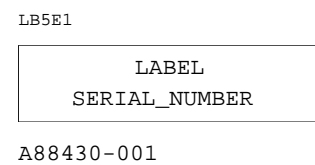
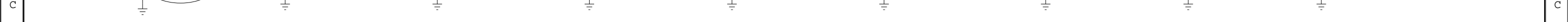


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D							
C							
B							
A							

Item#	Sch Page	Ref Designator	Voltage Name	Nominal Voltage	Active in States
0	306	J2A4	VCC3P3_PS	3.3V	S0
1	306	J2A5	VCC5_PS	5.0V	S0 - S5
2	306	J1A3	VCC12_PS	12.0V	S0
3	306	J2A7	VCC3P3_STBY	3.3V	S0 - S5
4	306	J2J2	VCC5_AUX	5.0V	S0 - S5
5	306	J1F5	VCC5_PS_STBY	5.0V	S0 - S5
6	306	J3J2	VCC1P8_PCH0_STBY	1.8V	S0 - S5
7	306	J3D5	VCC1P8_PCH1_STBY	1.8V	S0 - S5
8	306	J2A6	VCC3P3_AUX	3.3V	S0 - S5
9	306	J3J3	VCC1P0_PCH0_STBY	1.0V	S0 - S5
10	306	J3J1	VCC3P3_STBY_PCH0	3.3V	S0 - S5
11	306	J3D3	VCC1P0_PCH1_STBY	1.0V	S0 - S5
12	306	J3D2	VCC3P3_STBY_PCH1	3.3V	S0 - S5
13	307	J4H2	VCCDMI_PCH0	1.05V/1.0V	S0
14	307	J2H7	VCC1P5_PCH0	1.5V	S0
15	307	J3G1	VCC1P0_EP0_AUX	1.0V	S0 - S5
16	307	J4C2	VCCDMI_PCH1	1.05V/1.0V	S0
17	307	J3C1	VCC1P5_PCH1	1.5V	S0
18	307	J3B1	VCC1P0_EP1_AUX	1.0V	S0 - S5
19	307	J3J4	VCC1P8_PCH0	1.8V	S0
20	307	J3G2	VCC1P05_EP0_AUX	1.05V	S0 - S5
21	307	J2H8	VCC1P05_PCH0	1.05V	S0
22	307	J3D4	VCC1P8_PCH1	1.8V	S0
23	307	J3B2	VCC1P05_EP1_AUX	1.05V	S0 - S5
24	307	J2C6	VCC1P05_PCH1	1.05V	S0

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D							
C							
B							
A							

Item#	Sch Page	Ref Designator	Voltage Name	Nominal Voltage	Active in States
25	308	J5B1	VDDQ_EFG	1.5V	S0, S3 - S4
26	308	J5B2	VTT_DDR_EFG	0.75V	S0
27	308	J9H2	VDDQ_AB	1.5V	S0, S3 - S4
28	308	J5H2	VDDQ_CD	1.5V	S0, S3 - S4
29	308	J9H1	VTT_DDR_AB	0.75V	S0
30	308	J3G3	VCC1P8_EP0_AUX	1.8V	S0 - S5
31	308	J3B3	VCC1P8_EP1_AUX	1.8V	S0 - S5
32	308	J4J1	VCC3P3_PCH0	3.3V	S0
33	308	J4D6	VCC3P3_PCH1	3.3V	S0
34	308	J1K2	VCC3P3_EP0_AUX	3.3V	S0 - S5
35	308	J1B4	VCC3P3_EP1_AUX	3.3V	S0 - S5
36	308	J5H1	VTT_DDR_CD	0.75V	S0
37	309	J8D1	VTT_CPU1	1.05V	S0
38	309	J8G1	VTT_CPU0	1.05V	S0
39	309	J4G1	VCC1P0_EP1	1.0V	S0
40	309	J4C1	VCC1P0_PCH1	1.0V	S0
41	309	J4G1	VCC1P0_EP0	1.0V	S0
42	309	J4H1	VCC1P0_PCH0	1.0V	S0
43	310	J9C1	VCC_CPU1	1.1V*	S0
44	310	J7K2	VCC_CPU0	1.1V *	S0
45	310	J8A2	VCCPLL_CPU1	1.8V	S0
46	310	J7K3	VCCPLL_CPU0	1.8V	S0
47	310	J8A3	VCCSA_CPU1	0.85V*	S0
48	310	J6J1	VCCSA_CPU0	0.85V*	S0

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