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D							D	
C	GALILEO GEN2						C	
	INTEL QUARK X1000							
B	FAB H						B	
	PB: H48142-207							
	PBA:H48125-800							
A							A	
						<div>INTEL CORPORATION</div> <div>2111 NE 25TH AVENUE</div> <div>HILLSBORO OR 97124</div>		
						TITLE GALILEO Gen2	DOCUMENT NUMBER H38681	REV 2.0
						DESIGN TITLE PAGE		SHEET 1 OF 28
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Thu Sep 11 08:52:51 2014

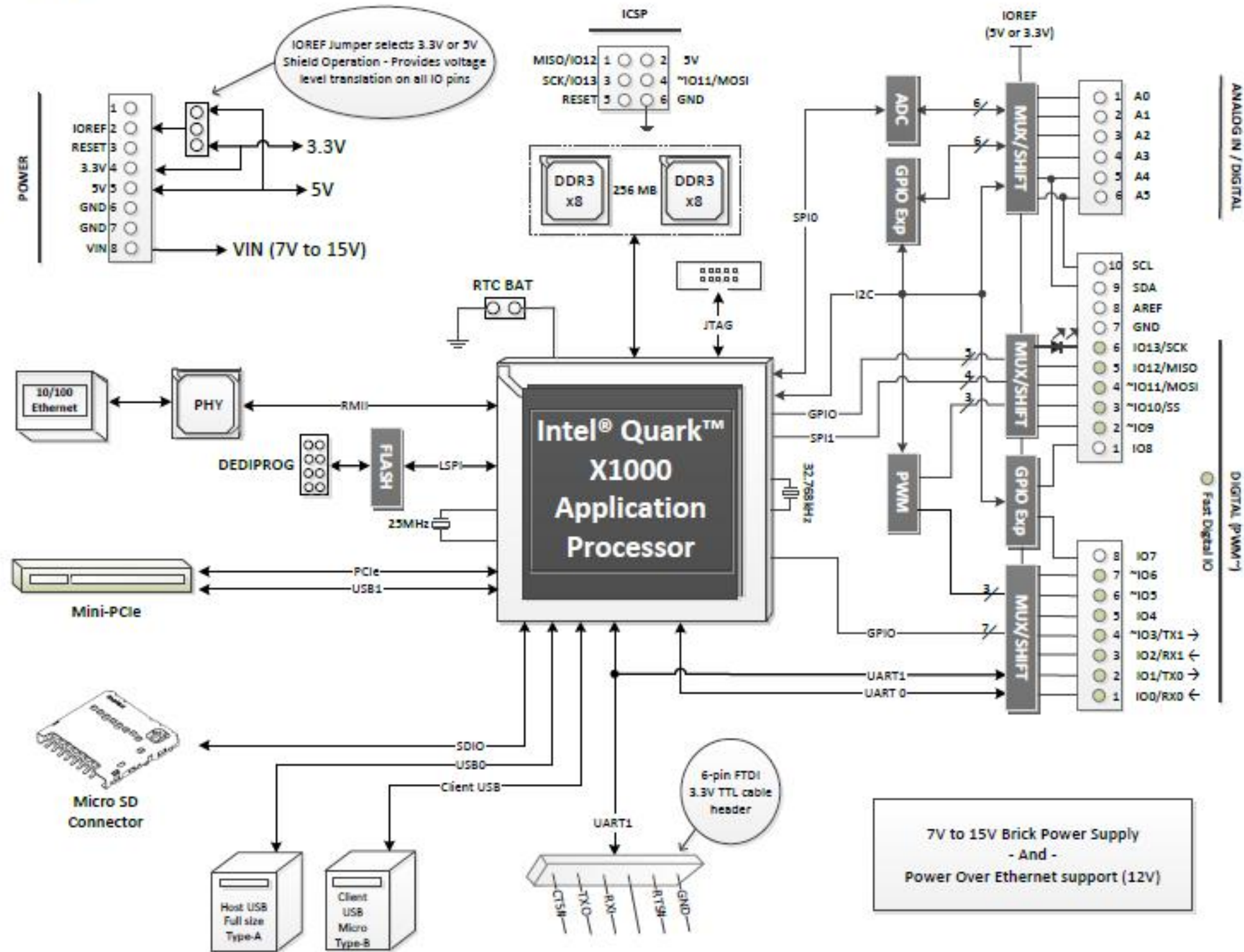
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	1		DESIGN TITLE PAGE																																							
	2		TABLE OF CONTENTS																																							
	3		DISCLAIMER																																							
	4		SYSTEM BLOCK DIAGRAM																																							
	5		QUARK DDR3 & PCIE																																							
	6		QUARK GPIO																																							
	7		QUARK MISC																																							
	8		QUARK POWER																																							
	9		QUARK DECOUPLING																																							
C	10		SDRAM 1																																							
	11		SDRAM 2																																							
	12		SDRAM TERMINATION																																							
	13		MINI PCIE CONNECTOR																																							
	14		MICRO SD CONNECTOR																																							
	15		USB CONNECTORS																																							
	16		UART 1 & JTAG																																							
	17		LAN																																							
	18		SPI: ADC&FLASH																																							
	19		QUARK STRAPS																																							
B	20		EXTERNAL IO MUXING 1																																							
	21		EXTERNAL IO MUXING 2																																							
	22		LVL B BUFFER																																							
	23		LVL C BUFFER																																							
	24		AMUX & EXTERNAL IO																																							
	25		VOLTAGE REGULATORS																																							
	26		VOLTAGE REGULATORS																																							
	27		VOLTAGE REGULATORS																																							
	28		POWER BUTTONS & MISC																																							
A																																										
Thu Mar 03 10:58:31 2011										<table><tr><td colspan="6">INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124</td><td colspan="6">DOCUMENT NUMBER: H38681</td></tr><tr><td colspan="6">TITLE: GALILEO Gen2 TABLE OF CONTENTS</td><td colspan="3">REV: 2.0</td><td colspan="6">SHEET 2 OF 28</td></tr></table>						INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124						DOCUMENT NUMBER: H38681						TITLE: GALILEO Gen2 TABLE OF CONTENTS						REV: 2.0			SHEET 2 OF 28					
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124						DOCUMENT NUMBER: H38681																																				
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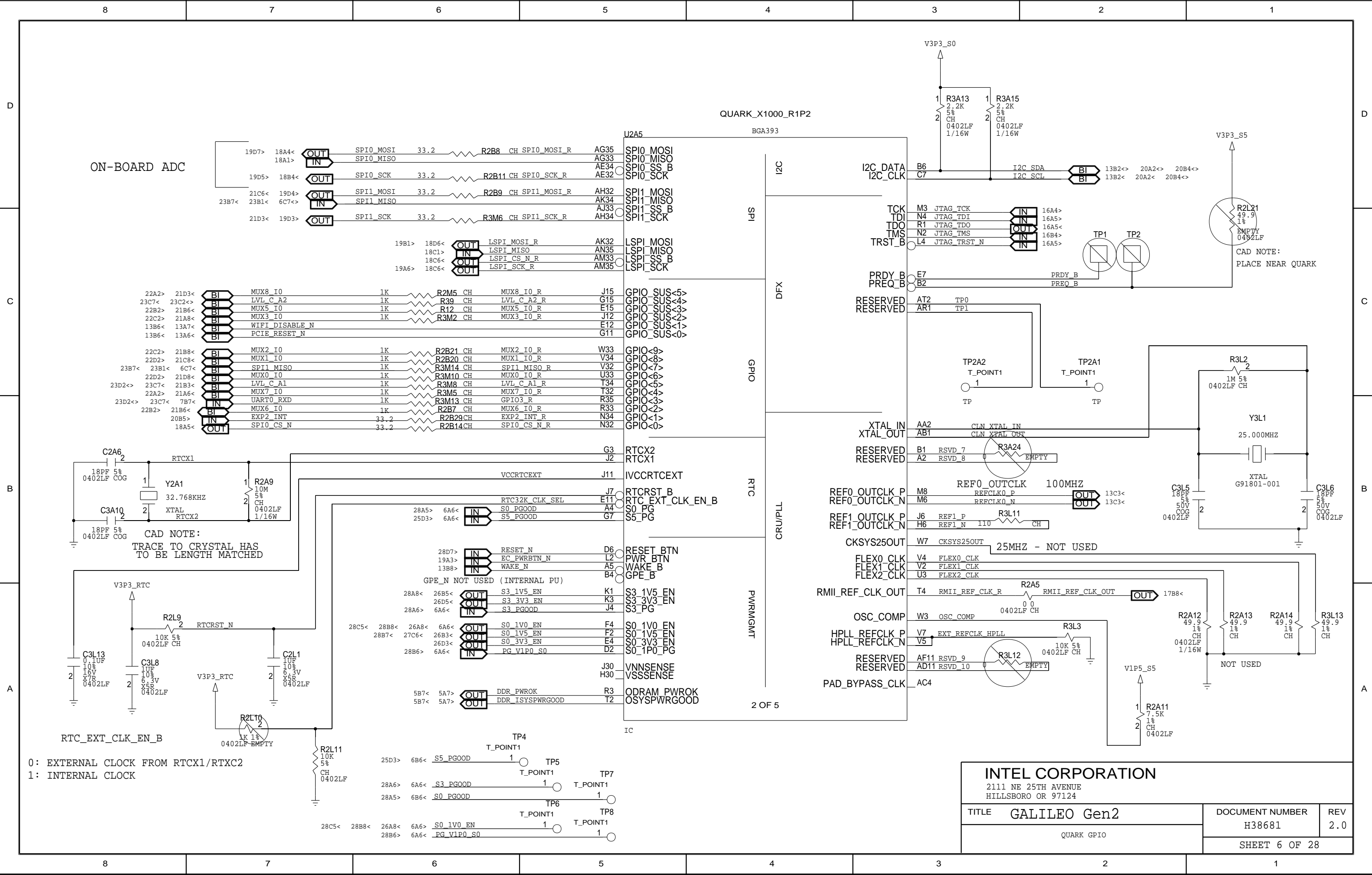
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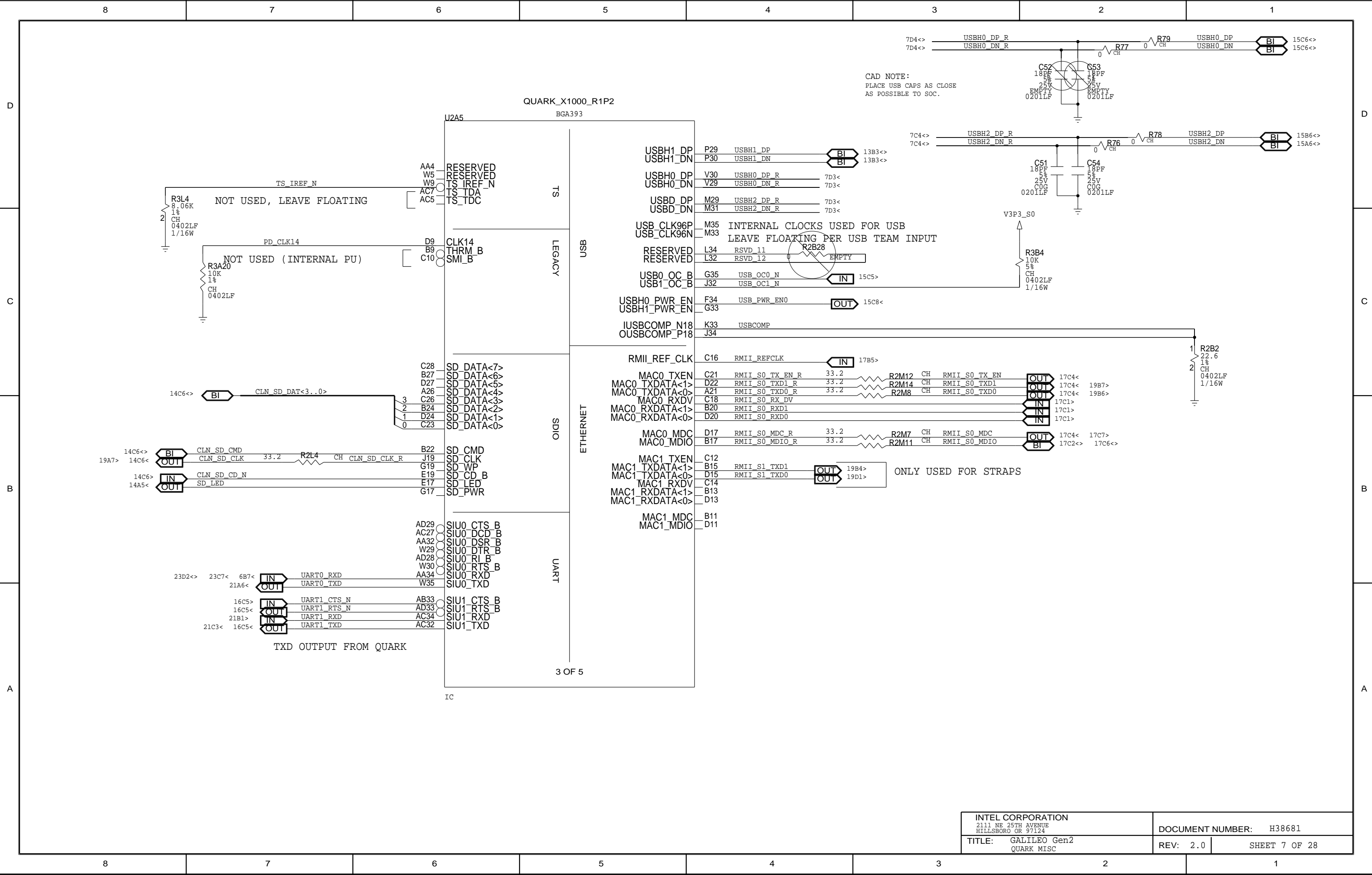
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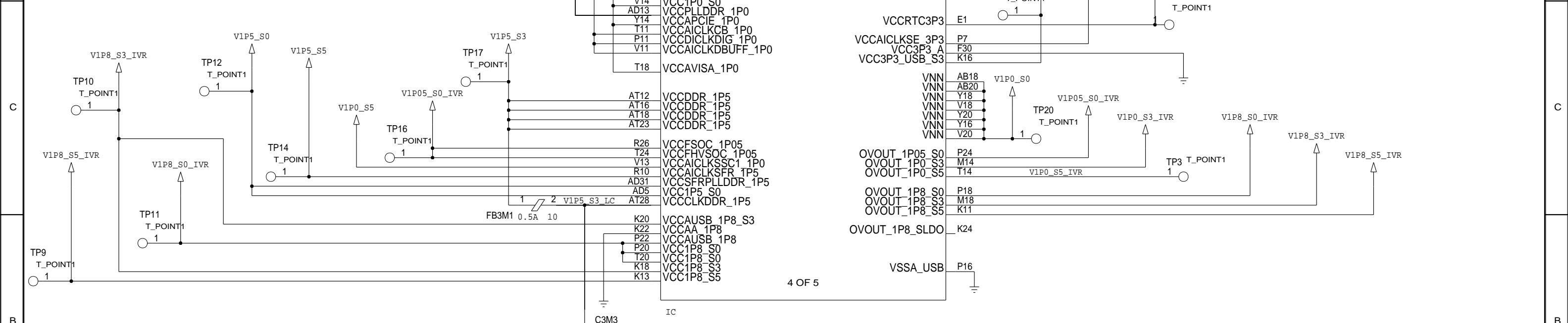
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May/2014



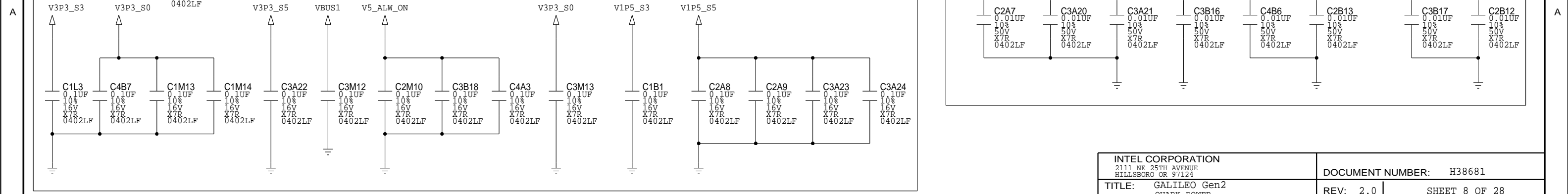




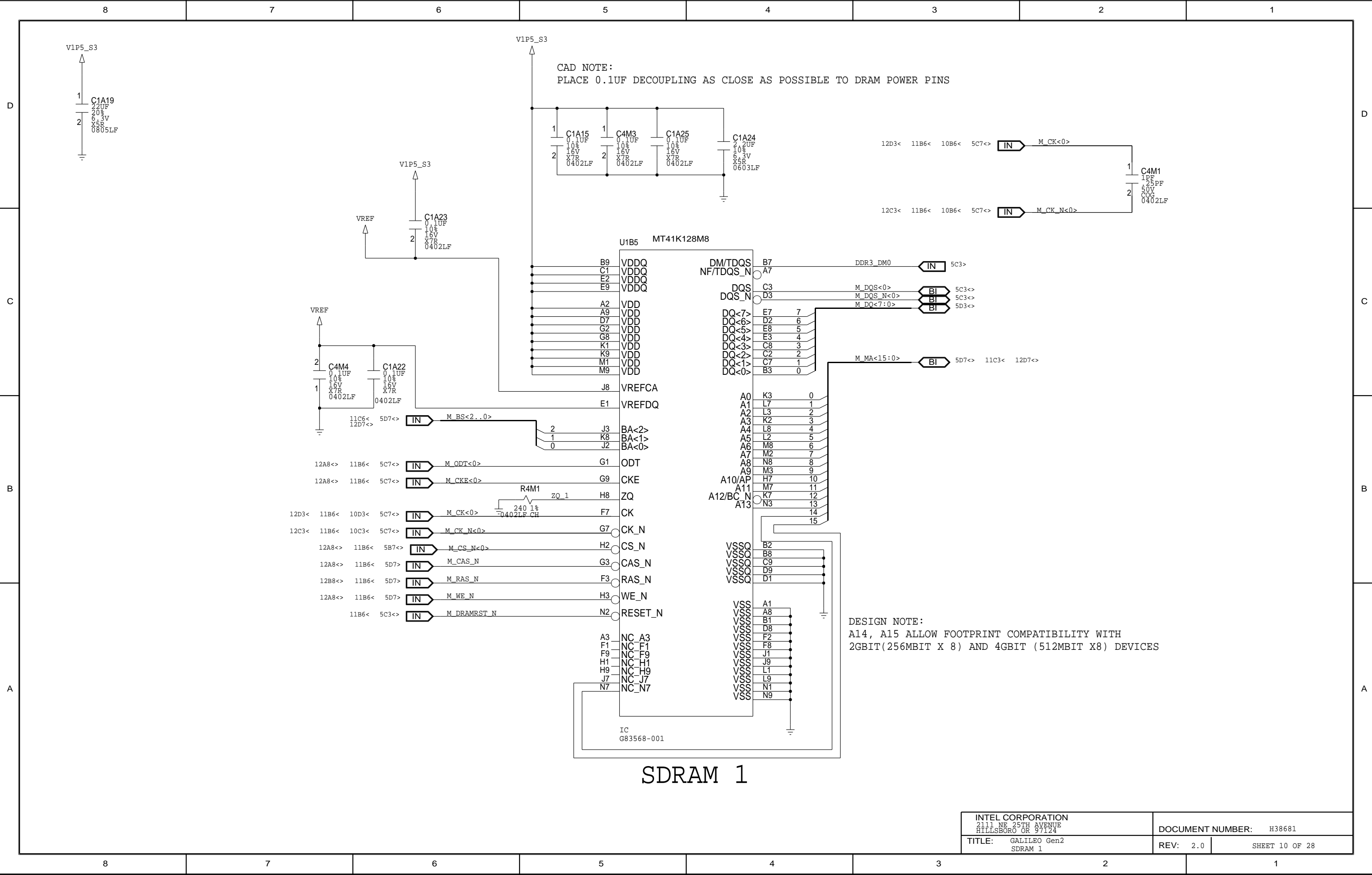




PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

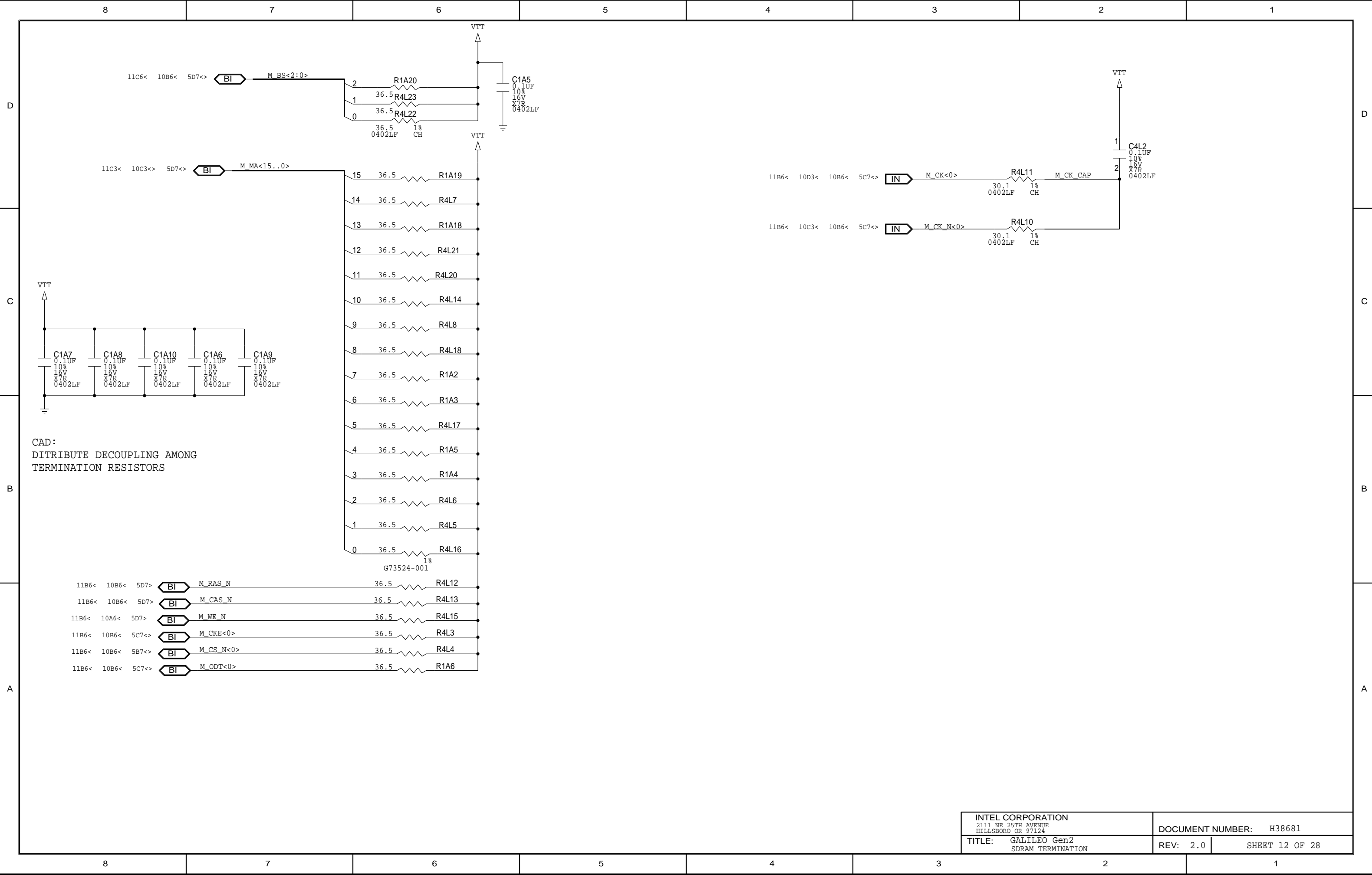


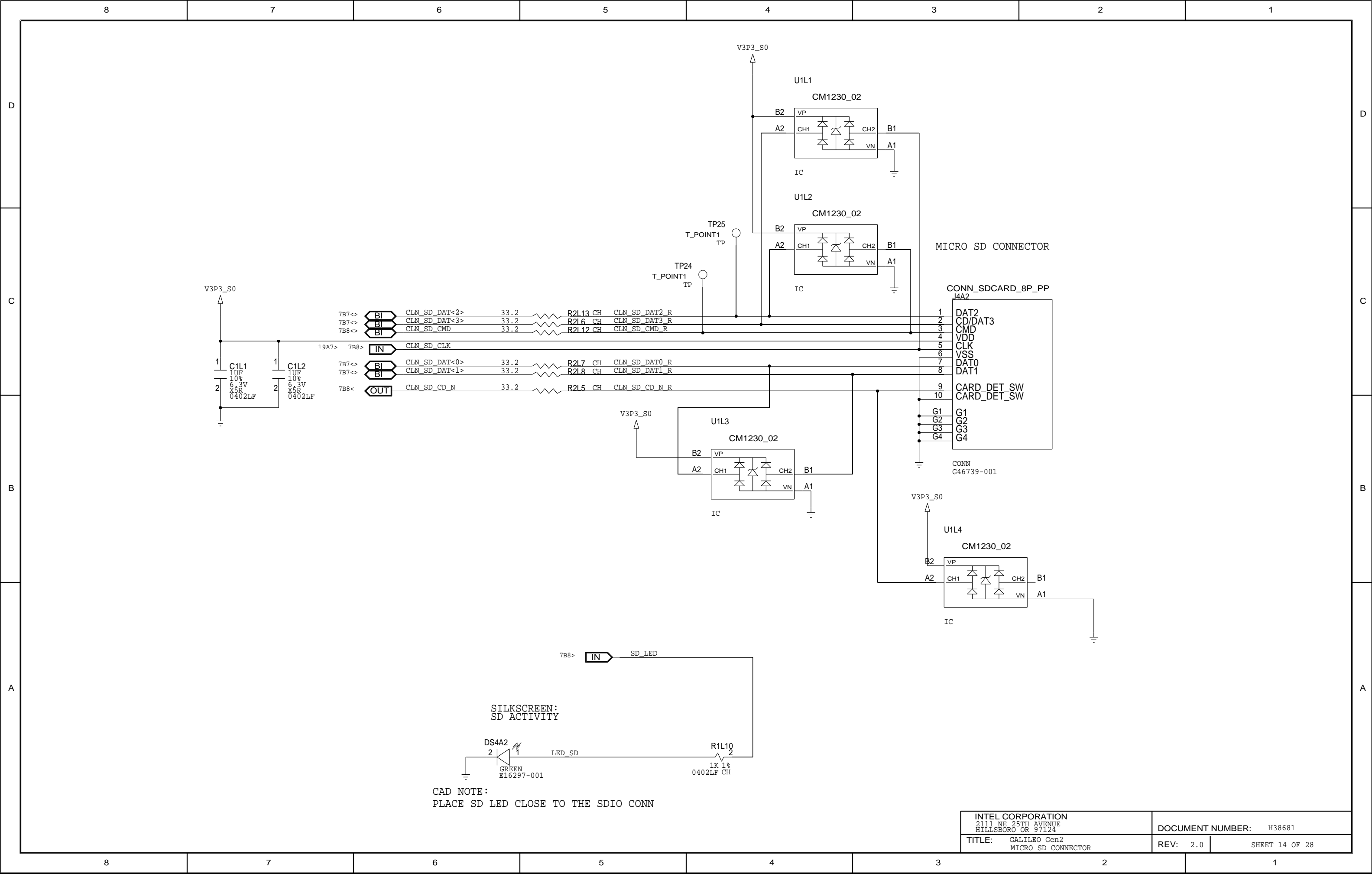


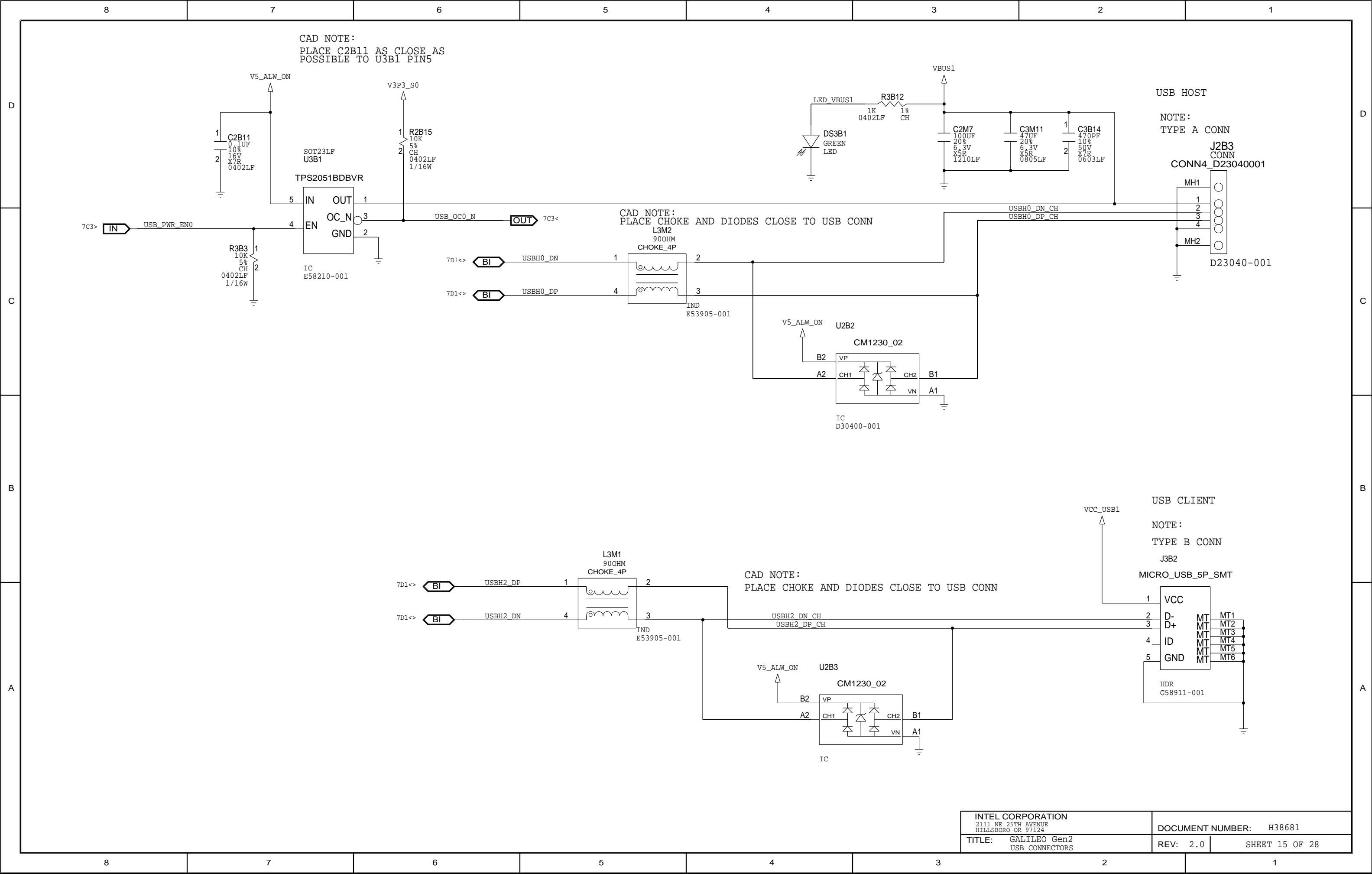


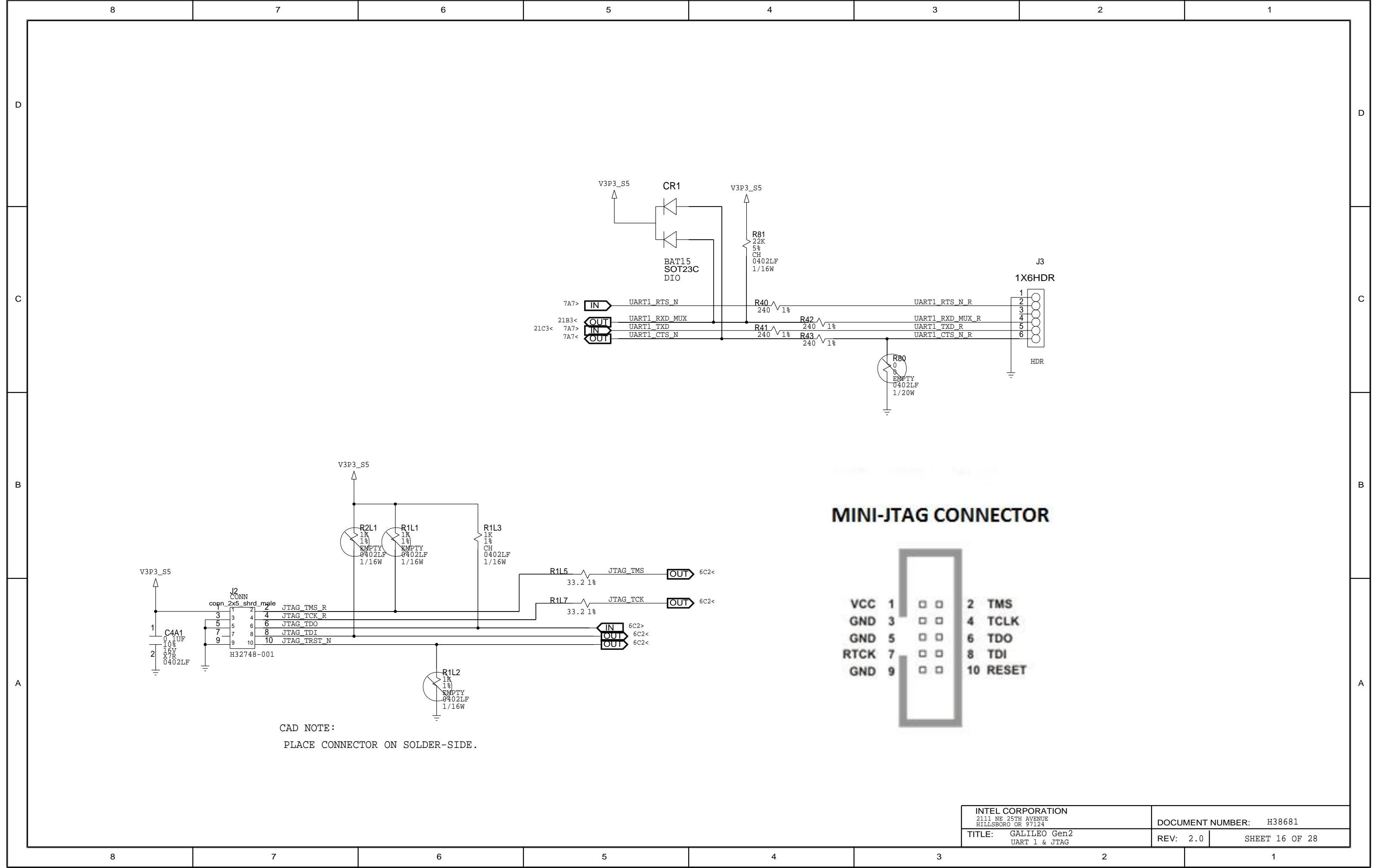


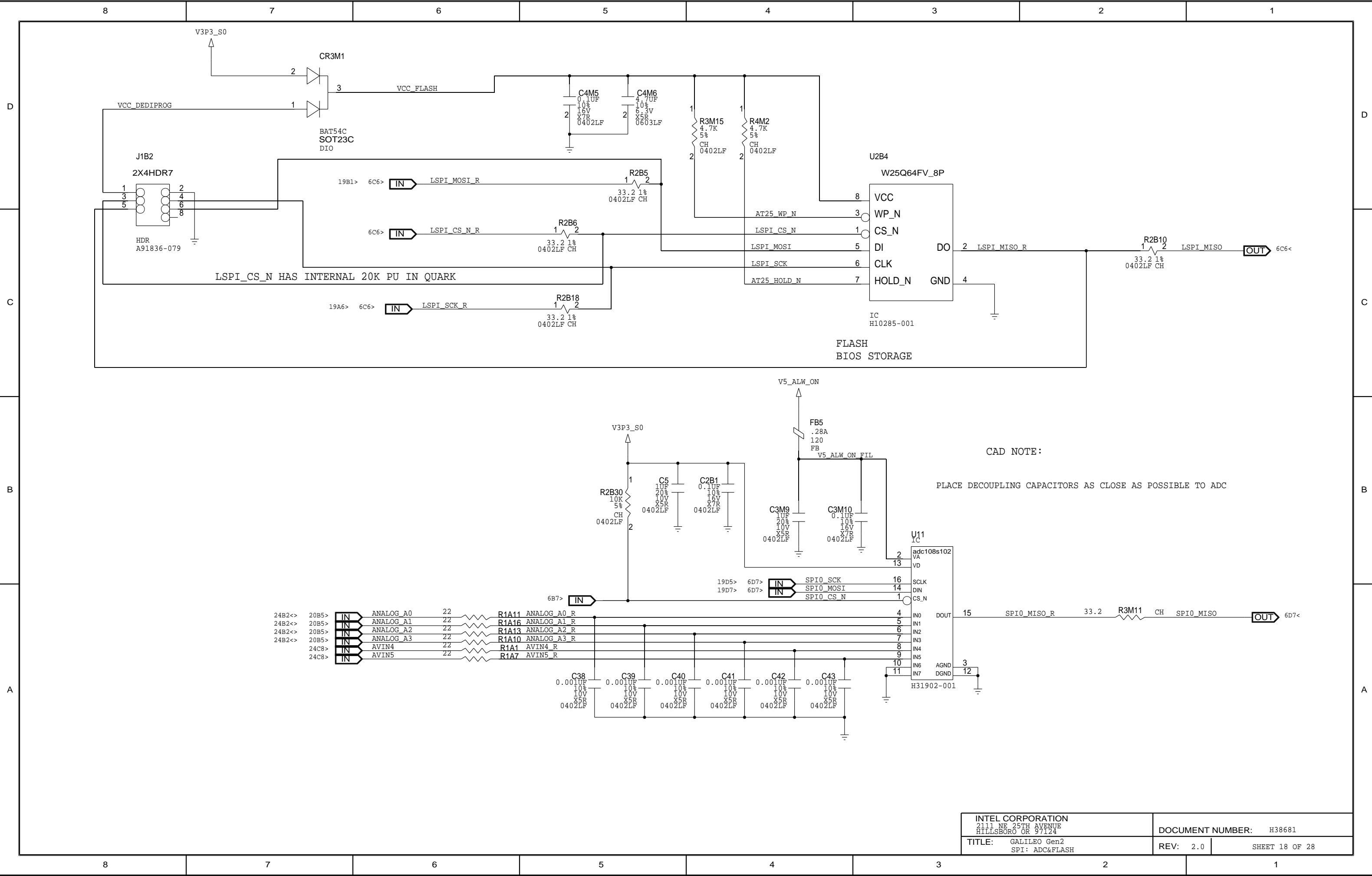
DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH
2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES

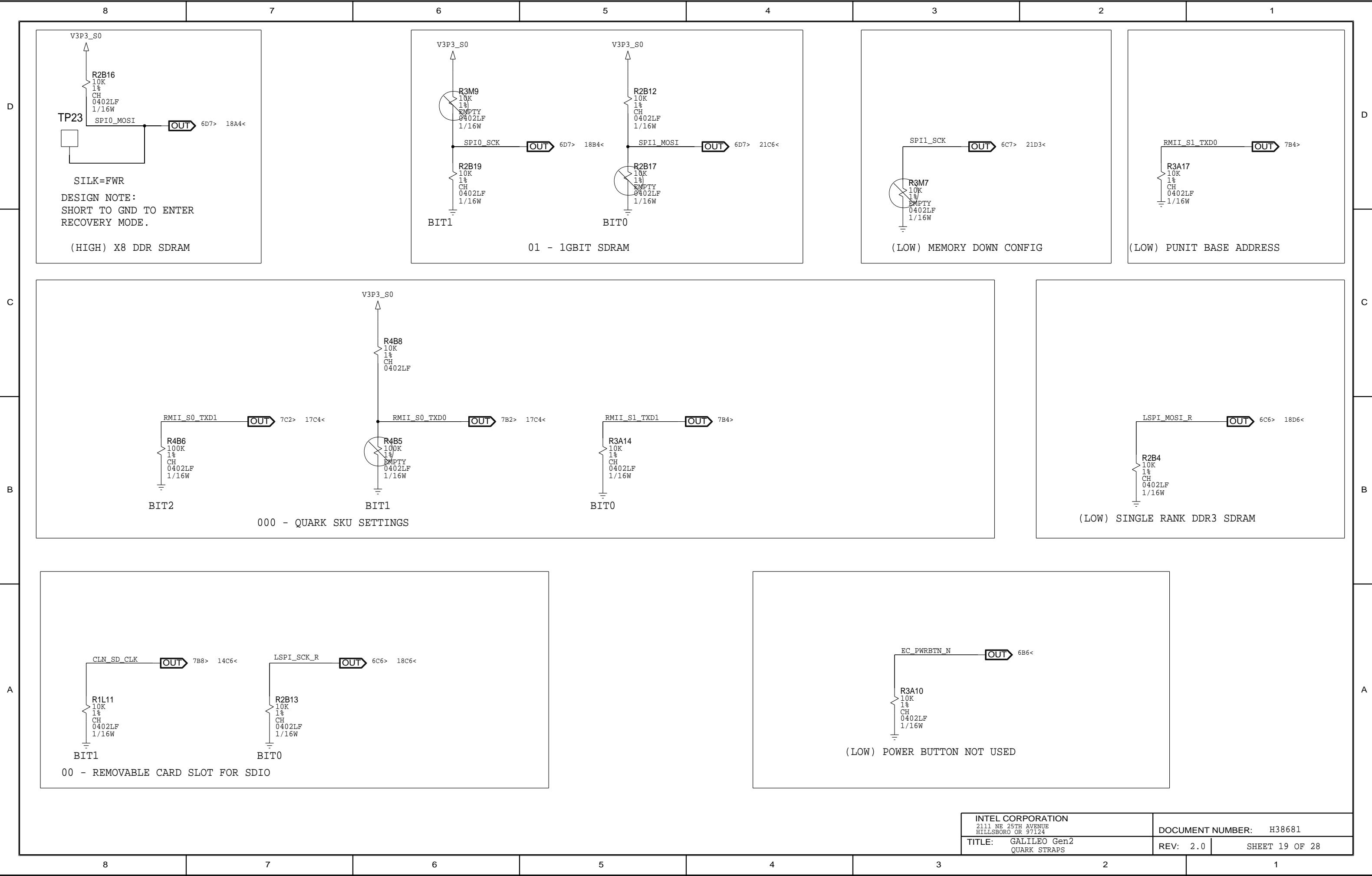


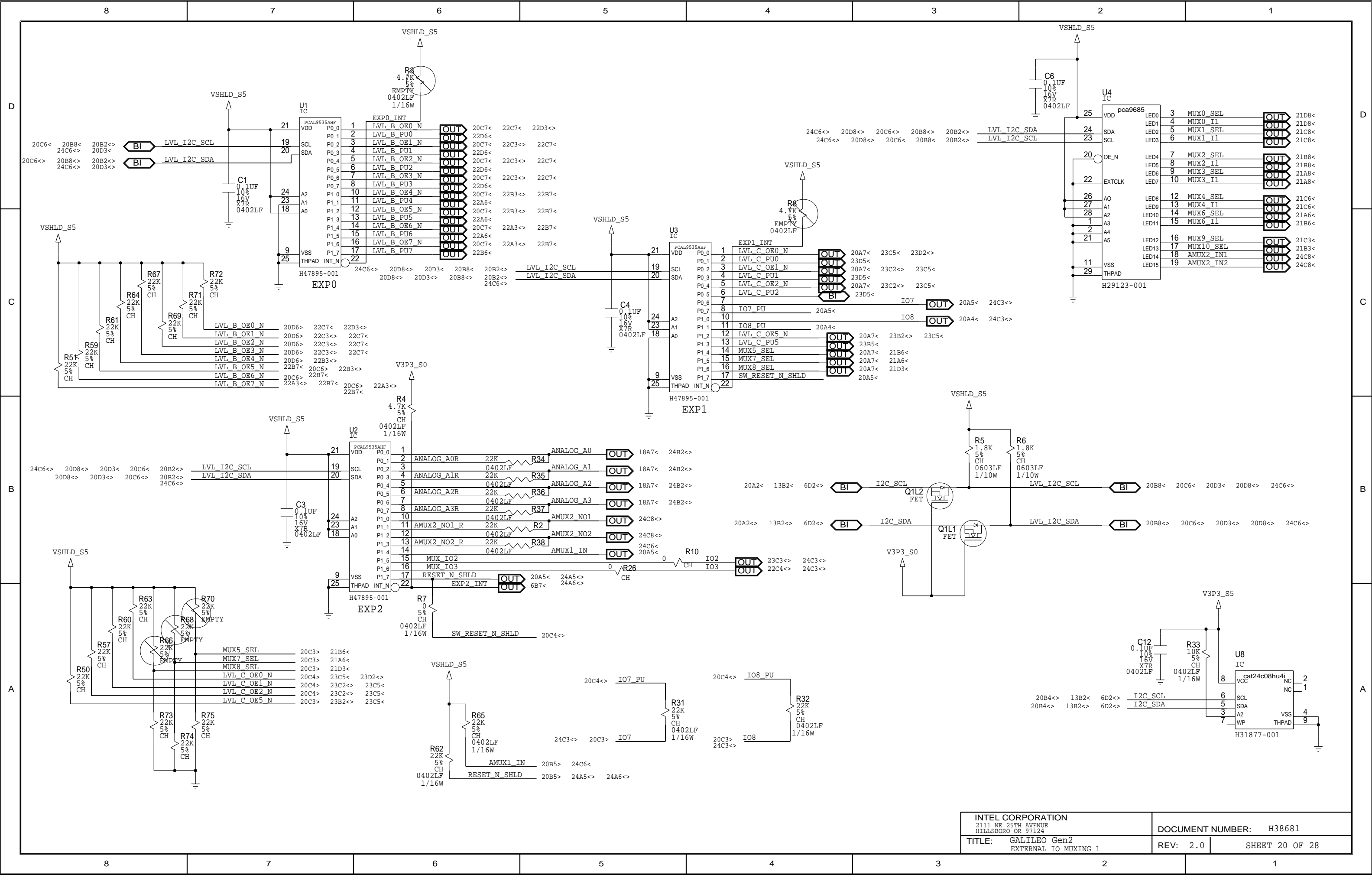


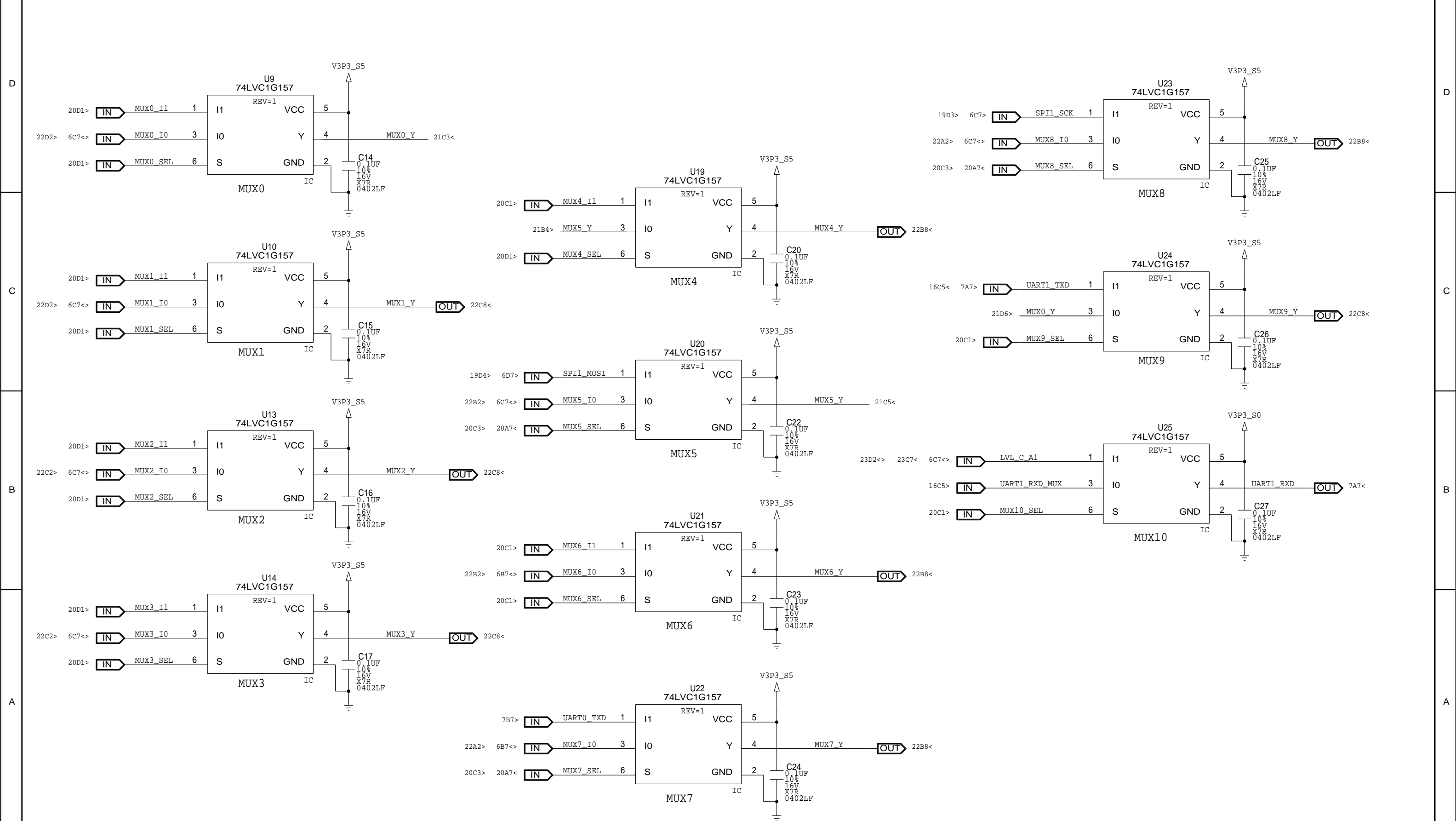


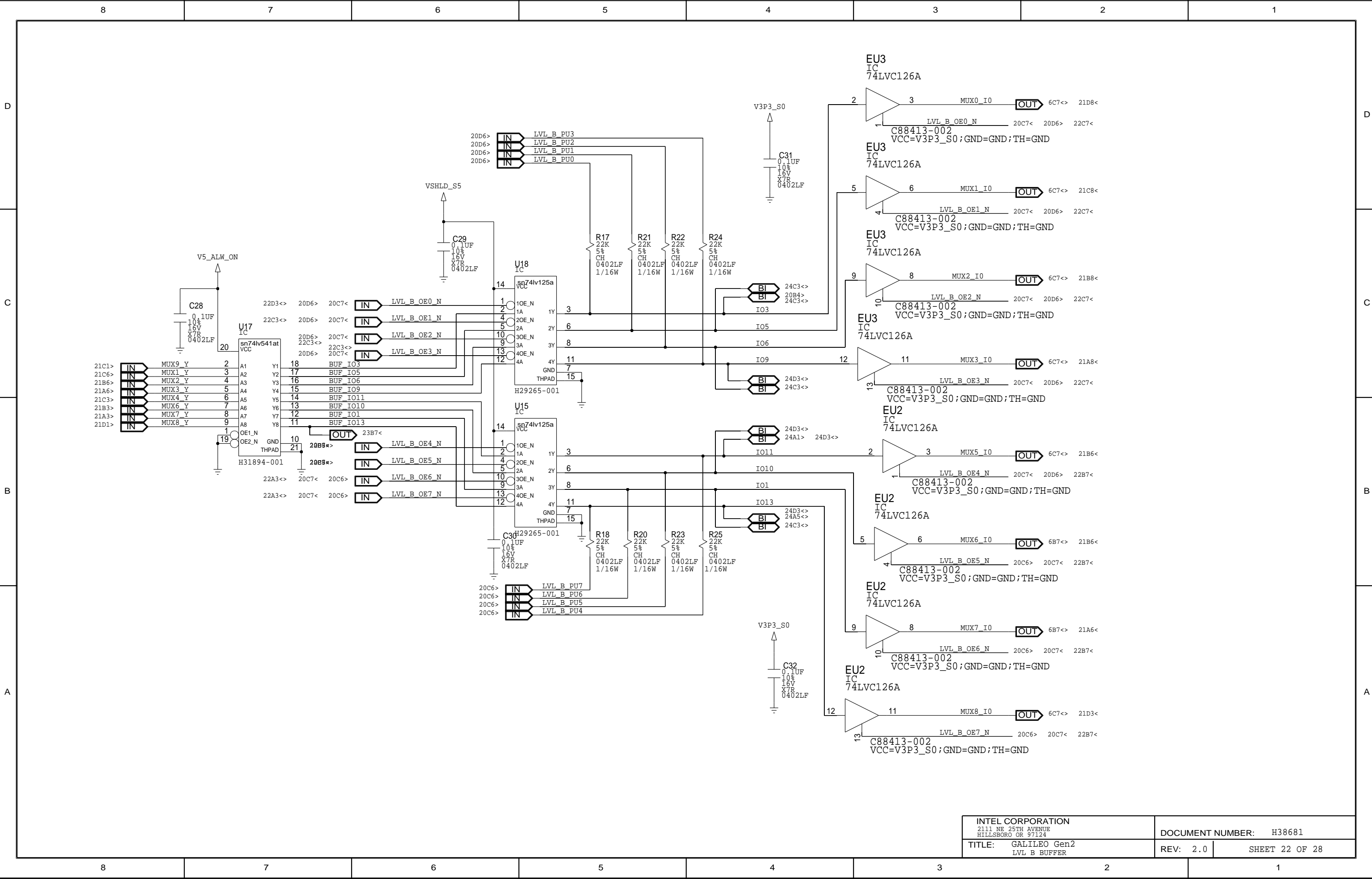




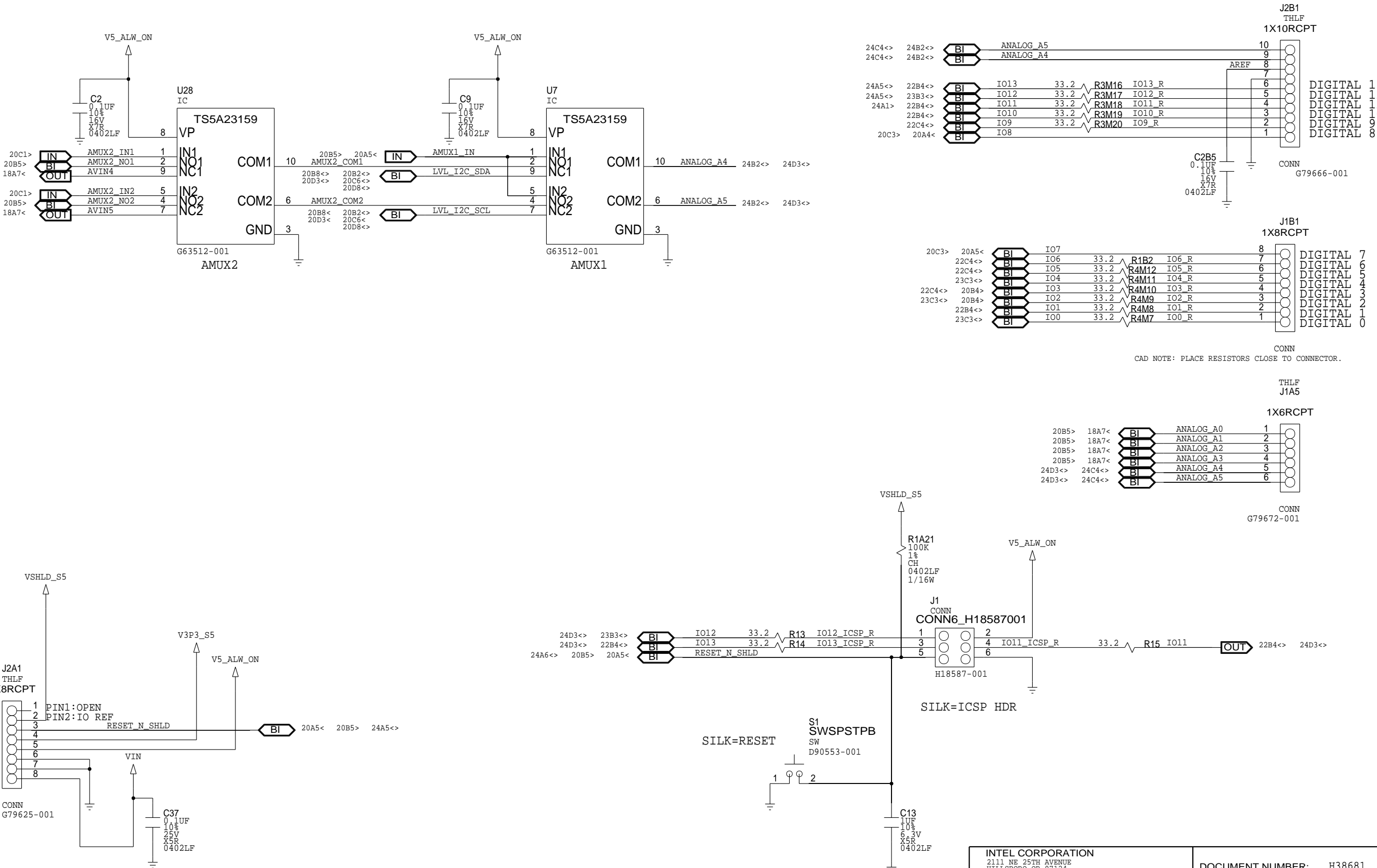








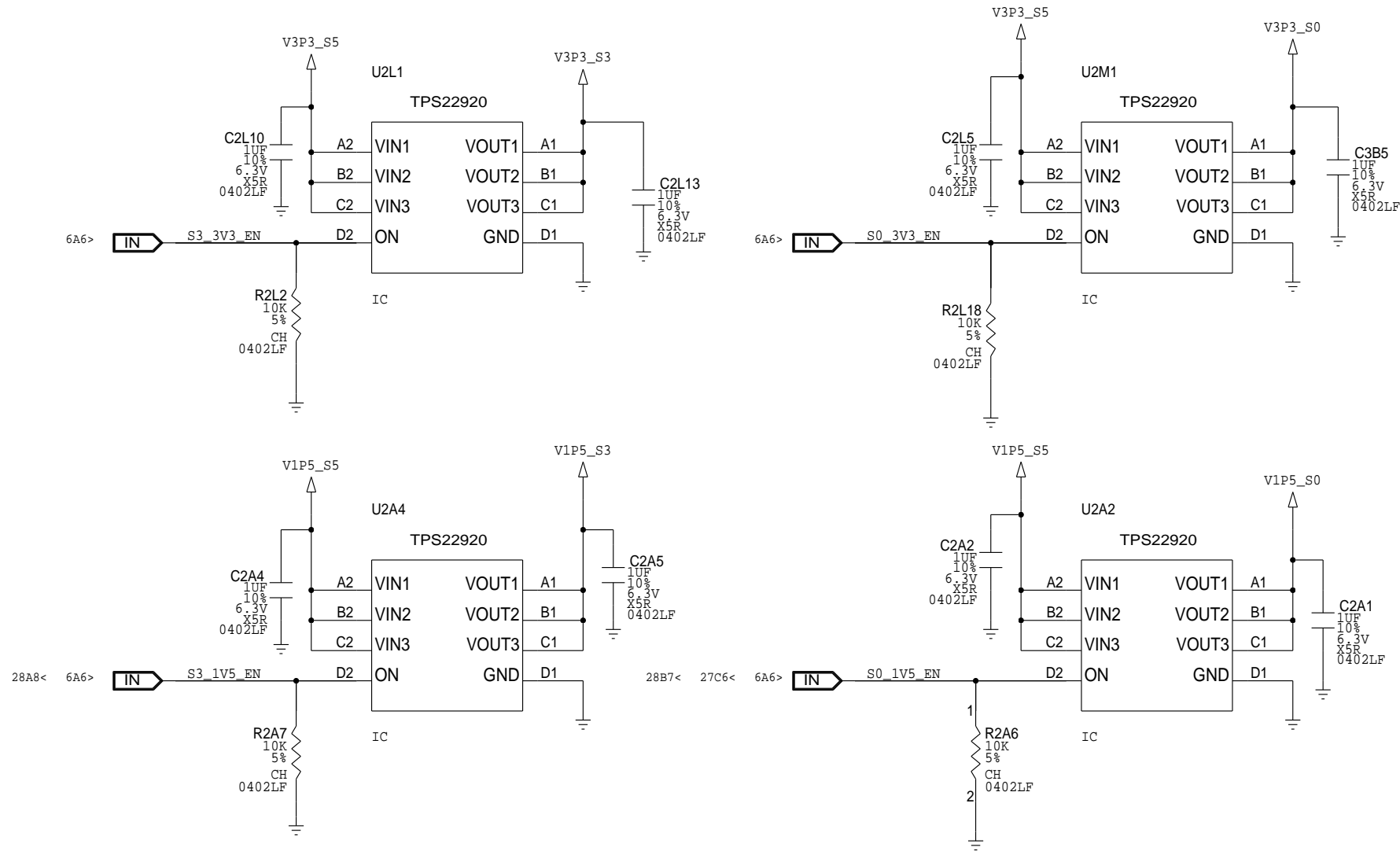




V3P3_S5 IS GENERATED W ON-BRD REGULATOR

V1P5_S5 IS GENERATED W ON-BRD REGULATOR

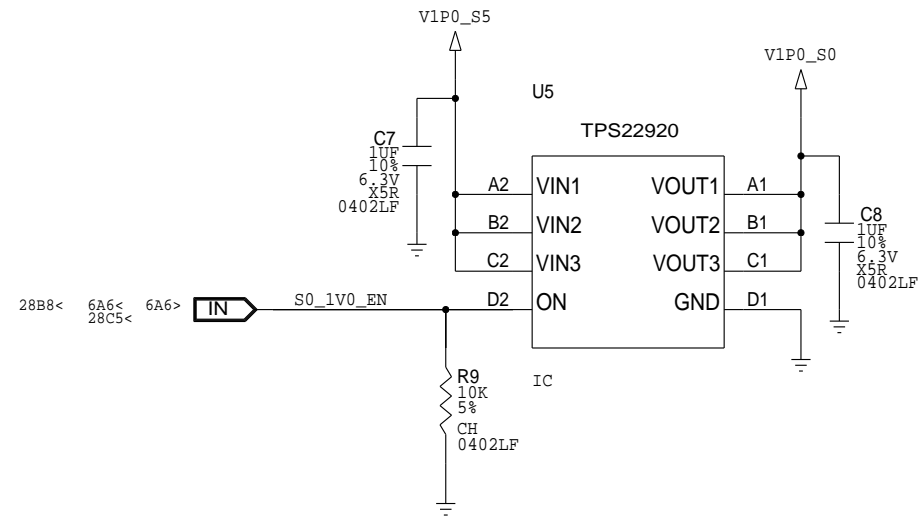
V1P0_S5 IS GENERATED W ON-BRD REGULATOR



CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

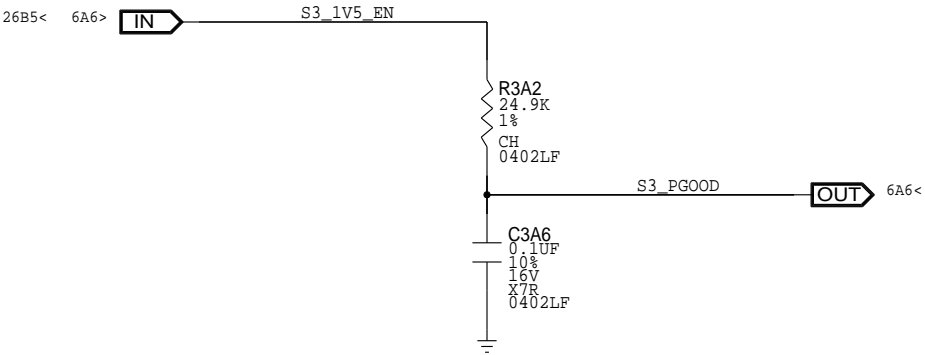
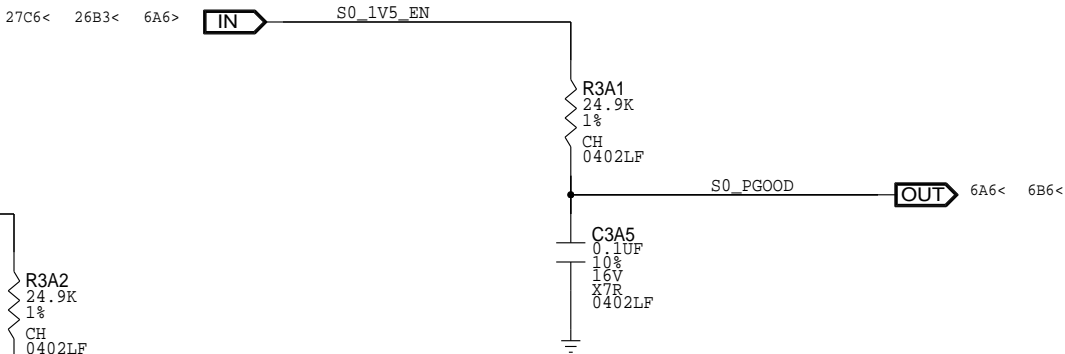
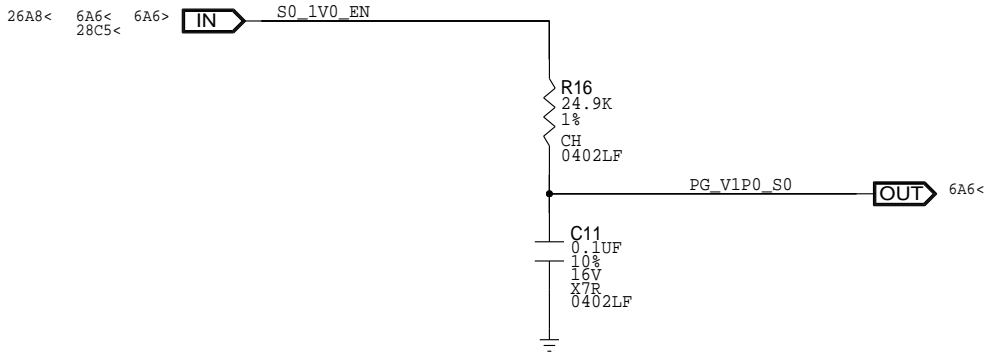
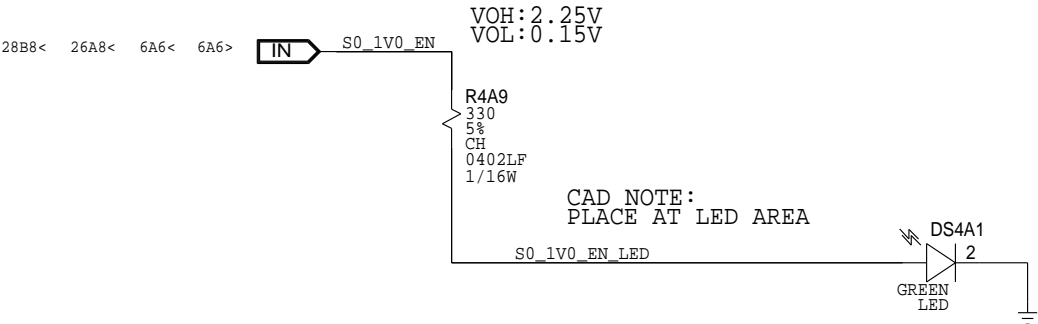
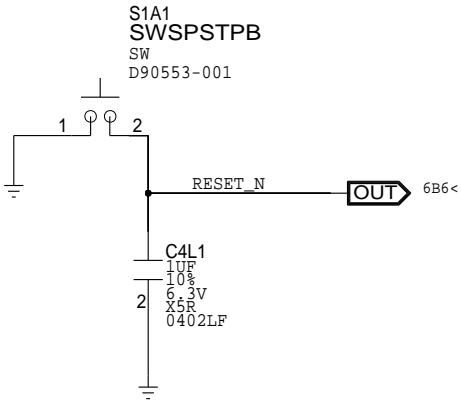
V1P0_S3 IS GENERATED INTERNALLY

V1P0_S0 IS GENERATED W ON-BRD REGULATOR

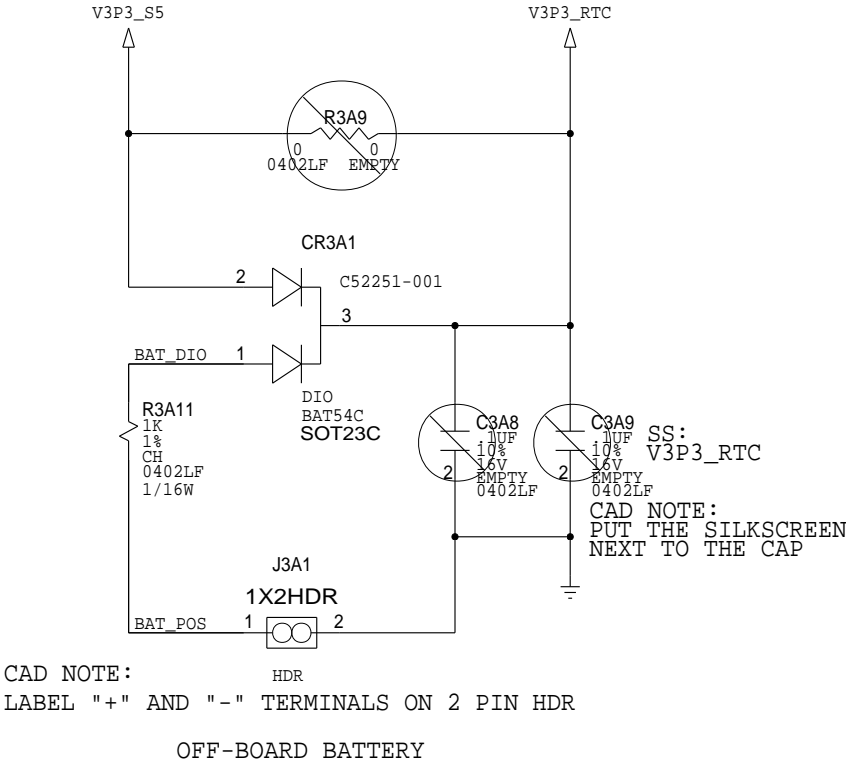


NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3

SS:
REBOOT BUTTON



PG DELAY



CAD NOTE:
LABEL "+" AND "-" TERMINALS ON 2 PIN HDR

OFF-BOARD BATTERY

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 POWER BUTTONS & MISC		REV: 2.0	SHEET 28 OF 28