

Intel® Joule™ compute module

96B compatible expansion board Technical Guide

Revision = 1.0

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Revision History

Revision Number	Description	Revision Date
1.0	Initial public release of the reference design package.	June 2017

1 Introduction

1.1 Document organization

This document combines information that you would normally find in a User Guide with information normally found in a Hardware Guide. This Technical Guide provides information for the Intel® Joule™ platform when using the 96Boards* - compatible carrier board reference design, from this point referred to as the 96B compatible carrier board.

The user guide portion covers platform assembly, port identification, recommended accessories, workstation recommendations and the functional steps of BIOS update and power on, in the next two sections.

Once you successfully power on the platform, functional control is given to the installed operating system. Follow established methods for installing a chosen operating system on an Intel Joule module based development platform. Refer to <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Choosing your OS* for additional information.

The hardware guide portion provides technical information regarding platform subsystems, external interfaces, component recommendations, and board layout suggestions to facilitate design modifications in sections 4-14.

The 96B compatible carrier board is a functional reference design and shall not be considered a validated product. Where possible, known errata and electrical workarounds are fully disclosed.

1.2 Scope

The material provided within this publication is intended to accelerate the development of products powered by the Intel Joule compute module by providing a reference board that is based on the 96Boards* Consumer Edition specification.

It is important to note that the Intel 96B compatible carrier board is not offered by Intel as retail product. The intent of this reference design is to demonstrate functionality within a layout and configuration familiar to those who have worked on other 96Boards* products.

Scope of this document is limited to functions performed by the 96B compatible carrier board.

Consult datasheets from the original device manufacturer and available information provided by the operating system vendors for software environments to fully understand options available.

Additional information may be available outside of this publication. Contact your Intel business representative for the latest information regarding CAD files, material lists, and schematics.

1.3 Intended audiences

Board Design Teams

This document provides technical guidance at a level appropriate for those experienced in working with similar products. Where possible, discrete component and device manufacturers are referenced as suggestions. No regulatory certification is implied by use of recommendations.

See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Expansion Board Design Guide* for additional information.

Validation and Support Teams:

The user guide provides sufficient information to power on the reference design, install an operating system, and exercise the primary interfaces. Many features require specific software elements that may not be available in all board support packages or operating systems.

See <https://software.intel.com/en-us/intel-joule-getting-started> for additional information.

Documentation Content Teams:

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1.4 Acronyms and terminology

Term	Definition
BIOS	Basic Input/Output System
BOM	Bill of Materials
CAD	Computer Aided Design
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read Only Memory
EMI	Electro-Magnetic Interference
eMMC	Embedded Multi-media Card
ESD	Electro-Static Discharge

Term	Definition
FET	Field Effect Transistor
FS	Function Select
GPIO	General Purpose Input Output
HDMI	High Definition Multi-media Interface
LED	Light Emitting Diode
MISO	Master In Slave Out
MOSI	Master Out Slave In
ODM	Original Design Manufacturer
OS	Operating System
PCB	Printed Circuit Board
PWM	Pulse Width Modulated
RF	Radio Frequency
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VR	Voltage Regulator

1.5 References

Document	Document Location
Intel® Joule™ Online Guide which includes: <ul style="list-style-type: none"> • Getting Started • Programmers Guide • Compute Module Datasheet • Expansion Board Design Guide • Expansion Board Datasheet • Accessories • Troubleshooting and FAQ 	https://software.intel.com/en-us/intel-joule-getting-started
96Boards™ Consumer Edition, Low Cost Hardware Platform Specification, Rev 1.0, January 2015	http://www.96boards.org/specifications/

2 Platform Assembly

2.1 Tools and materials needed

The following items are required to completely assemble the reference platform. Users will need to make modifications and adjustments to their design to accommodate their specific design objectives.

Table 1. Platform assembly checklist

Items	Description / Usage
Intel Joule compute module	One Intel Joule compute module is required per reference 96B compatible carrier board design.
96Boards* compliant board	This is the 96Boards* (non-extend A or B version) that will accept the Intel Joule module.
Active heatsink for Intel Joule compute module (optional)	Instructions in this document are specific to the reference active heatsink for the Intel® Joule™ module. See also https://store.gumstix.com/fansink-intel.html . Other heatsink options are available; refer to Section 2.6.
Board standoffs and hardware	A standoff of at least 0.25" must be installed at each mounting location on the 96B compatible carrier board. This will stabilize and level the board during development and also provides protection for devices attached to the bottom side of the board.
Power supply	<p>The 96B compatible carrier board accepts a (male) barrel connector with a 1.7mm center pin (positive) and 4.75mm outer ring (ground). We used an Autec* WM24P6-12-A-QL.</p> <p>The supply must be capable of providing 12 VDC at 2 Amps.</p> <p>Note: 2 A covers basic platform operation. Attached accessories and peripherals can increase the power needed at the input.</p>
Keyboard and mouse (optional)	Input devices are used to perform development tasks on the platform; headless configuration and operation is possible, yet initial tasks are best performed directly upon the platform.
Cables and accessory devices	<p>Various cables and accessories will be required to connect display device, sensors, mass storage, and test equipment.</p> <p>At a minimum this includes:</p> <ul style="list-style-type: none"> • USB type C cable between platform and workstation • Standard HDMI cable between platform and display device.

2.2

2.3 Board layout overview

This section describes the location of physical interfaces on the 96B compatible carrier board. Where possible references designators from the schematic are provided on the figures.

Figure 1. 96B compatible carrier board layout.top view

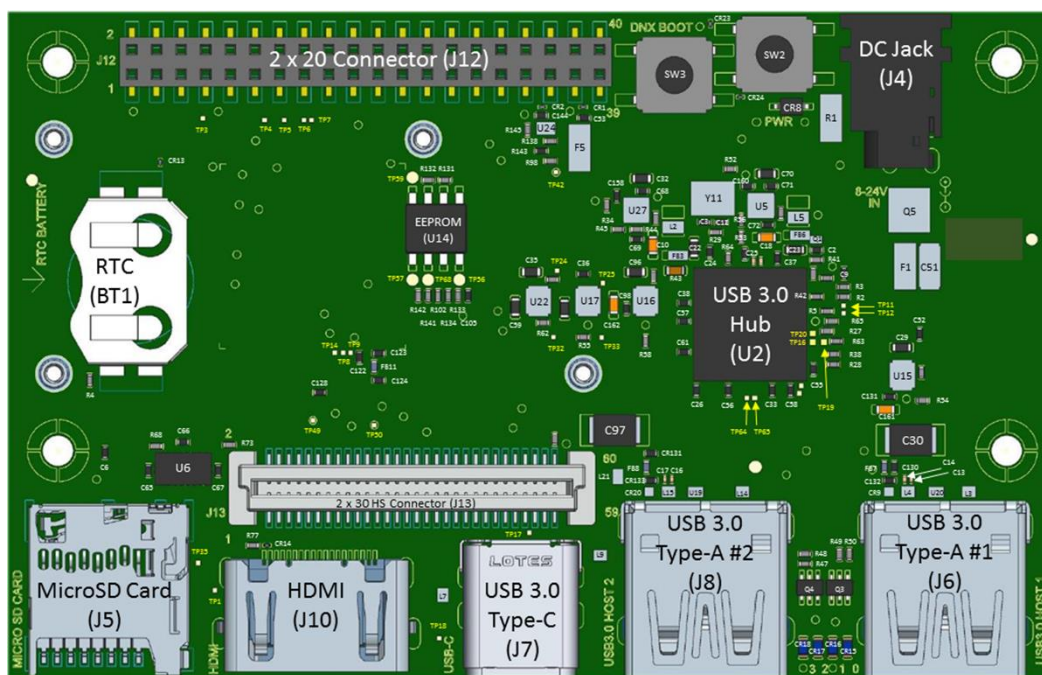
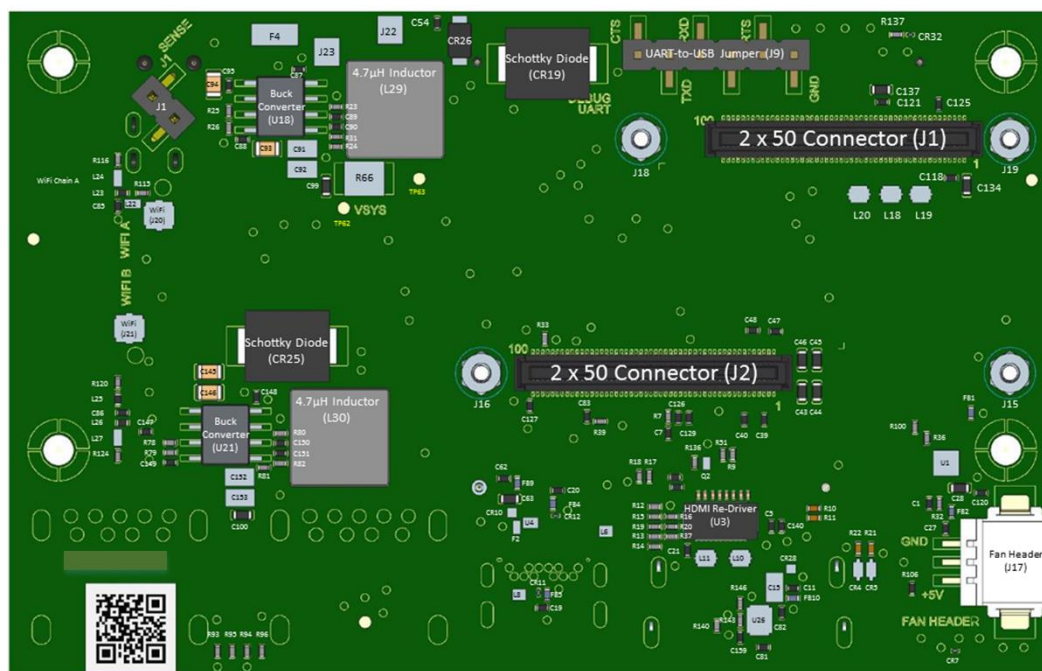


Figure 2. 96B compatible carrier board layout.bottom view without module installed



The Intel Joule compute module attaches to the bottom side of the 96B compatible carrier board and is retained with M1.6 size hardware that passes through the four inserts of the module and into board mounted captive nuts or other retention solutions.

2.4 Module installation and removal

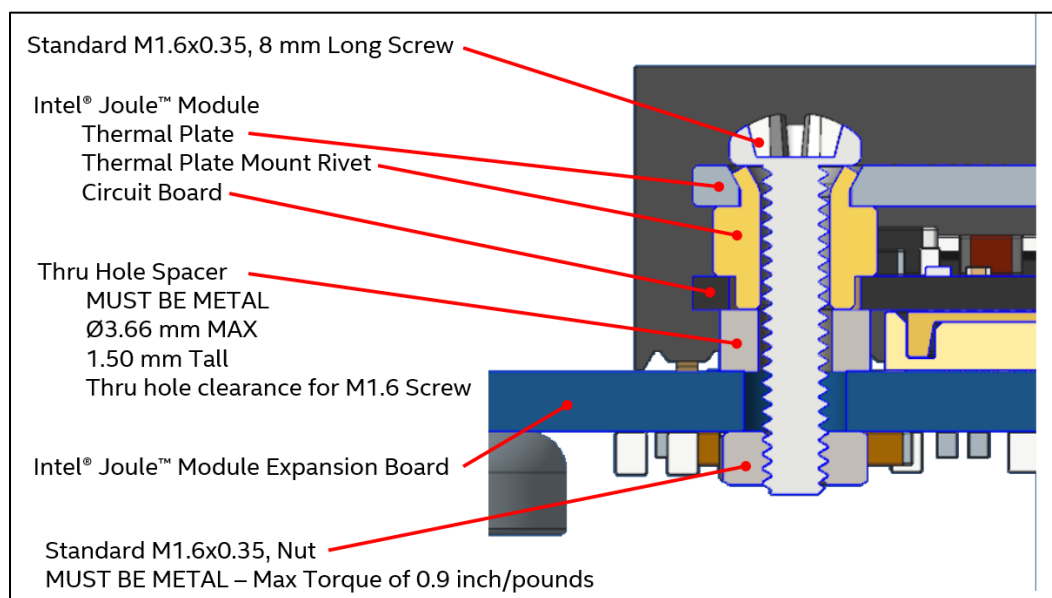
See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Module Datasheet* for specific handling information. The board to board connectors on the module are rated at 30-maximum connect-disconnect cycles.

2.4.1 Planar spacing requirement

A 1.5 mm space must be maintained between the bottom plane of the module and the corresponding plane of the expansion board to ensure full engagement of the board to board connectors.

While this is commonly provided by the board mounted retention hardware, a mounting screw could travel through a simple spacer to achieve the same result.

Figure 3. Planar spacing diagram



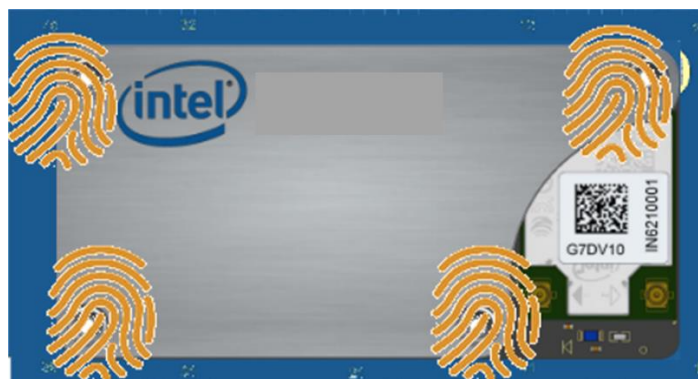
Note: The module retention hardware must create and maintain a ground path connection.

See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Module Retention* for additional retention information.

2.4.2 Module installation steps

1. Place the board on secure, flat, and ESD protected surface with the module side up.
2. Align module connectors with board to board connectors J1 and J2. See Figure 2 for the location of the board-to-board connectors.
3. Using evenly applied pressure, engage the board to board connectors by pressing the module against the connectors where shown until the connectors snap/click in place.

Figure 4. Module press-points to engage board to board connectors.



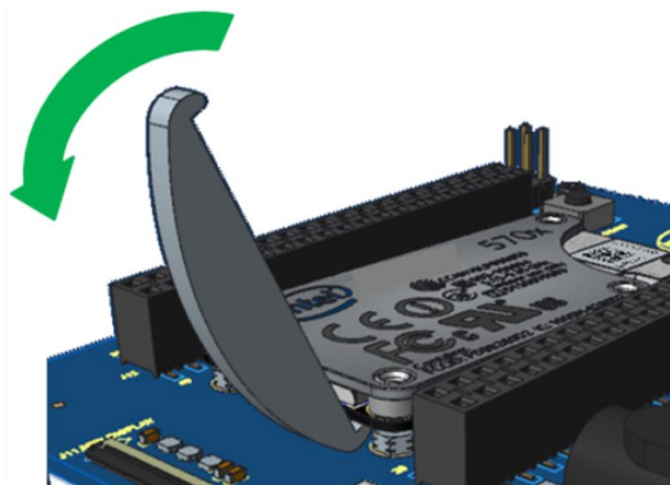
4. Visually inspect the board to board connectors to ensure they are evenly seated and that the module remains coplanar with a 1.5 mm spacing to the expansion board.
5. Install M1.6 hardware of appropriate length or engage with the chosen retention hardware.
6. Avoid over-tightening the mounting hardware to prevent damage. It should be just snug.

2.4.3 Module removal method

1. Power down the platform and disconnect all power sources and accessories.
2. Remove all cooling system components and module retention hardware.
3. Only use non-metal, soft materials tools when applying leverage to separate the module.
4. Place a leverage-arm (tool) along the short edge of the module, near the board to board connectors and away from components on the board and module.
5. Apply smooth and steady force with the tool to separate the module from the board.
6. Stop if the tool slips or comes into contact with any board or module components.
7. The board to board connectors are designed to pop-in and pop-out with tactile response.

Note: See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Removal Tool* to find a 3D model of the demonstrated tool and additional usage information.

Figure 5. Module removal from expansion board



Note: Image shown is of the Intel Joule expansion board and not the 96B compatible carrier board reference design.

2.5 Connect antenna leads

The reference board includes a wireless antenna embedded in the PCB traces that must be attached to the module before installing any heatsink solutions. See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Antenna Connector* for more details.

Use 50 Ohm micro coaxial leads with male MHF-4 connectors similar to Foxconn* KK1201

- Module antenna A1 to 96B compatible carrier board J20
- Module antenna A2 to 96B compatible carrier board J21

Figure 6. Antenna leads (white) installed

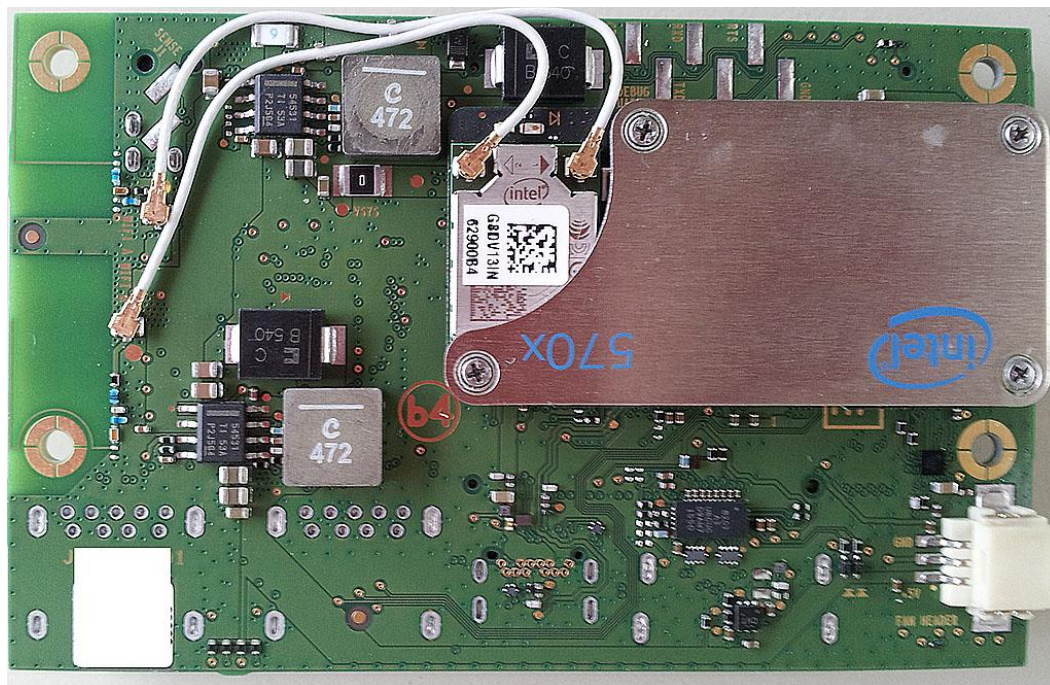
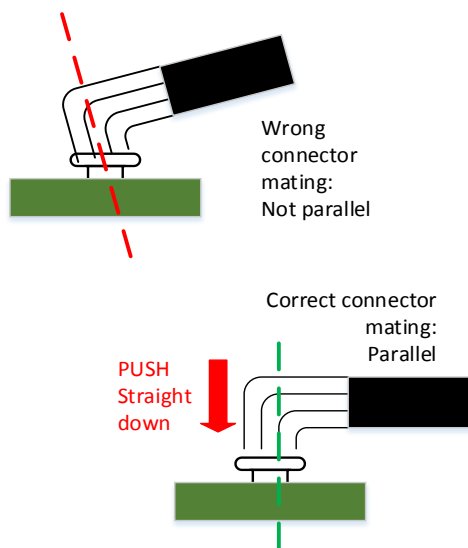


Figure 7. Making the MHF-4 connections.



Note: Ensure connectors are properly aligned before attempting connection; use tools provided by connector manufacturer whenever possible.

2.6 Heatsink options

The module thermal plate can dissipate workloads of less than 2 watts. A fan moving air across the thermal plate is recommended when not using a heatsink.

The Intel Joule module reference heatsink can be used for workloads under 4 watts. The instructions can be found in <https://software.intel.com/en-us/intel-joule-getting-started>. Search for *Thermal Solutions*.

For workloads above 4 watts, an active heatsink is recommended. The instructions for installing a heatsink with an attached fan, a fansink, can be found in <https://software.intel.com/en-us/intel-joule-getting-started>. Search for *Thermal Solutions*.

2.6.1 Custom cooling solutions

The following recommendations are made towards any custom cooling solutions.

Passive cooling methods

- Ensure the surface area of the cooling fins is appropriate for intended workload
- Use thermal transfer material between the thermal plate and heatsink
- Integrate the heatsink retention system with the module retention solution
- Have the heatsink connected to electrical ground
- Ensure solutions do not exert excessive force on the module

Active cooling methods

- Create linear airflow paths to prevent recirculating heated air (thermal runaway)
- Evaluate solutions for blower induced vibration of module
- Ensure incoming air is clean and that exhaust vents enable convection

2.7 Fan connector pinout

The 96B compatible carrier board provides a 3-pin fan header to power the fan contained on the module heatsink. This fan header shall use the pin assignments as described below:

Table 2. Fan connector pin assignments

Pin #	Net Name	Direction	Signal Description
1	+V5P0V	Output	+5-volt supply to fan assembly
2	Reserved.No connect	No connect	No connect - Reserved
3	GND	Ground	Ground

2.8 Install standoffs to protect the board components

Install hex-standoff spacers or similar 'legs' at the board mounting locations that will provide clearance for all bottom side components to prevent damage to the board, module, and heatsink.



Note: The 96B compatible carrier board for the Intel Joule module exceeds the bottom side height specification. Cooling solutions can add additional clearance requirements for standoffs to accommodate. Be sure that standoffs provide adequate clearance.

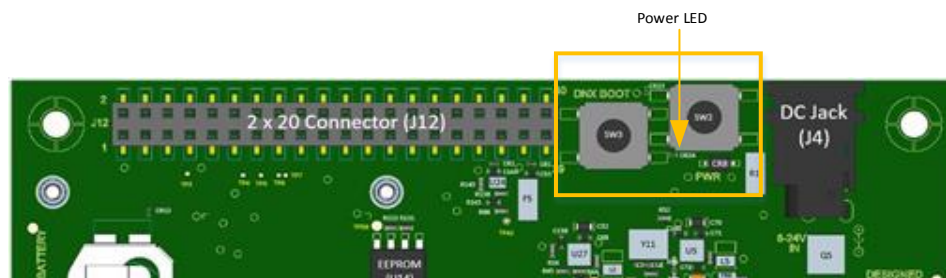
2.9 Board mounted buttons and LEDs

The 96B compatible carrier board contains two buttons:

- Power Button (PWR BTN)
- DNX Boot Button (DNX BOOT)

Refer to Figure 8 for the locations of the buttons.

Figure 8. 96B compatible carrier board buttons



2.9.1 Power button (SW2)

The power button is connected to the PMIC_PWRBTN_N signal of the module. When the button is pressed, the PMIC_PWRBTN_N signal is pulled to ground, driving the PMIC_PWRBTN_N signal to a low state. When the button is released, the PMIC_PWRBTN_N signal is pulled high, to +VDD1 (1.8 volts).

Note: The low time durations of the PMIC_PWRBTN_N signal result in various actions on the module. See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *PMIC_PWRBTN_N* for specific information and usage for the PMIC_PWRBTN_N signal and the resulting actions.

2.9.2 Power LED (CR24)

A main power LED is located near the power switch (SW2) and is enabled when all expansion board power rails are stabilized and a general power good state is achieved.

2.9.3 DNX boot button (SW3)

The DNX boot button is connected to the UART_2_TXD signal of the module. When the button is pressed, the UART_2_TXD signal is pulled high through a 100Ω resistor to +VDD1 (1.8 volts). When the button is released, the UART_2_TXD signal is left floating, but relies on a 20kΩ internal pull-down within the module SoC to insure a low-level signal.

The DNX boot button is used to initiate a BIOS programming cycle when pressed and held during a power-up cycle. At the rising edge of the module's PMIC_PWRGOOD signal (for example during a power-up cycle), the UART_2_TXD is sampled by the module SoC. If the UART_2_TXD is sampled as a high signal, then the SoC initiates a BIOS update from the USB Type-C port. Similarly, if the UART_2_TXD signal is sampled as a low signal (for example DNX boot button released) on the rising edge of PMIC_PWRGOOD, then a BIOS update is not initiated and the boot process continues normally.

2.9.4 GPIO LEDs

There are four general purpose LEDs located as shown in Figure 9 that are connected to GPIO lines 0-3. The LED will light when their respective signal is at a logic high level.

Figure 9. 96B compatible carrier board general purpose LEDs

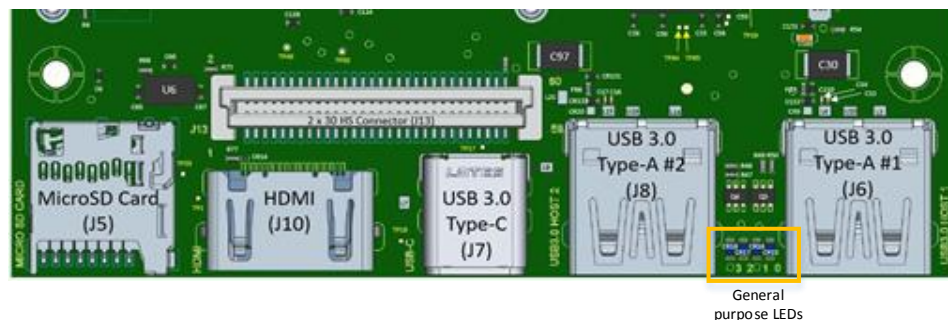


Table 3. On-board LED mapping

Reference Designator	Net Name	Breakout Pin #	Linux* GPIO
GPIO0	ISH_GPIO_0	J12-35	337
GPIO1	ISH_GPIO_1	J12-33	339
GPIO2	ISH_GPIO_2	J12-31	338

Reference Designator	Net Name	Breakout Pin #	Linux* GPIO
GPIO3	ISH_GPIO_3	J12-29	340

Note: These board mounted LEDs can be used by the BIOS for multiple purposes. See the current BIOS release notes for details of their usage during boot and configuration state (input, output, high/low) when control is passed to the operating system.

3 Power on Sequence

While the power on sequence is initiated on the expansion board, the overall flow is defined by module requirements and handshakes between the module firmware and the 96B compatible carrier board.

Section 6 covers the power path in detail and provides system supply and modification guidance while the information provided here is limited to typical power on and reset events.

The 96B compatible carrier board for the Intel Joule compute module contains a single power input source (J4) and a single power button (SW2) that can initiate power up, power down, and reset events based on current platform state and duration the button is depressed.

3.1 Pre-Boot checklist

Ensure that the following conditions are met before attempting to power up the platform:

1. Standoffs of sufficient height are installed to ensure that no board components are resting on the working surface, including the heatsink which would put pressure on the module.
2. If using a heatsink or fan, ensure they are correctly installed, secured, and torqued (maximum 0.1 newton-meters).
3. The module is properly mated to the board-to-board connectors (1.5 mm planar gap).
4. Grounded hardware is installed at the module mounting locations.
5. A properly rated (12VDC @ 3A) power supply is connected to the DC Jack (J4).
6. An HDMI 1.4 display device is connected to J10 by a quality, shielded cable.

3.2 Standard power on process

Supplying DC power at the J4 jack or via the VDC_IN line of the low speed connector are the only power sources supported; the platform will not run on USB-C power.

Refer to Section 6 for additional details of the power subsystem.

When in a mechanical off state, depressing SW2 for greater than 2 seconds and less than 10 seconds will begin the power on sequence. When DC power or VDC_IN (via the low speed connector) is available to the module, the module will boot, execute the installed firmware microcode, signal various voltage and devices, and reset or power on as appropriate.

See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Boot Sequence* for additional information on the boot sequence.

3.3 BIOS update procedure

The BIOS update process for the 96B compatible carrier board is very similar to the Intel Joule module expansion board. It is recommended to review the current online instructions at <https://software.intel.com/en-us/intel-joule-getting-started>. Search for *Flashing the BIOS*. Specific differences in the BIOS update sequence are outlined below.

3.3.1 Workstation setup for BIOS updating

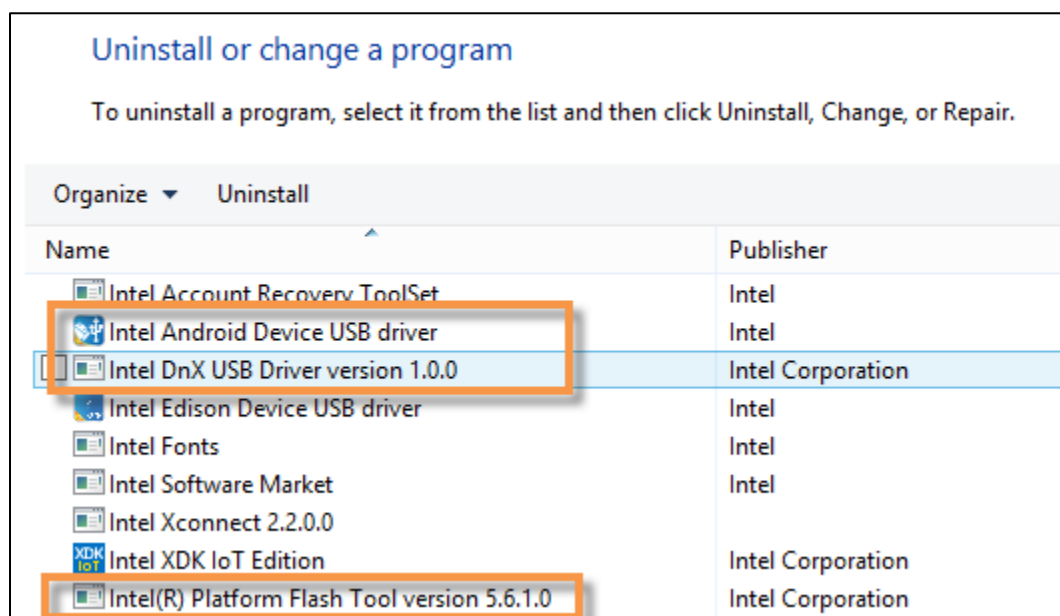
Note: A workstation running Windows* 8, 8.1 or 10 (both 32-bit and 64-bit are supported) is required to use the DnX drivers and BIOS update process.

Remove previous drivers

If you have previously installed any of the following on your host computer:

- Intel® Device USB driver for Android* OS
- Intel® DnX driver
- Intel® Platform Flash Tool

You must first uninstall these components before flashing the BIOS on the development platform. On your Windows host, go to the **Control Panel** and navigate to **Programs and Features**, then uninstall each entry.



Install current DnX driver

Download and extract the contents of the newest BIOS package from the [Intel Joule compute module BIOS downloads page](#).

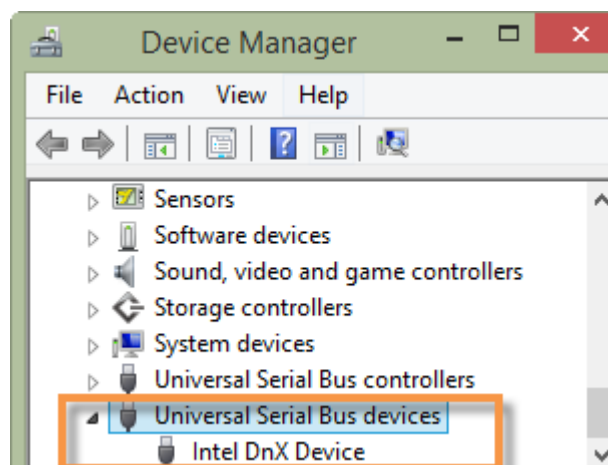
This package contains installers and scripts that are used to flash the BIOS of a 96B compatible carrier board. Within the package downloaded, review the readme and other instructions provided. Find and execute the **FlashUsbDriver-#.#.#.exe** to install the required drivers on the workstation.

Reboot the workstation to ensure the DnX drivers are loaded before attempting to update the 96B compatible carrier board. Failure to do so can prevent the BIOS update from completing successfully.

3.3.2 Push the BIOS.BIN file to the module

Unplug all cables, accessory devices connected directly to the 96B compatible carrier board, and any circuitry connected to the breakout connectors.

1. Connect a USB cable between the workstation and the 96B compatible carrier board Type C connector.
2. Depress and hold the DnX button (SW2).
3. Connect power to the 96B compatible carrier board (while holding the DnX button closed).
4. Release the DnX button once the 96B compatible carrier board has successfully completed power on. The platform should show up in device manager.



- Return to the BIOS firmware folder that was downloaded and extracted.

<input type="checkbox"/> Name	Date modified	Type
<input checked="" type="checkbox"/> DNX	9/29/2016 11:32 A...	File folder
Docs	10/5/2016 3:05 PM	File folder
Public	10/5/2016 3:00 PM	File folder

- Locate the .bin file, named Joule_C0-X64-Release-**193**-Public_DNX.bin and move this file into the DNX folder. The 96B compatible carrier board has been functionally tested with BIOS version 193.
- On your host computer, open a command prompt window.

Downloads > Joule-Firmware-2016-09-23-131_Public > DNX >				
Name	Date modified	Type	Size	
DNX-dldrcli	9/29/2016 11:26 A...	File folder		
clearpmb-bxt-emmc.cmd	9/19/2016 9:06 AM	Windows Comma...	1 KB	
debug.log	9/29/2016 11:32 A...	Text Document	32 KB	
DNX.zip	9/23/2016 7:50 AM	WinRAR ZIP Archive		
Flash.bat	9/29/2016 11:32 A...	Windows Batch File	1 KB	
Flash.log	9/29/2016 11:32 A...	Text Document	1 KB	
get-info-emmc.cmd	9/19/2016 9:06 AM	Windows Comma...	1 KB	
Joule_C0-X64-Release-131-Public_DNX.bin	9/23/2016 2:01 PM	BIN File	8,200 KB	
provision-bxt-emmc.cmd	9/19/2016 9:06 AM	Windows Comma...	1 KB	

- From the command line, navigate to the DNX directory previously extracted.
- In the command prompt window, enter the following command:

```
Flash.bat Joule_C0-X64-Release-###-Public_DNX.bin
```

Note: Example shown is for reference only and must be revised with actual target file name.

10. The display device will show status messages and return to the prompt when complete.

```
=====
Intel(R) Joule Flash.bat version #1.1.3
=====
- Provisioning the eMMC...
- WARNING: Provisioning failed!
  Probably already provisioned.
- Checking for RPMB...
- Downloading the BIOS...
- Clearing NvStorage...
=====
C:\Users\*****\Downloads\DNX>
```

11. Power down the 96B compatible carrier board, disconnect the Type C connector, reboot device into the BIOS setting menu to confirm the update, and adjust BIOS settings.

3.4 BIOS menu settings

Upon first boot after updating the BIOS it is recommended to review the BIOS menus for new options and to ensure previous settings are correct. To enter the BIOS menu, watch the prompts on the display device and follow the on-screen prompts. See <https://software.intel.com/en-us/intel-joule-getting-started> for the latest information on recommended BIOS settings.

3.5 Transition from BIOS to Operating System

This guide only covers hardware boot and firmware operations. 96B compatible carrier board control is transferred to the selected boot device upon successful firmware loading.

See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Choosing Your OS*, for information about installing operating systems.

4 Hardware Overview

The 96B compatible carrier board is designed to be compatible with the 96Boards™ Consumer Edition Specification, though there are exceptions, as described in Section 0.

The various interfaces available from the Intel Joule module are routed to user accessible connectors on the 96B compatible carrier board.

Platform power is received at either the DC input jack or the SYS_DCIN pins located on the low speed connector. This input source is supplied to the Intel Joule compute module, all devices on, and any accessories directly powered by the expansion board.

Caution: DC input jack and SYS_DCIN should never be supplied simultaneously.

Note: The USB-C port cannot be used to power the 96B compatible carrier board.

The Intel Joule module is located on the bottom or back side of the 96B compatible carrier board, the opposite side of the low/high speed connectors. An EEPROM device on the 96B compatible carrier board can hold board specific information such as ACPI, serial number, and manufacturing date.

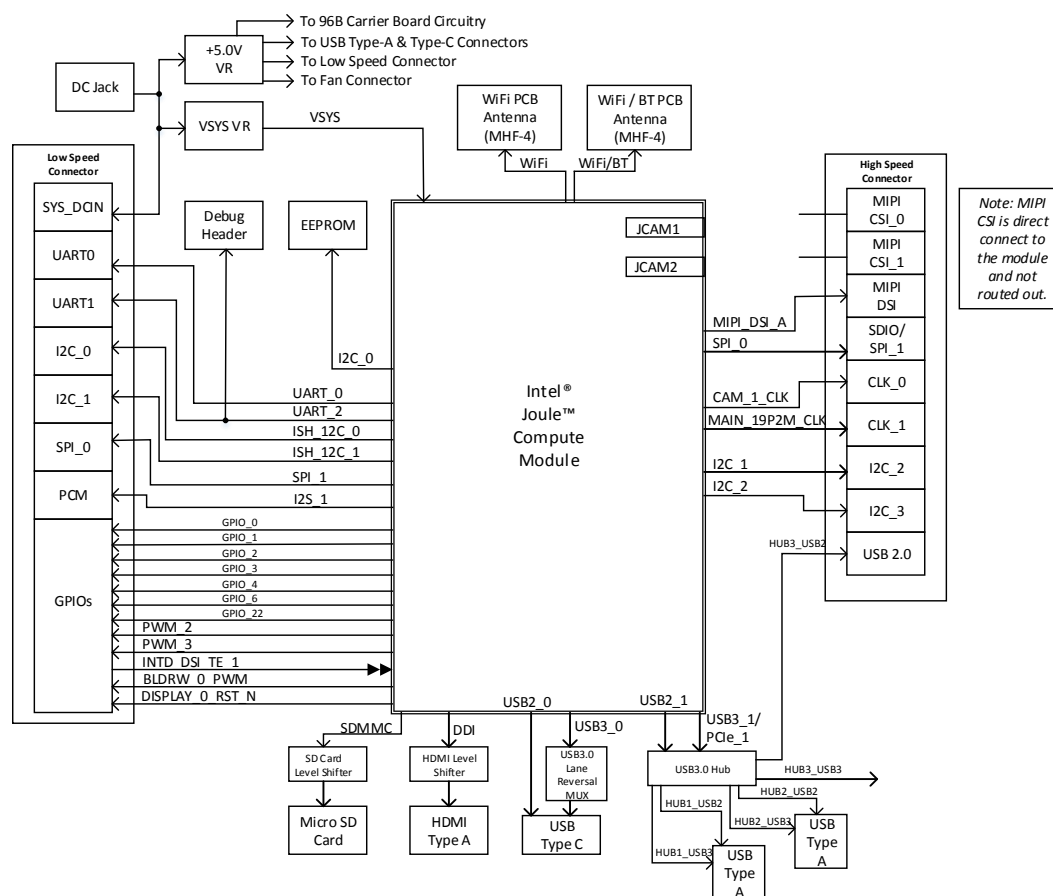
Table 4. Expansion board physical interface highlights

Physical Interfaces	Usage
J13	96BCE style high-speed connector
J12	96BCE style Single low-speed connector
J5	MicroSD Card receptacle
J6 and J8	Two USB Type-A connectors (each support USB 3.x and USB 2.x through backwards compatibility)
J7	USB Type-C connector
J9	UART header (unstuffed) for the debug console interface
J10	HDMI Type-A (full-size) connector
J17	Fan connector (3-pin) to support an active cooling solution
SW2 and SW3	Two buttons: power and DnX boot
CR15.CR18	Four green general purpose LEDs connected to GPIO 0-3

4.1 Platform block diagram

Figure 10 provides the system level block diagram for the 96B compatible carrier board mated with an Intel Joule compute module.

Figure 10. 96B compatible carrier board system block diagram



4.2 Configuration EEPROM and hardware strapping

The 96B compatible carrier board supports an optional 2Mbit I²C-based EEPROM device that can hold post-boot configuration information and product data such as serial number and date code.

If used, the EEPROM device is to be connected to I2C_0 (I2C_0_SCL and I2C_0_SDA) of the module, at addresses 0x50 through 0x53 and 0x58 through 0x5B (assuming 8-bit address, including R/W), with the EEPROM chip select (E2 pin) tied low.

Table 5. 96B compatible carrier board required boot strapping

Intel® Joule™ Module Signal Name	Intel® Joule™ Module Connector.Pin #	Default Intel® Joule™ Module Pin Configuration	Boot Strapping Requirement
UART_0_TXD	J2.93	Internal 20k pull-down	The UART_0_TXD signal is utilized by the 96B compatible carrier board and routed to pin 5 of the low speed expansion connector. In order to insure proper booting of the Intel® Joule™ module, any mezzanine board attached to the 96B compatible carrier board, that utilizes the UART_0_TXD signal, must insure that the attached mezzanine board does not drive the UART_0_TXD signal or include any value of pull-up resistor, until after the rising edge of the PMIC_PWRGOOD signal.
ISH_UART_0_RTS	J3.11	Internal 20k pull-up	The ISH_UART_0_RTS signal is not utilized by the 96B compatible carrier board. However, in order to insure proper booting of the Intel® Joule™ module, the ISH_UART_0_RTS signal must remain unconnected (e.g. high impedance) or pulled up to the Intel® Joule™ module's +1.8-volt (VDD1) supply until after the rising edge of the PMIC_PWRGOOD.
ISH_UART_0_TXD	J3.15	Internal 20k pull-down	The ISH_UART_0_TXD signal is not utilized by the 96B compatible carrier board. However, in order to insure proper booting of the Intel® Joule™ module, the ISH_UART_0_TXD signal must remain unconnected (e.g. high impedance) or pulled down to GND until after the rising edge of the PMIC_PWRGOOD signal.

Intel® Joule™ Module Signal Name	Intel® Joule™ Module Connector.Pin #	Default Intel® Joule™ Module Pin Configuration	Boot Strapping Requirement
SPI_0_FS1	J3.79	Internal 20k pull-up	The SPI_0_FS1 signal is utilized by the 96B compatible carrier board and routed to pin 26 of the low speed expansion connector. In order to insure proper booting of the Intel® Joule™ module, any mezzanine board attached to the 96B compatible carrier board, that utilizes the SPI_0_FS1 signal, must insure that the attached mezzanine board does not drive the SPI_0_FS1 signal, until after the rising edge of the PMIC_PWRGOOD signal. In addition, the attached mezzanine board must not contain any value of pull-up or pull-down resistance on the SPI_0_FS1 signal.

4.2.1 Test pads for programming the EEPROM

The following test pads are provided to directly interface with the EEPROM device.

Table 6. EEPROM access test pads

Reference Designator	Usage
TP56	EEPROM_VCC
TP57	I2C_0_SDA_EE_R
TP68	I2C_0_SCL_EE_R
TP59	Ground

4.3 96BCE specification exceptions

The advanced design of the Intel Joule module prevents some aspects of the 96Boards Consumer Edition Specification from being implemented exactly as specified.

These exceptions are outlined below and noted in the specific subsystem section where applicable.

Table 7. 96Boards compliance exceptions

Item	Specification	Implementation
Wi-Fi* & Bluetooth® Support	The 96Boards™ specification requires that the expansion board provides Wi-Fi* and Bluetooth® capability.	The Intel Joule module, attached to the 96B compatible carrier board, contains Wi-Fi/Bluetooth® capability in the embedded Intel AC8260 module.
Wi-Fi* & Bluetooth® activity LED Support	The 96Boards™ specification requires that yellow and blue LEDs be provided on the expansion board to indicate Wi-Fi* and Bluetooth activity, respectively.	Wireless activity LEDs are not implemented on the 96B compatible carrier board reference design.
Wi-Fi* & Bluetooth® PCB Antennas	The 96Boards™ specification requires that the antennas for the Wi-Fi* and Bluetooth® solutions be located on the expansion board.	The 96B compatible carrier board reference design contains an antenna within the circuit board layers. This antenna is connected to the wireless device on the module by use of male-to-male MHF-4 RF extension cables.
MIPI CSI 2 Support	The 96Boards™ specification optionally supports MIPI CSI on the expansion board high speed connector.	Two MIPI CSI ports are provided on the module through two dedicated flex-circuit connectors and not routed through the 96B compatible carrier board high speed connector interface.
JTAG Interface	JTAG interface support is optional in the 96Boards™ specification.	The 96B compatible carrier board reference design does not provide a JTAG interface.
PCIe Support	The 96Boards™ specification allows for the optional support of a PCIe interface, by either a PCIe mini or M.2 connector on the extended board version.	The 96B compatible carrier board does not support the 96Boards™ extended version and thus will not support a PCIe interface.
Component Height Restrictions	The 96Boards™ specification provides requirements for the maximum component heights on the top and bottom surfaces of the expansion board.	The 96B compatible carrier board complies with the top-side component height specification of less than 7.0mm. However, the assembled 96B compatible carrier board will exceed the bottom side component height specifications of less than 3.4mm. Cooling solutions can further extend the bottom side clearance requirements.

5 High and Low Speed Breakout

The 96B compatible carrier board specification defines a number of standard interface ports in addition to one low speed and one high speed breakout connector. These are each detailed below, including implementation, pinout, and net-name mapping.

5.1 Low speed breakout connector

The low speed expansion connector is a 2x20 pin configuration with a pin-to-pin spacing of 2mm and a height of 4.5mm. The reference designator is J2.

Refer to the 96Boards™ Consumer Edition Specification for representative manufacturers and part numbers.

The low speed expansion connector pinout is shown in Table 8, along with the Intel Joule module connector reference designator and pin number corresponding to the net name.

Refer to See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Compute Module Datasheet* for additional specifications.

Table 8. Low speed expansion connector pinout.sorted by pin name

Low Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
+V1P8V	35	+1.8V	--	+1.8-volt power supply from the 96B compatible carrier board power supply sub-system. The 96B compatible carrier board power supply sub-system must be design to support up to a maximum of 300 mA of current draw from this 1.8-volt supply.
+V5P0V	37	+5V	--	+5.0-volt power supply from the 96B compatible carrier board power supply sub-system. Maximum current draw for a mezzanine board utilizing this supply is 1000mA (1.0A), per the 96Boards™ Consumer Edition Specification
GND	1, 2, 39, 40	GND	--	Ground signal.connect to system ground
GPIO-A	23	CHRG_INT_N	J2.40	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as a wake enabled inverted input, with an internal 20kΩ pull-up. This GPIO also supports an edge triggered interrupt capability on interrupt signal 118, which is routed to the Intel® Joule™ module IOAPIC.

Low Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
GPIO-B	24	ISH_GPIO_5	J2.38	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an output signal, driving a high level, with no internal pull-up or pull-down.
GPIO-C	25	FLASH_TORCH	J3.75	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an output signal, driving a low level with an internal 20kΩ pull-down.
GPIO-D	26	BTN_N	J2.84	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as a non-wake enabled inverted input, with an internal 20kΩ pull-up. This GPIO also supports a level triggered interrupt capability on interrupt line 116.
GPIO-E	27	ISH_GPIO_4	J2.29	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an output signal, driving a high level, with no internal pull-up or pull-down.
GPIO-F	28	BLDRW_O_PWM	J3.56	1.8-volt compliant pulse width modulated (PWM) output signal used to control backlight brightness on a panel attached to the high speed connector MIPI DSI interface
GPIO-G	29	INTD_DSI_TE1	J3.82	1.8-volt compliant Tear Enable (TE) input signal from a panel attached to the high speed connector MIPI DSI interface. Signal is used to indicate the vertical sync interval for the MIPI DSI panel.
GPIO-H	30	DISPLAY_O_RST_N	J3.68	1.8-volt compliant general purpose input/output signal intended for use as a reset signal to reset a panel attached to the high speed connector MIPI DSI interface. The default GPIO configuration is as an output signal, driving a low level, with an internal 20kΩ pull-down.
GPIO-I	31	ISH_GPIO_6	J2.31	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an output signal, driving a high level, with no internal pull-up or pull-down.
GPIO-J	32	PWM_2	J2.22	1.8-volt compliant programmable pulse width modulated output signal from the 96B compatible carrier board.
GPIO-K	33	PWM_3	J2.24	1.8-volt compliant programmable pulse width modulated output signal from the 96B compatible carrier board.

Low Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
GPIO-L	34	GPIO_22	J2.94	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as a non-wake enabled inverted input, with an internal 20kΩ pull-up. This GPIO also supports an edge triggered interrupt capability on interrupt line 51.
I2C0_SCL	15	ISH_I2C_0_SCL	J2.16	1.8-volt compliant, open drain I ² C clock output from the 96B compatible carrier board, for ISH I ² C port 0.
I2C0_SDA	17	ISH_I2C_0_SDA	J2.18	1.8-volt compliant, open drain I ² C data input/output from the 96B compatible carrier board, for ISH I ² C port 0.
I2C1_SCL	19	ISH_I2C_1_SCL	J2.21	1.8-volt compliant, open drain I ² C clock output from the 96B compatible carrier board, for ISH I ² C port 1.
I2C1_SDA	21	ISH_I2C_1_SDA	J2.23	1.8-volt compliant, open drain I ² C data input/output from the 96B compatible carrier board, for ISH I ² C port 1.
PCM_CLK	18	I2S_1_CLK	J2.39	1.8-volt compliant, I ² S clock output from the 96B compatible carrier board.
PCM_DI	22	I2S_1_RXD	J2.47	1.8-volt compliant, I ² S data input from the 96B compatible carrier board.
PCM_DO	20	I2S_1_TXD	J2.49	1.8-volt compliant, I ² S data output from the 96B compatible carrier board.
PCM_FS	16	I2S_1_FS	J2.45	1.8-volt compliant, I ² S frame select output from the 96B compatible carrier board.
PWR_BTN_N	4	PMIC_PWRBTN_N	J2.9	Active low, open drain, power button input signal to the Intel® Joule™ module. Signal to be shared with the power button located on the 96B compatible carrier board. The PMIC_PWRBTN_N signal is pulled-up on the Intel® Joule™ module to the Intel® Joule™ module VSYS power supply. A mezzanine board attached to the 96B compatible carrier board must not include any pull-up or pull-down resistors or circuitry. The mezzanine board should contain circuitry (e.g. momentary pushbutton or open drain circuitry) to "short" the PMIC_PWRBTN_N signal to ground. Refer to Section 2.9.1 for additional details on the power button usage.

Low Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
RST_BTN_N	6	HW_RST_N	N/A	The HW_RST_N signal is connected, through a 0-ohm resistor to the PMIC_PWRBTN_N signal (i.e. pin 4 of this same connector). This allows the user to either power down (e.g. mechanical off, which is equivalent to reset), or place in standby (e.g. S0ix), or power-up the 96B compatible carrier board through either pin-4 (i.e. PMIC_PWRBTN_N) or pin-6 (HW_RST_N) of the low speed expansion connector. Refer to Section 2.9.1 for additional details on the usage of the HW_RST_N (a.k.a. PMIC_PWRBTN_N) signal
SPIO_CS	12	SPI_1_FS0	J2.55	1.8-volt compliant Function Select (FS) zero output signal for Serial Peripheral Interface (SPI) port 1.
SPIO_DIN	10	SPI_1_MISO	J2.63	1.8-volt compliant Master In Slave Out (MISO), the data input signal for Serial Peripheral Interface (SPI) port 1.
SPIO_DOUT	14	SPI_1_MOSI	J2.51	1.8-volt compliant Master Out Slave In (MOSI), the data output signal for Serial Peripheral Interface (SPI) port 1.
SPIO_SCLK	8	SPI_1_CLK	J2.53	1.8-volt compliant clock output signal for Serial Peripheral Interface (SPI) port 1.
SYS_DCIN	36	SYS_DCIN	--	+8.0 to +24.0-volt power supply sourced from either the 96B compatible carrier board DC Power Jack or a mezzanine board attached to the 96B compatible carrier board. The 996B compatible carrier board design must support a minimum of 7W of power delivered to/from an attached mezzanine board, shared with pin 38 of the low speed expansion connector. Note: The end-user MUST insure that the 96B compatible carrier board is powered only from either the DC Power Jack or from a mezzanine board attached to the 96B compatible carrier board...never both. Failure to follow this requirement may result in damage to the supply connected to the DC Power Jack, the 96B compatible carrier board, the mezzanine board, or any combination of the three. A resettable fuse is included between the DC Power Jack and the SYS_DCIN pins on this low speed expansion connector, to aid in minimizing the risk for damage if the requirement for a single supply source is not followed.
SYS_DCIN	38	SYS_DCIN	--	Refer to description for pin 36 connector.
UART0_CTS	3	UART_0_CTS	J3.47	Clear To Send signal (CTS) for UART0, a high speed UART at 1.8-volt signal levels.

Low Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
UART0_RTS	9	UART_0_RTS	J3.55	Ready To Send signal (RTS) for UART0, a high speed UART at 1.8-volt signal levels.
UART0_RxD	7	UART_0_RXD	J3.51	Receive signal for UART0, a high speed UART at 1.8-volt signal levels.
UART0_TxD	5	UART_0_TXD	J2.93	Transmit signal for UART0, a high speed UART at 1.8-volt signal levels.
UART1_RxD	13	UART_2_RXD	J2.26	Receive signal for UART2, a standard speed UART at 1.8-volt signal levels. UART2 is also the console port for Intel OS build for Linux. Refer to Section 0 for additional details on using UART2 for console output.
UART1_TxD	11	UART_2_TXD	J2.28	Transmit signal for UART2, a standard speed UART at 1.8-volt signal levels. UART2 is also the console port for Intel's standard Linux OS build. Refer to Section 0 for additional details on using UART2 for console output. UART_2_TXD is one of the boot strapping pins for the Intel® Joule™ module. Refer to Table 5 for the boot strapping requirements for this signal.

5.1.1 Low speed connector visual mapping

Table 9. Low speed expansion connector pinout.visual mapping

Module Net Name	Pin Name	Pin #		Pin #	Pin Name	Module Net Name
GND	GND	1		2	GND	GND
UART_0_CTS	UART0_CTS	3		4	PWR_BTN_N	PMIC_PWRBTN_N
UART_0_TXD	UART0_TXD	5		6	RST_BTN_N	PMIC_PWRBTN_N
UART_0_RXD	UART0_RXD	7		8	SPI_SCLK	SPI_1_CLK
UART_0_RXD	UART0_RXD	7		8	SPI_SCLK	SPI_1_CLK
UART_0_RTS	UART0_RTS	9		10	SPI0_DIN	SPI_1_MISO
UART_2_TXD	UART1_TXD	11		12	SPI0_CS	SPI_1_FS0
UART_2_RXD	UART1_RXD	13		14	SPI0_DOUT	SPI_1_MOSI
ISH_I2C_0_SCL	I2C0_SCL	15		16	PCM_FS	I2S_1_FS
ISH_I2C_0_SDA	I2C0_SDA	17		18	PCM_CLK	I2S_1_CLK

Module Net Name	Pin Name	Pin #		Pin #	Pin Name	Module Net Name
ISH_I2C_1_SCL	I2C1_SCL	19		20	PCM_DO	I2S_1_TXD
ISH_I2C_1_SDA	I2C1_SDA	21		22	PCM_DI	I2S_1_RXD
CHARG_INT_N	GPIO-A	23		24	GPIO-B	ISH_GPIO_5
FLASH_TORCH	GPIO-C	25		26	GPIO-D	BTN_N
ISH_GPIO_4	GPIO-E	27		28	GPIO-F	BLDRW_0_PWM
INTD_DSI_TE1	GPIO-G	29		30	GPIO-H	DISPLAY_0_RST_N
ISH_GPIO_6	GPIO-I	31		32	GPIO-J	PWM_2
PWM_3	GPIO-K	33		34	GPIO-L	GPIO_22
+1.8V	+1V8	35		36	SYS_DCIN	SYS_DCIN
+5V	+5V	37		38	SYS_DCIN	SYS_DCIN
GND	GND	39		40	GND	GND

5.2 High speed breakout connector

The high speed breakout connector is a 60 pin, 0.8 mm height, board-to-board receptacle connector. Refer to the 96Boards™ Consumer Edition Specification for representative manufacturers and part numbers.

The High Speed Breakout Connector pinout is shown in below, along with the Intel Joule module connector reference designator and pin number corresponding to the net name.

Refer to See <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Compute Module Datasheet* for additional specifications.

Table 10. High speed breakout connector pinout.sorted by pin name

High Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
CLK0 / CSIO_MCLK	15	CLK_19P2M	J2.71	1.8-volt compliant 19.2MHz clock output from the 96B compatible carrier board.
CLK1 / CSI1_MCLK	17	CODEC_MCLK	J2.43	1.8-volt compliant clock for I ² S interface master mode operation.
CSIO_C-	4	ISH_UART_0_RTS	J3.11	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an input signal with an internal 20kΩ pull-down.

High Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
CSIO_C+	2	ISH_UART_0_CTS	J3.9	1.8-volt compliant general purpose input/output signal. The default GPIO configuration is as an input signal with an internal 20kΩ pull-down.
DSI_CLK-	23	MDSI_A_CLK_DN	J3.27	Negative-side differential MIPI-DSI compliant clock output signal from 96B compatible carrier board.
DSI_CLK+	21	MDSI_A_CLK_DP	J3.25	Positive-side differential MIPI-DSI compliant clock output signal from 96B compatible carrier board.
DSI_D0-	29	MDSI_A_DATA_0_DN	J3.19	Negative-side differential MIPI-DSI compliant data lane 0 input/output signal from 96B compatible carrier board.
DSI_D0+	27	MDSI_A_DATA_0_DP	J3.21	Positive-side differential MIPI-DSI compliant data lane 0 input/output signal from 96B compatible carrier board.
DSI_D1-	35	MDSI_A_DATA_1_DN	J3.31	Negative-side differential MIPI-DSI compliant data lane 1 output signal from 96B compatible carrier board.
DSI_D1+	33	MDSI_A_DATA_1_DP	J3.33	Positive-side differential MIPI-DSI compliant data lane 1 output signal from 96B compatible carrier board.
DSI_D2-	41	MDSI_A_DATA_2_DN	J3.37	Negative-side differential MIPI-DSI compliant data lane 2 output signal from 96B compatible carrier board.
DSI_D2+	39	MDSI_A_DATA_2_DP	J3.39	Positive-side differential MIPI-DSI compliant data lane 2 output signal from 96B compatible carrier board.
DSI_D3-	47	MDSI_A_DATA_3_DN	J3.76	Negative-side differential MIPI-DSI compliant data lane 3 output signal from 96B compatible carrier board.
DSI_D3+	45	MDSI_A_DATA_3_DP	J3.78	Positive-side differential MIPI-DSI compliant data lane 3 output signal from 96B compatible carrier board.
GND	6, 12, 13, 18, 19, 24, 25, 30, 31, 37, 40, 43, 46, 49, 52, 55, 58	GND	--	Ground signal.connect to system ground
I2C2_SCL	32	I2C_1_SCL	J3.43	1.8-volt compliant, open drain I ² C clock output from the 96B compatible carrier board, for Core I ² C port 1

High Speed Connector		Intel® Joule™ Module Connector		Description
Pin Name	Pin #	Net Name	Pin #	
I2C2_SDA	34	I2C_1_SDA	J3.45	1.8-volt compliant, open drain I ² C data input/output from the 96B compatible carrier board, for Core I ² C port 1
I2C3_SCL	36	I2C_2_SCL	J3.28	1.8-volt compliant, open drain I ² C clock output from the 96B compatible carrier board, for Core I ² C port 2
I2C3_SDA	38	I2C_2_SDA	J3.26	1.8-volt compliant, open drain I ² C data input/output from the 96B compatible carrier board, for Core I ² C port 2
NC	3, 5, 8 10, 14, 16, 20, 22, 26, 28, 42, 44, 48, 50, 54, 56, 57, 59	No Connect	--	No connect.pin to remain unconnected / floating
RESERVED	60	Reserved	--	Reserved.pin to remain unconnected / floating
SD_CMD / SPI1_DIN	11	SPI_0_MISO	J3.49	1.8-volt compliant Master In Slave Out (MISO), the data input signal for Serial Peripheral Interface (SPI) port 0
SD_DAT0 / SPI1_DOUT	1	SPI_0_MOSI	J3.57	1.8-volt compliant Master Out Slave In (MOSI), the data output signal for Serial Peripheral Interface (SPI) port 0
SD_DAT3 / SPI1_CS	7	SPI_0_FS0	J3.77	1.8-volt compliant Function Select (FS) zero output signal for Serial Peripheral Interface (SPI) port 0
SD_SCLK / SPI1_SCLK	9	SPI_0_CLK	J3.59	1.8-volt compliant clock output signal for Serial Peripheral Interface (SPI) port 0
USB_D-	53	HUB3_USB2_DN	--	Negative-side differential USB2.0 compliant signal from a USB hub device on the 96B compatible carrier board.
USB_D+	51	HUB3_USB2_DP	--	Positive-side differential USB2.0 compliant signal from a USB hub device on the 96B compatible carrier board.

5.2.1 High speed physical mapping diagram

Table 11. High speed breakout connector pinout.visual mapping

Module Net Name	Pin Name	Pin #		Pin #	Pin Name	Module Net Name
SPI_0_MOSI	SD_DAT0/SPI1_DOUT	1		2	CSIO_C+	ISH_UART_0_CTS
NC	SD_DAT1	3		4	CSIO_C-	ISH_UART_0_RTS
NC	SD_DAT2	5		6	GND	GND
SPI_0_FS0	SD_DAT3/SPI1_CS	7		8	CSIO_D0+	NC
SPI_0_CLK	SD_SCLK/SPI1_SCLK	9		10	CSIO_D0-	NC
SPI_0_MISO	SD_CMD/SPI1_DIN	11		12	GND	GND
GND	GND	13		14	CSI_D1+	NC
CLK_19P2M	CLK0/CSIO_MCLK	15		16	CSI_D1-	NC
CODEC_MCLK	CLK1/CSI1_MCLK	17		18	GND	GND
GND	GND	19		20	CSIO_D2+	NC
MDSI_A_CLK_DP	DSI_CLK+	21		22	CSI_D2-	NC
MDSI_A_CLK_DN	DSI_CLK-	23		24	GND	GND
GND	GND	25		26	CSIO_D3+	NC
MDSI_A_DATA_0_DP	DSI_D0+	27		28	CSI_D3-	NC
MDSI_A_DATA_0_DN	DSI_D0-	29		30	GND	GND
GND	GND	31		32	I2C2_SCL	I2C_1_SCL
MDSI_A_DATA_1_DP	DSI_D1+	33		34	I2C2_SDA	I2C_1_SDA
MDSI_A_DATA_1_DN	DSI_D1-	35		36	I2C3_SCL	I2C_2_SCL
GND	GND	37		38	I2C3_SDA	I2C_2_SDA
MDSI_A_DATA_2_DP	DSI_D2+	39		40	GND	GND
MDSI_A_DATA_2_DN	DSI_D2-	41		42	CSI1_D0+	NC
GND	GND	43		44	CSI1_D0-	NC
MDSI_A_DATA_3_DP	DSI_D3+	45		46	GND	GND

Module Net Name	Pin Name	Pin #		Pin #	Pin Name	Module Net Name
MDSI_A_DATA_3_DN	DSI_D3-	47		48	CSI1_D1+	NC
GND	GND	49		50	CSI1_D1-	NC
HUB3_USB2_DP	USB_D+	51		52	GND	GND
HUB3_USB2_DN	USB_D-	53		54	CSI1_C+	NC
GND	GND	55		56	CSI1_C-	NC
NC	HSIC_STR	57		58	GND	GND
NC	HSIC_DATA	59		60	RESERVED	RESERVED

6 Power Delivery Subsystem

6.1 Power delivery overview

The expansion board can operate off of one of two power sources; either the DC input jack (J4) or from the low speed connector (J12) on pins 36 and 38 as +SYS_DCIN.

The DC power jack is specified to support up to 5-amps of current, with the VR architecture capable of supporting input voltages between +8-volts and +18-volts.

Caution: It is important to note that the architecture is designed for a total input power at the DC Power Jack of 60W, including any power drawn by an attached mezzanine board or accessories.

This implies that a minimum input voltage at the DC power jack is required to deliver 60W, as the total power draw can remain at 5-amps. If the input voltage at the DC power jack is less than +12-volts, then the total power draw through the DC power jack must be decreased such that the maximum input current does not exceed 5-amps (e.g. max power draw is 40-watts at +8-volts).

Referring to the power architecture block diagram, the input supply splits to deliver the input voltage to both the voltage regulators on the expansion board and to the SYS_DCIN pins of the low speed expansion connector.

A polarity reversal protection FET is included in the path to the voltage regulators, to prevent damage to the expansion board, as well as a 6-amp resettable fuse to protect against short circuits or over current conditions.

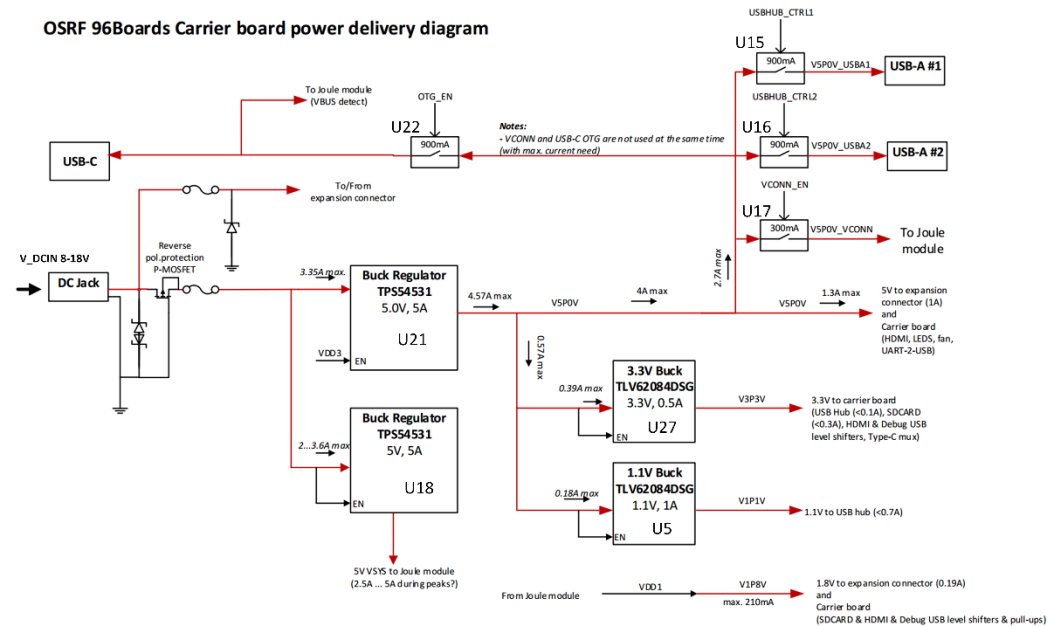
A 6-amp resettable fuse is also included in the power path to the low speed expansion connector. Polarity reversal protection is not provided to the low speed expansion connector.

Due to the interconnect between the low speed expansion connector SYS_DCIN pins and the DC power jack, it is possible to provide power to the 96B compatible carrier board from an attached mezzanine board, but the expansion board draw from the mezzanine board must be limited to less than 7-watts, per the 96Boards™ Consumer Edition Specification.

Note: The expansion board must NOT be powered from both the DC power jack and an attached mezzanine board at the same time. Only one power source is allowed, per the 96Boards™ Consumer Edition Specification and failure to follow this requirement may result in damage to the module, the expansion board, any attached mezzanine board, or the power supplies connected at any input point.

The 96B compatible carrier board does not support being powered from the USB Type-C connector.

Figure 11. 96B compatible carrier board power delivery block diagram



6.2 DC power jack

The DC power jack accepts a 1.75 mm, center-positive / outer barrel negative configuration of a 4.75 mm plug to a depth of 8.00 mm. Through-hole attachment adds strength against lifting.

Caution: Do not connect the DC power jack and provide power at the SYS_DCIN pins at the same time.

The DC power jack located on the 96B compatible carrier board accepts, at a minimum, the nominal input voltage range of between +8.0 volts and +18.0 volts, as specified in the 96Boards Consumer Edition Specification.

The table below shows the required voltage ranges, along with the associated supply current ratings.

Table 12. DC power jack electrical specifications

Source	Item	Min	Typ	Max	Units	Conditions
DC Power Jack	V _{DCIN}	8	12	18	V	At V _{DCIN} pin of DC power jack
	I _{DCIN}			5.0	A	

6.3 Battery power and RTC backup

Note: No battery enabling, charging, or support services are currently provided by the expansion board.

All battery solutions must be completely external to the expansion board except for standard communication and I/O interfaces. The U18 device serves as the +V_{SY}S voltage regulator.

6.3.1 RTC Back up Battery

The 96B compatible carrier board provides a coin cell battery receptacle (that can hold CR1225, CR1216, or CR1220 size batteries) to provide battery backup power to maintain the modules power management IC, the time management unit's data, configuration, status registers, and timekeeping logic in the case of power loss.

The positive terminal of the battery shall be connected to the +VRTC pin on the module expansion connectors. The coin cell battery receptacle will not support backup battery charging.

Note: If the 96B compatible carrier board is removed from power (for instance, if no power is provided from the DC power jack or the USB Type-C connector) for an extended period of time, the back-up battery may drain to below the minimum operating voltage, with the result that the data stored in the module's time management unit may become invalid.

6.4 Power on and shut-down signaling

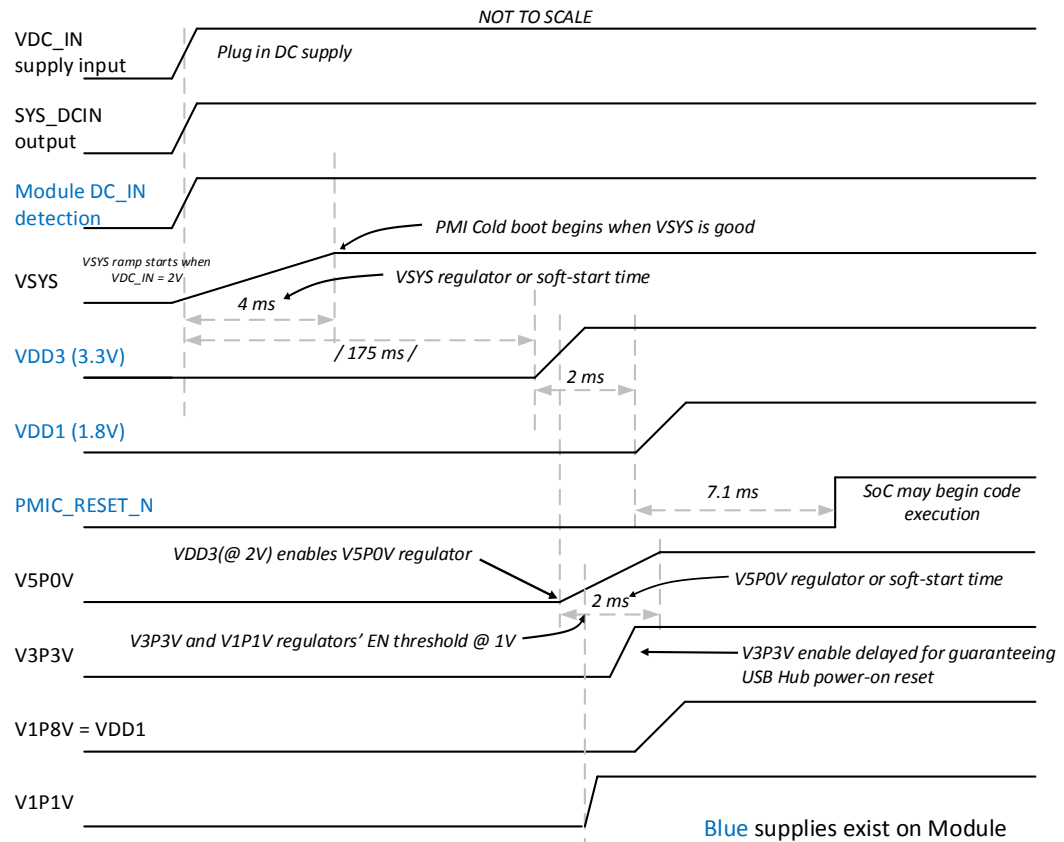
A power source must be available at either the DC input jack or the USB Type-C connector before power on can be initiated.

Closing (pressing) SW2 pulls PMIC_PWRBTN_N low, enabling the Intel® Joule™ module to begin the power on logic sequence. PMIC_PWRBTN_N is also connected to the module on J2 pin 9, and J12 on pins 4 and 6. The J12 connection can be used to reset the 96B compatible carrier board which is required for 96Board compliance.

Refer to <https://software.intel.com/en-us/intel-joule-getting-started> and search for *power button* for power button behaviors.

6.5 Power supply sequencing

Figure 12: Power on timing sequence (cold boot)



All rails are off within 2 milliseconds of a power off event. Power off supply sequencing is not specified or guaranteed.

6.6 Voltage regulators and load switches

Refer to Figure 11 for a block diagram of the power delivery system including the buck regulators.

6.6.1 +VSYS Buck regulator (U18)

The +VSYS buck converter (Texas Instruments* Part number TPS54531) converts the +VDC_IN input supply to a +5V / 5A power rail, labelled +VSYS. Refer to Table 14 for the maximum allowable current draw.

The +VSYS power rail supplies power only to the SoC Module via connectors J2 and J3.

6.6.2 +5.0V Buck regulator (U21)

The +5.0V buck converter (a Texas Instruments* Part number TPS54531), enabled by +VDD3, converts the +VDC_IN input supply to a +5V power rail, labelled +V5P0V. Refer to Table 14 for the maximum allowable current draw.

The +V5P0V power rail supplies power to:

- HDMI connector (J10) and power distribution switch (U26)
- USB load switches (U15-U17,U22), USB Hub (U2), and USB connectors (J6,J8)
- +V5P0V_BREAKOUT on connector J12 pin 37 via PTC 1A Fuse (F5)
- Fan header J17
- 3.3V and 1.1V buck regulators
- GPIO LEDs

Note: The +5.0V buck regulator does not start ramping until the +VDD3 supply from the module connector (J2 pin 30) reaches a minimum of 1.25 V and +VDC_IN reaches at least 2.2 V.

6.6.3 +3.3V Buck regulator (U27)

The +3.3V buck-regulator (a Texas Instruments* TLV62084DSGR switching regulator) converts the +V5P0V rail to a +3.3V power rail labelled +V3P3V. Refer to Table 14 for the maximum allowable current draw.

The +V3P3V power rail supplies power to:

- +V3P3V_USB_Hub through a noise suppression / EMI suppression filter (FB3)
- +V3P3V_MICROSD through a noise suppression / EMI suppression filter (FB2)
- USB Type-C Mux
- Micro-SD card interface level shifter and connector
- HDMI and UART debug interface level shifters
- Breakout connector J13 and the fan header

Note: The +3.3 volt buck regulator does not start ramping until the +V5P0V supply reaches at least 1.0 V.

6.6.4 +1.8 Voltage supply

The +1.8 power rail is created by driving the +VDD1 supply (out of connector J2 at pin 36 and) through a noise suppression / EMI suppression filter (FB11). Refer to Table 14 for the maximum allowable current draw.

The +V1P8V power rail supplies power to:

- +V1P8V_MICROSD through a noise suppression / EMI suppression filter (FB1)
- Micro-SD card interface level shifter, ESD and EMI filtering
- Low-Speed (J12) & High-Speed (J13) connectors
- HDMI and UART debug interface level shifters and re-drivers
- I2C EEPROM
- Boot from DNX (SW3)
- +V1P8V_BREAKOUT on connector J12 pin 37 via load switch U24
- Breakout connector J13 pin 60

6.6.5 +1.1 Buck regulator (U5)

The +1.1V buck regulator (a Texas Instruments* TLV62084DSGR switching regulator) converts the +V5P0V rail to a +1.1V power rail labelled +V1P1V.

The +V1P1V power rail supplies power to:

- +V1P1V_USB_Hub through a noise suppression / EMI suppression filter (FB6)

Note: The +1.1V buck regulator does not start ramping until the +V5P0V supply from the module connector reaches a minimum of 1.0 V.

6.6.6 USB current limiters (U15, U16, and U22)

There are three USB current limiters (Texas Instruments* TPS2553DRVT) that control the delivery of the +V5P0V supply to the USB Type-C Configuration Channel (CC) lines for the module, and the USB Type-C and USB Type-A connectors. The current limiters are able to provide 900 mA per USB specification.

6.6.7 Module sourced power supplies (+VDD1 and +VDD3)

The module provides two power rails, each limited to 300 mA. The +VDD1 rail provides power to the +1.8V power rail. The +VDD3 rail enables the +5.0V buck regulators.

Caution: Ensure that the low speed connector loads do not cause power supplies to be overloaded.

6.6.8 Module sourced power supplies

Table 13. Power supplies electrical specifications

Source	Item	Min	Typ	Max	Units	Max mA
VDD1	+VDD1	1.71	1.8	1.89	V	300
VDD3	+VDD3	3.15	3.3	3.45	V	300

Note: Do not exceed specified current limits; ensure that all device loads are accounted for.

6.7 Maximum current draw

Electrical specifications for each power source are as follows:

Table 14. Maximum current draw

Source	Parameter	Min	Typical	Maximum	Units
+V3P3V	Voltage	3.135	3.3	3.465	V
	Current			1.4	A
+V5P0V	Voltage	4.75	5.0	5.25	V
	Current			1.0	A

The total combined power for +V3P3V and +V5P0V should not exceed 4.5 W given 12 V to VDCIN. This is assuming that the USB ports are not sourcing 900 mA to devices for OTG mode. If your use case requires full OTG current, then the OTG power should be subtracted from 4.5 W to find your new max power allowed to the IO breakout connectors.

7 Clocks

The 96B compatible carrier board provides two clock signals on the breakout connectors - a 19.2 MHz clock and a 32.768 kHz real time clock (RTC). The following two sections provide the AC and DC specifications for both of these clock signals.

7.1 19.2 MHz system clock (XTAL)

The 19.2 MHz system clock is sourced from the Intel Joule module and is routed to the high speed connector J13 pin 15. The following tables provide the DC and AC specifications for the 19.2 MHz system clock signal.

Table 15. The 19.2 MHz clock DC specifications

Parameter	Min	Typ	Max	Units	Conditions
V _{OH}	1.44			V	At R _{PULLUP} (min)
V _{OL}			0.45	V	At R _{PULLUP} (min)
I _{SOURCE}			1.5	mA	

Table 16. The 19.2 MHz clock AC specifications

Parameter	Min	Typ	Max	Units	Conditions
T _{RISE}	13		17	ns	20% to 80%
T _{FALL}	13		17	ns	20% to 80%
Frequency		19.2		MHz	
Duty Cycle	45	50	55	%	

8 HDMI Type-A Connector

The HDMI Type-A connector includes through-hole mechanical attachment to the PCB for robust grounding. The HDMI interface on the expansion board includes capacitive coupling for HDMI data and clock signals plus a level shifter between the module and the HDMI Type-A connector.

The HDMI Type-A connector can supply up to 55 mA of current from the +V5P0 supply rail.

Table 17. HDMI, Type-A Connector Pinout

HDMI Type-A Connector Pin #	Intel® Joule™ Module		Description Viewed from expansion board
	Net Name	Connector.Pin #	
1	HDMI_TX_2_DP	J2.52	Positive-side differential signal for HDMI data lane 2
2	GND	--	Ground signal.connect to system ground
3	HDMI_TX_2_DN	J2.50	Negative-side differential signal for HDMI data lane 2
4	HDMI_TX_1_DP	J2.56	Positive-side differential signal for HDMI data lane 1
5	GND	--	Ground signal.connect to system ground
6	HDMI_TX_1_DN	J2.58	Negative-side differential signal for HDMI data lane 1
7	HDMI_TX_0_DP	J2.64	Positive-side differential signal for HDMI data lane 0
8	GND	--	Ground signal.connect to system ground
9	HDMI_TX_0_DN	J2.62	Negative-side differential signal for HDMI data lane 0
10	HDMI_CLK_DP	J2.44	Positive-side differential signal for HDMI clock
11	GND	--	Ground signal.connect to system ground
12	HDMI_CLK_DN	J2.46	Negative-side differential signal for HDMI clock
13	No Connect		No connect.pin to remain unconnected / floating
14	Reserved	--	Reserved.pin to remain unconnected / floating
15	DDI1_CTRL_CLK	J2.68	Display Data Channel (DDC) open drain clock signal output
16	DDI1_CTRL_DAT	J2.70	Display Data Channel (DDC) open drain data signal input
17	GND	--	Ground signal.connect to system ground
18	+5V	--	5.0-volt power supply from the expansion board Maximum current draw on this supply is not to exceed 55mA, per the HDMI Specification

HDMI Type-A Connector Pin #	Intel® Joule™ Module		Description Viewed from expansion board
	Net Name	Connector.Pin #	
19	HPD_SRC	J2.65	Hot plug detect signal input to the expansion board
20,21,22,23	Shell / Shield	Ground	Signal ground

9 GPIOs

The 96B compatible carrier board provides 12 dedicated GPIO lines at the J12 low speed connector as shown in Table 18. There are four additional GPIO signals, not driven from J12, that drive the GPIO LEDs (ISH_GPIO_0 through ISH_GPIO_3) when the line is HIGH from either the low speed connector or the module. Refer to Table 3 for the mapping of GPIO to LEDs.

The default pin usage refers to the vantage point of the 96B compatible carrier board.

Table 18. GPIO mapping table

Connector.Pin #	Signal Name	Default Breakout Usage	Signal Description
J12.23	CHRG_INT_N	GPIO	GPIO-A
J12.24	ISH_GPIO_5	GPIO	GPIO-B
J12.25	FLASH_TORCH	GPIO	GPIO-C
J12.26	BTN_N	GPIO	GPIO-D
J12.27	ISH_GPIO_4	GPIO	GPIO-E
J12.28	BLDRW_0_PWM	GPIO	GPIO-F
J12.29	INTD_DSI_TE_1	GPIO	GPIO-G
J12.30	DISPLAY_0_RST_N	GPIO	GPIO-H
J12.31	ISH_GPIO_6	GPIO	GPIO-I
J12.32	PWM_2	GPIO	GPIO-J
J12.33	PWM_3	GPIO	GPIO-K
J12.34	GPIO_22	GPIO	GPIO-L

10 I2S Interface

The 96B compatible carrier board provides one I2S port at the low speed connector to enable the connection of audio-based devices.

Table 19. I2S Mapping to low speed connector

Connector.Pin #	Signal Name	Default Breakout Direction	Signal Description
J12.22	I2S_1_RXD	Input	Audio data input to the expansion board, from an I2S compliant audio input device on the breakout board
J12.20	I2S_1_TXD	Output	Audio data output to an I2S compliant audio output device on the breakout board
J12.16	I2S_1_FS	Output	Audio left/right frame select signal to an I2S compliant audio device on the breakout board
J12.18	I2S_1_CLK	Output	Audio bit clock output to an I2S compliant audio device on the breakout board

11 SD Card Interface

The 96B compatible carrier board provides single micro SD Card receptacle that supports both +3.3-volt and +1.8-volt SD Cards through the use of level shifter between the module and connector.

The micro SD card connector power and level shifter are sourced from the buck regulator.

Refer to the micro SD card specifications for electrical and power requirements. Refer to the NXP IP4856CX25 datasheet for the SD card interface signal specifications. The power from the level shifter can support a maximum current of 100 mA and has a supply voltage of 3.3V if SDCARD LVL SEL is logic High or 1.8V if SDCARD LVL SEL is logic Low.

Table 20. Micro SD card connector pinout

J5 Pin	Net Name	Direction	Signal Description
1	SDCARD_D2_CONN	Bidirectional	Data lane 2
2	SDCARD_D3_CONN	Bidirectional	Data lane 3
3	SDCARD_CMD_CONN	Bidirectional	
4	+V3P3V_MICROSD	Output	+3.3 volt or +1.85 V supply to SD card
5	SDCARD_CLK_CONN	Output	
6	GND	Ground	Ground
7	SDCARD_D0_CONN	Bidirectional	Data lane 0
8	SDCARD_D1_CONN	Bidirectional	Data lane 1
9	GND	Ground	Detection lever
10	SDCARD_CD_N_CONN	Input	
11,12,13,14	Shield ground	Ground	EMI and ESD protection

12 SPI Interface

The 96B compatible carrier board routes two SPI interfaces from the module onto the low speed and high speed connectors for development use.

Table 21. SPI mapping to the low speed and high speed connectors

Connector.Pin #	Signal Name	Direction at Breakout Connector	Signal Description
J13.9	SPI_0_CLK	Input	SPI port 0 Clock
J13.7	SPI_0_FSO	Input	SPI port 0 slave select 0
J13.11	SPI_0_MISO	Output	SPI port 0 receive data
J13.1	SPI_0_MOSI	Input	SPI port 0 transmit data
J12.10	SPI_1_CLK_LS	Output	SPI port 1 Clock
J12.6	SPI_1_FSO_LS	Output	SPI port 1 slave select 0
J12.8	SPI_1_FS2_LS	Output	SPI port 1 slave select 2, hardware strap with disable boot from SD card functionality
J12.2	SPI_1_MISO_LS	Input	SPI port 1 receive data
J12.4	SPI_1_MOSI_LS	Output	SPI port 1 transmit data

13 UART Interfaces

The 96B compatible carrier board exposes two UART ports, UART_0 and UART_1, at the low speed connector for peripheral device communications and system development activities.

Table 22. UART mapping to low speed connector

Connector.Pin #	Signal Name	Direction	Signal Description
J12.3	UART_0_CTS	Input	UART port 0 clear-to-send
J12.9	UART_0_RTS	Output	UART port 0 ready-to-send
J12.7	UART_0_RXD	Input	UART port 0 receive data
J12.5	UART_0_TXD	Output	UART port 0 transmit data
J12.13	UART_2_RXD	Input	UART port 1 receive data
J12.11	UART_2_TXD	Output	UART port 1 transmit data, and hardware strap

The UART controllers are integrated into the module. Consult <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Compute Module Datasheet* for specific modes of operation.

UART1 of the module is dedicated to serial debug port J9 on the expansion board.

13.1 Debug header for UART (optional)

A single 6-pin header, in a 1x6 configuration can be soldered on the 96B compatible carrier board at J9 to enable access to UART2, the Linux console output port.

Note: In addition to the UART2 signal availability on this header, the UART2 signals are also routed to **UART1** on the low speed expansion connector, allowing the end user to install a mezzanine board which may then use the UART2 signals for peripheral connections.

For debug purposes one may either connect an RS-232 type console to the signals on the UART debug header, or use an “off-the-shelf” UART to USB adapter to connect a PC to this debug port.

Table 23. UART debug header pinout

UART Debug Header Pin #	Intel® Joule™ Module Expansion Connector		Description
	Net Name	Connector.Pin #	
1	GND	--	Ground signal.connect to system ground
2	UART_2_RTS	J2.76	Ready To Send signal (RTS) for UART2, a high speed UART at 1.8-volt signal levels
3	No Connect	--	No connect
4	UART_2_RXD	J2.80	Receive signal for UART2, a standard speed UART at 1.8-volt signal levels
5	UART_2_TXD	J2.78	Transmit signal for UART2, a standard speed UART at 1.8-volt signal levels. UART_2_TXD is one of the boot strapping pins for the Intel Joule module. Refer to Table 5 for the boot strapping requirements for this signal
6	UART_2_CTS	J2.74	Clear To Send signal (CTS) for UART2, a high speed UART at 1.8-volt signal levels

14 USB

The 96B compatible carrier board includes a discrete, 4 port hub device at U2 that serves to bridge the modules USB interface to the Type A and Type C connectors.

Refer to <https://software.intel.com/en-us/intel-joule-getting-started> and search for *Compute Module Datasheet* for specifications and features of the USB subsystem.

14.1 USB Type-A interfaces and high speed USB 2.0 port

Two USB Type-A connectors (J6 and J8) are connected to the lower two ports of the USB3.0 hub, as shown in the system block diagram (refer to Figure 10). Each connector can simultaneously supply up to 900mA through independent, dedicated load switches on the +V5P0V rail.

The on-board USB hub also provides a port to the high speed connector as HUB_3_USB2

Table 24. USB Type-A (J6) connector pinout

Pin #	Net Name	Direction	Signal Description
1	+V5P0V_USBA_1	Output	VBUS power
2	USBA_1_USB2_1_DN	Bidirectional	USB 2.0 data negative
3	USBA_1_USB1_1_DP	Bidirectional	USB 2.0 data positive
4	GND	Ground	Power return ground
5	USBA_1_USB3_1_RX_DN	Input	USB 3.0 data receive negative
6	USBA_1_USB3_1_RX_DP	Input	USB 3.0 data receive positive
7	GND	Ground	Signal return ground
8	USBA_1_USB3_1_TX_DN	Output	USB 3.0 data transmit negative
9	USBA_1_USB3_1_TX_DP	Output	USB 3.0 data transmit positive
10,11,12,13	Shield Mounting Ground	Ground	Power return ground

Table 25. USB Type-A (J8) connector pinout

Pin #	Net Name	Direction	Signal Description
1	+V5P0V_USBA_2	Output	VBUS power
2	USBA_2_USB2_1_DN	Bidirectional	USB 2.0 data negative
3	USBA_2_USB1_1_DP	Bidirectional	USB 2.0 data positive
4	GND	Ground	Power return ground
5	USBA_2_USB3_1_RX_DN	Input	USB 3.0 data receive negative
6	USBA_2_USB3_1_RX_DP	Input	USB 3.0 data receive positive

Pin #	Net Name	Direction	Signal Description
7	GND	Ground	Signal return ground
8	USBA_2_USB3_1_TX_DN	Output	USB 3.0 data transmit negative
9	USBA_2_USB3_1_TX_DP	Output	USB 3.0 data transmit positive
10,11,12,13	Shield Mounting Ground	Ground	Power return ground

14.2 USB Type-C Connector

A USB mux device (U6) provides cable reversibility functions for the USB Type-C connector while load switch (U17) provide 300ma from the +5P0V rail for CC lines (+5VP0V_VCONN) and load switch (U22) provides 900 mA from the +5P0V rail for On-The-Go service.

Table 26. USB type-C connector pinout

Pin #	Net Name	Direction	Signal Description
A1	GND	Ground	Ground
A2	USBC_USB3_0_MUX1_TX_DP	Output	USB 3.0 data transmit positive, from USB 3.0 2:1 mux
A3	USBC_USB3_0_MUX1_TX_DN	Output	USB 3.0 data transmit negative, from USB 3.0 2:1 mux
A4	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
A5	USB_TYPC_CONN_CC1	Bidirectional	USB type-C configuration channel 1
A6	USBC_USB2_0_DP	Bidirectional	USB 2.0 data positive
A7	USBC_USB2_0_DN	Bidirectional	USB 2.0 data negative
A8	TP_USB_TYPC_SBU1_CONN	Bidirectional	Test Point
A9	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
A10	USBC_USB3_0_MUX2_RX_DN	Input	USB 3.0 data receive negative, from USB 3.0 2:1 mux
A11	USBC_USB3_0_MUX2_RX_DP	Input	USB 3.0 data receive positive, from USB 3.0 2:1 mux
A12	GND	Ground	Ground
B1	GND	Ground	Ground
B2	USBC_USB3_0_MUX2_TX_DP	Output	USB 3.0 data transmit positive, from USB 3.0 2:1 mux
B3	USBC_USB3_0_MUX2_TX_DN	Output	USB 3.0 data transmit negative, from USB 3.0 2:1 mux
B4	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink

Pin #	Net Name	Direction	Signal Description
B5	USB_TYPC_CONN_CC2	Bidirectional	USB Type-C configuration channel 2
B6	USBC_USB2_0_DP	Bidirectional	Bidirectional
B7	USBC_USB2_0_DN	Bidirectional	Bidirectional
B8	TP_USB_TYPC_SBU2_CONN	Bidirectional	Test Point
B9	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
B10	USBC_USB3_0_MUX1_RX_DN	Input	USB 3.0 data receive negative, from USB 3.0 2:1 mux
B11	USBC_USB3_0_MUX1_RX_DP	Input	USB 3.0 data receive positive, from USB 3.0 2:1 mux
B12	GND	Ground	Ground

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