

TABLE OF CONTENTS

[illegible]96Boards^{*} Consumer Edition Reference Design for the Intel(R) Joule(TM) Compute Module.

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COVER PAGE

BOM_RELEASE_DATE		2016	PB_NUMBER FAB1		
SIGNATURE		DATE	INTEL CORPORATION 2200 MISSION BLVD SANTA CLARA, CA 95054 TITLE GT96B Expansion Board - provided under Creative Commons v3 unported license.		
DRN_BY Intel Design	2017				
CHK_BY Intel Design	2016				
ENGR_APVD MIG	2016				
VARIANT:				REV	PAGE
N/A				1.20.00	1/24

BPAGE DRAWING

gt96b.sch_1.1
Fri Feb 17 17:47:20 2017

8		7		6		5		4		3		2		1	
D														D	
C														C	
B														B	
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VARIANT:

N/A

REV

1.20.00

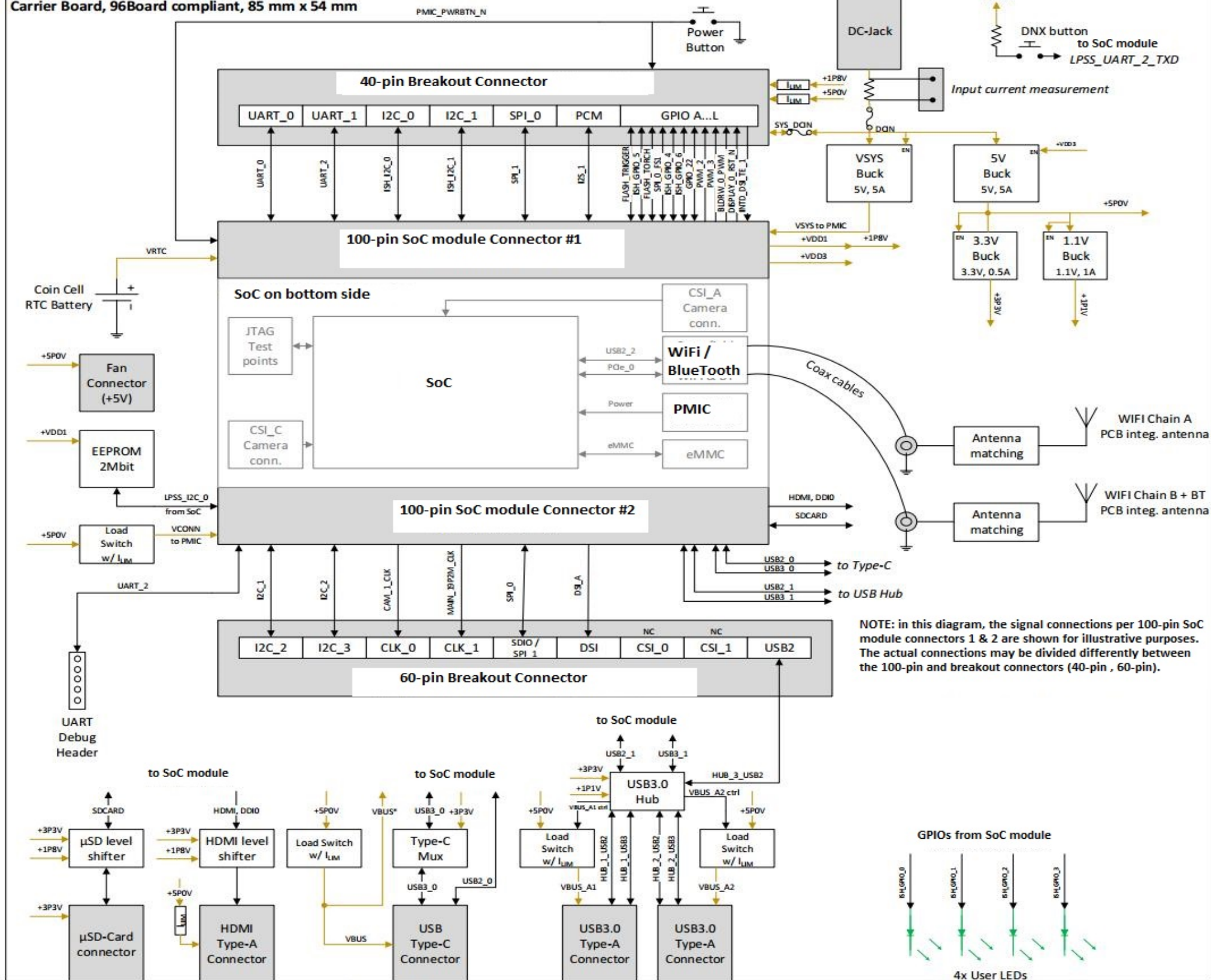
PAGE

2/24

BLOCK DIAGRAM

REV 1.0

Carrier Board, 96Board compliant, 85 mm x 54 mm



NOTE: in this diagram, the signal connections per 100-pin SoC module connectors 1 & 2 are shown for illustrative purposes. The actual connections may be divided differently between the 100-pin and breakout connectors (40-pin , 60-pin).

*VBUS to PMIC VBUS-detection.
No power input to the system

BPAGE DRAWING

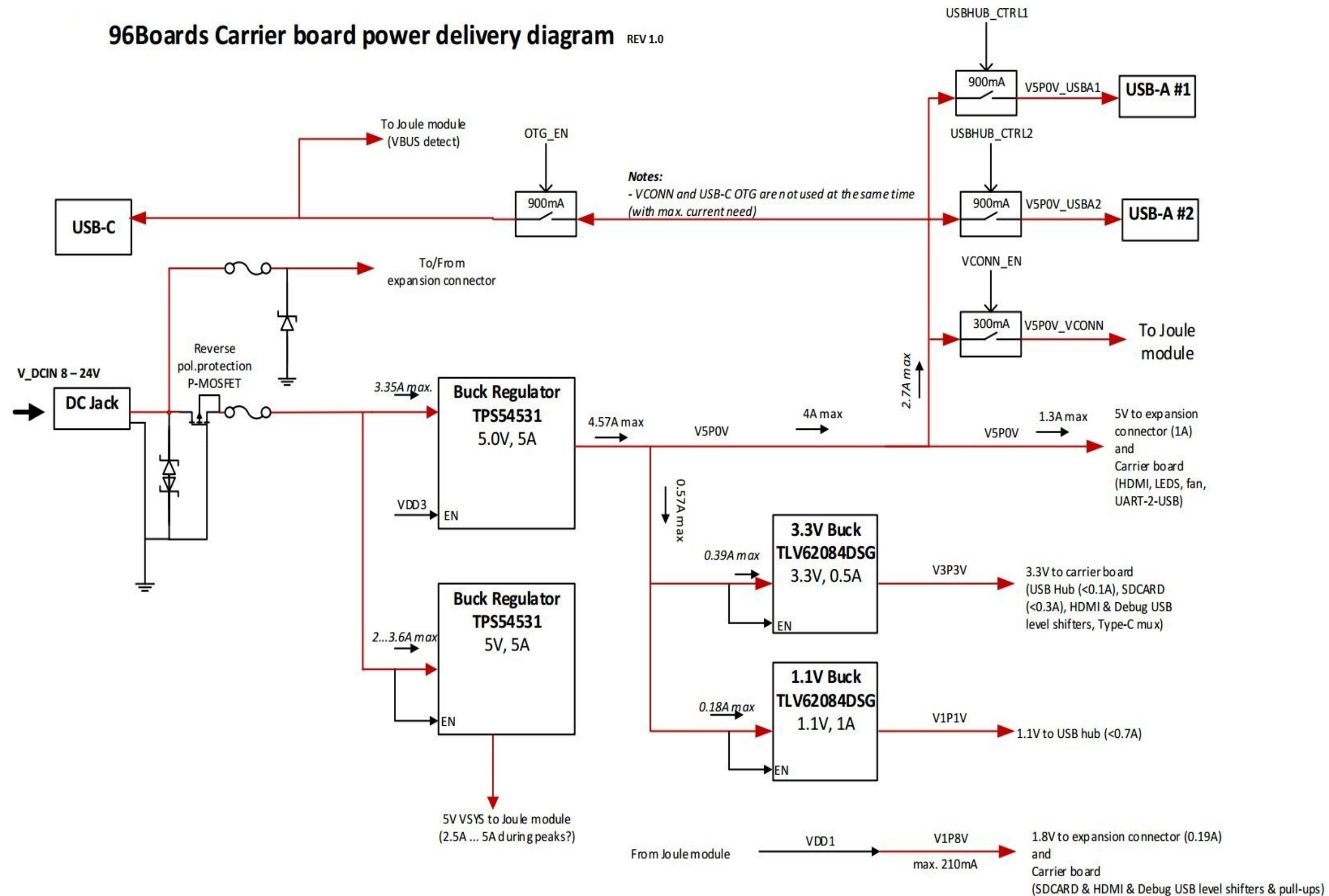
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Fri Feb 17 17:47:20 2017

BLOCK DIAGRAM

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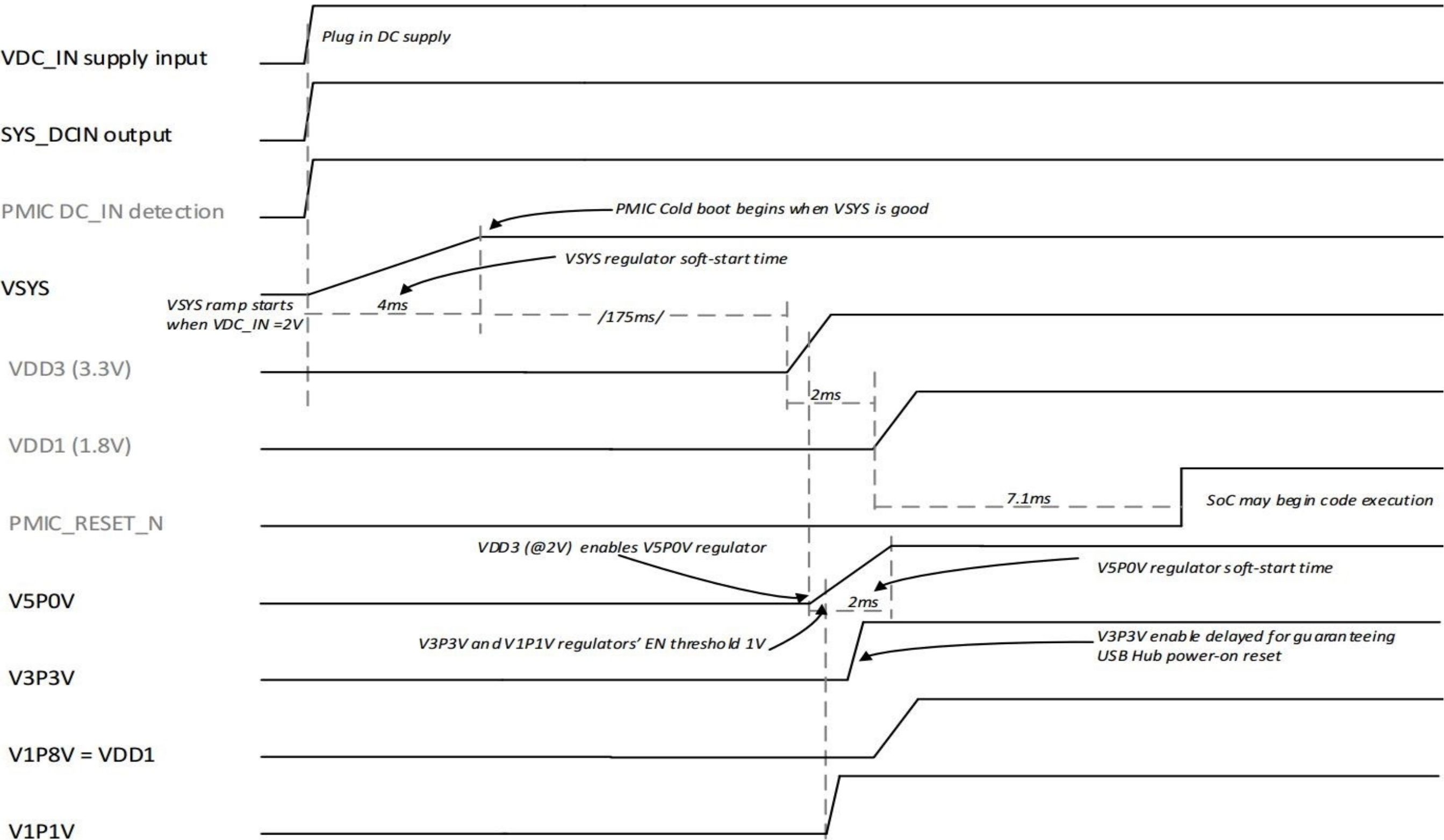
REV	PAGE
1.20.00	3/24

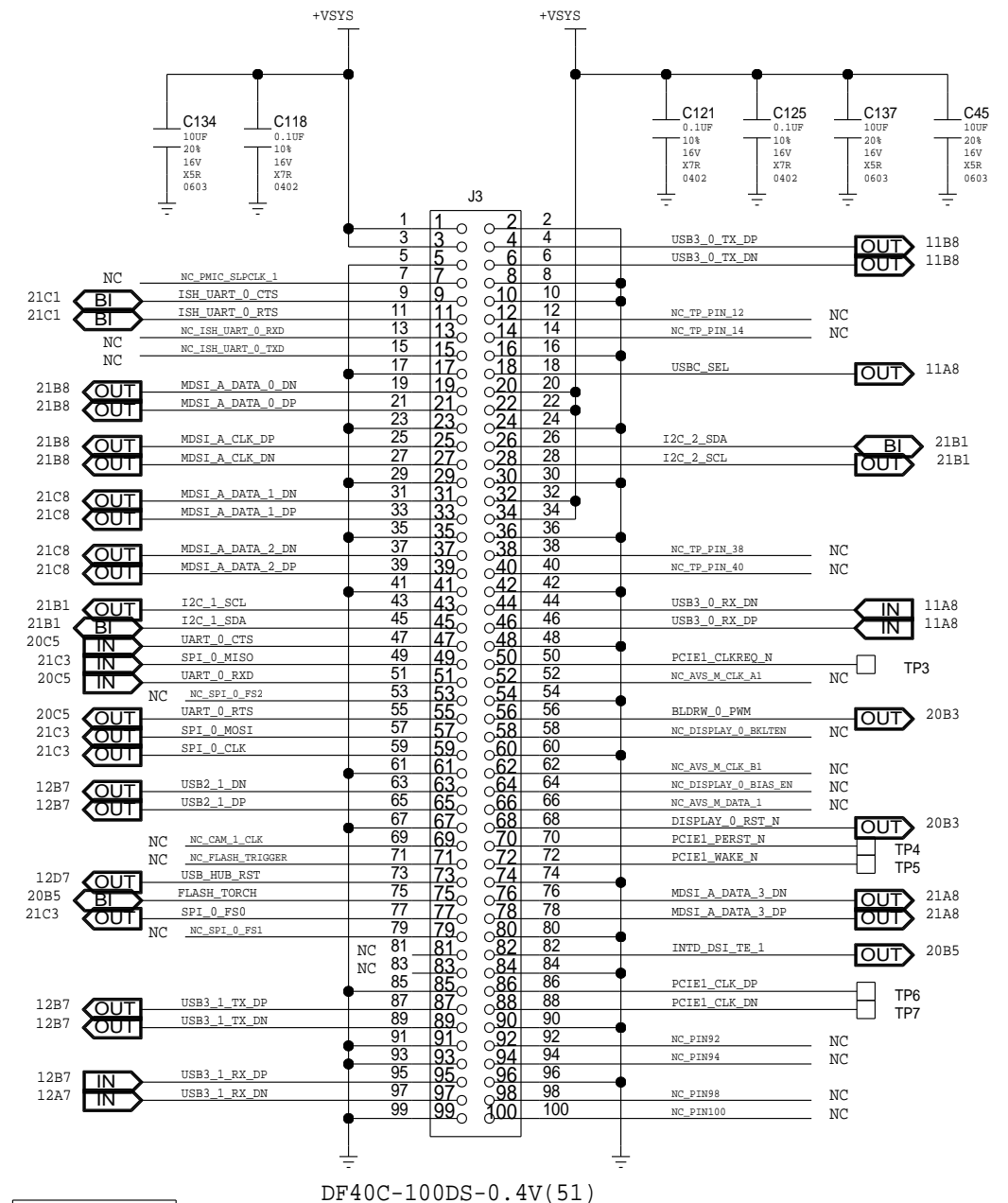
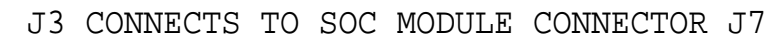
96Boards Carrier board power delivery diagram REV 1.0



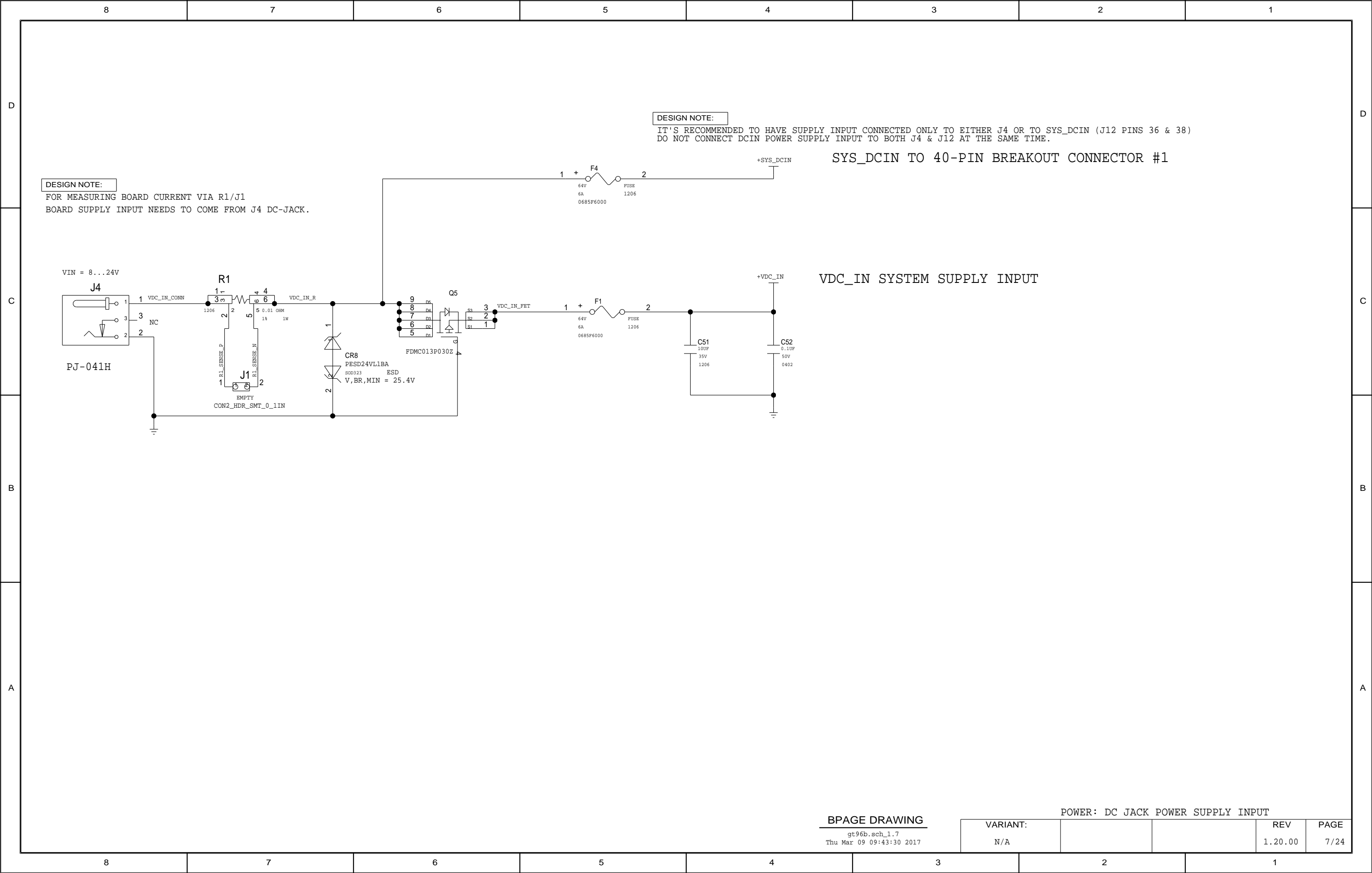
Carrier board power sequencing REV 1.0

Grey supplies are on SoC module.





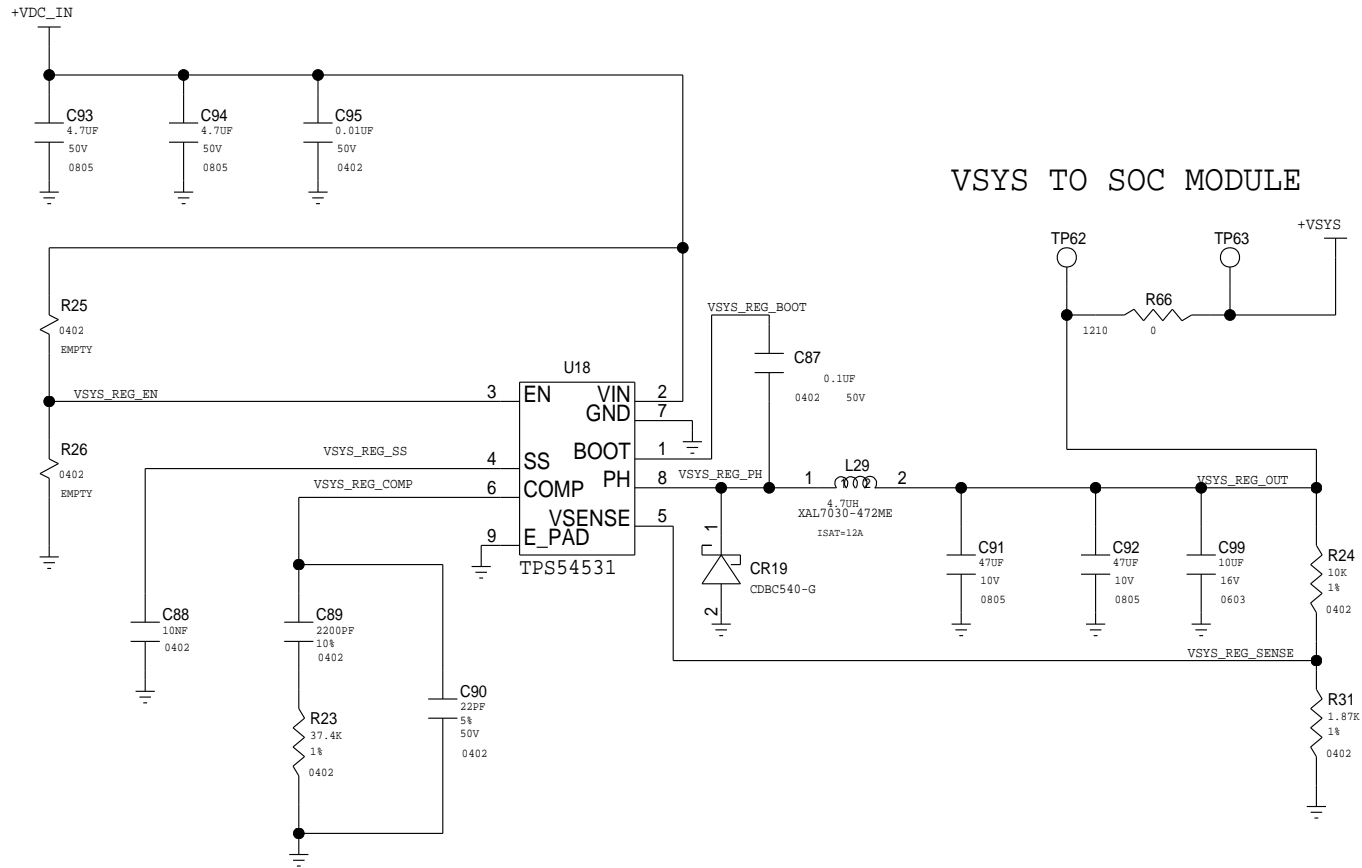
USB HUB RESET, FOR RESETTING USB HUB, OPTIONAL FOR FAB A FOR R&D USE.
NOT USED BY DEFAULT (Q1 'EMPTY' ON PAGE 12).



DCIN TO VSYS BUCK REGULATOR

DCIN TO 5.0V BUCK REGULATOR

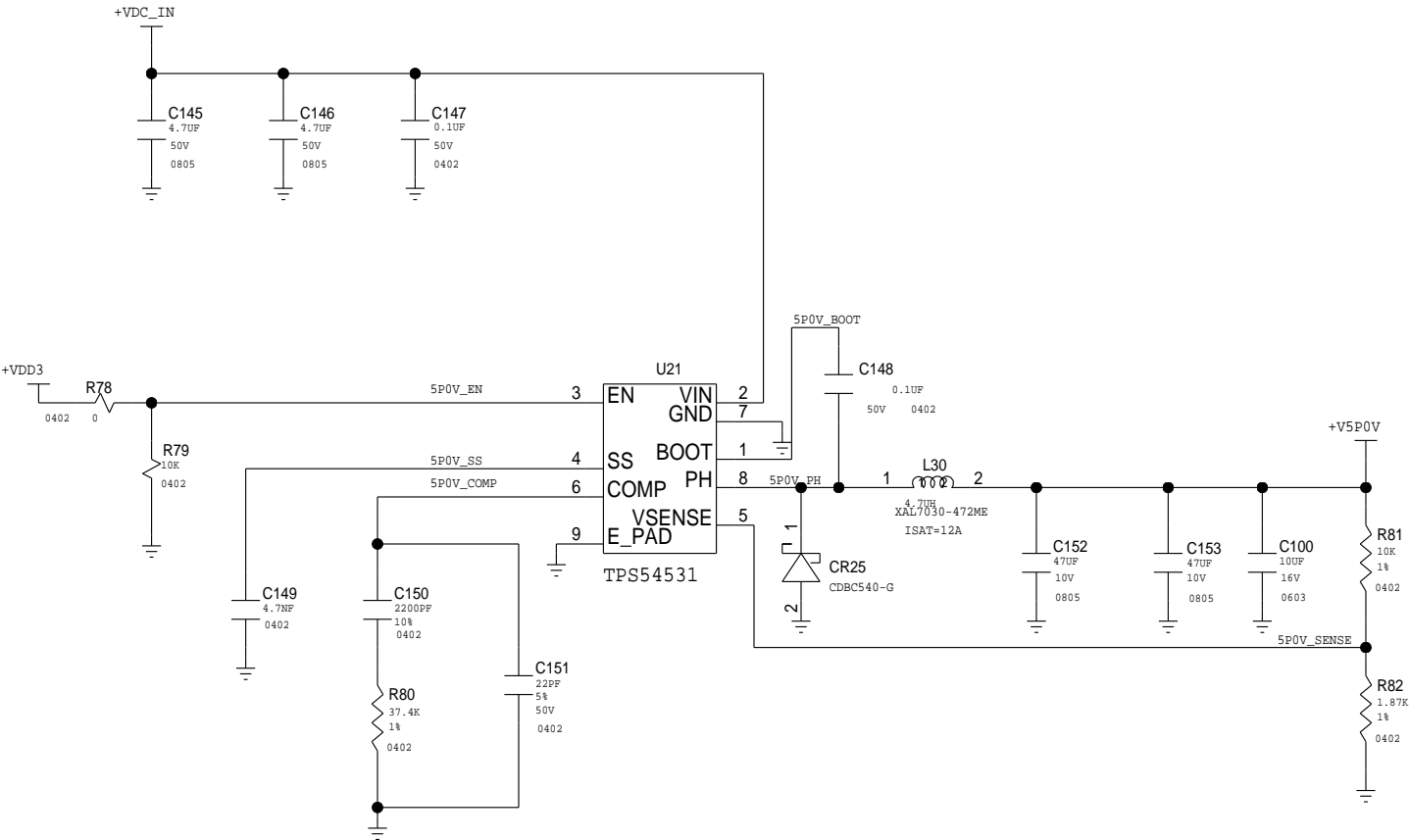
VSYS TO SOC MODULE



DESIGN NOTE:

ASSEMBLE (INSTALL) R25 AND R26 TO PROGRAM U18 EXTERNAL INPUT UNDERVOLTAGE LOCKOUT. FLOAT EN TO ENABLE U18 BY USING INTERNAL UVLO OF MAX. 3.5V.

R25 & R26 VALUES FOR EXTERNAL UVLO HYSTERESIS:
 $R25 = (V_{IN_TH_START} - V_{IN_TH_STOP}) / 3\mu A$
 $R26 = 1.25V / ((V_{IN_TH_START} - 1.25V) / R25) + 1\mu A$



DESIGN NOTE:

U21 5V REGULATOR ENABLE FROM VDD3 FOR POWERING UP AND SHUTTING DOWN CARRIER BOARD ALONG WITH SOC MODULE

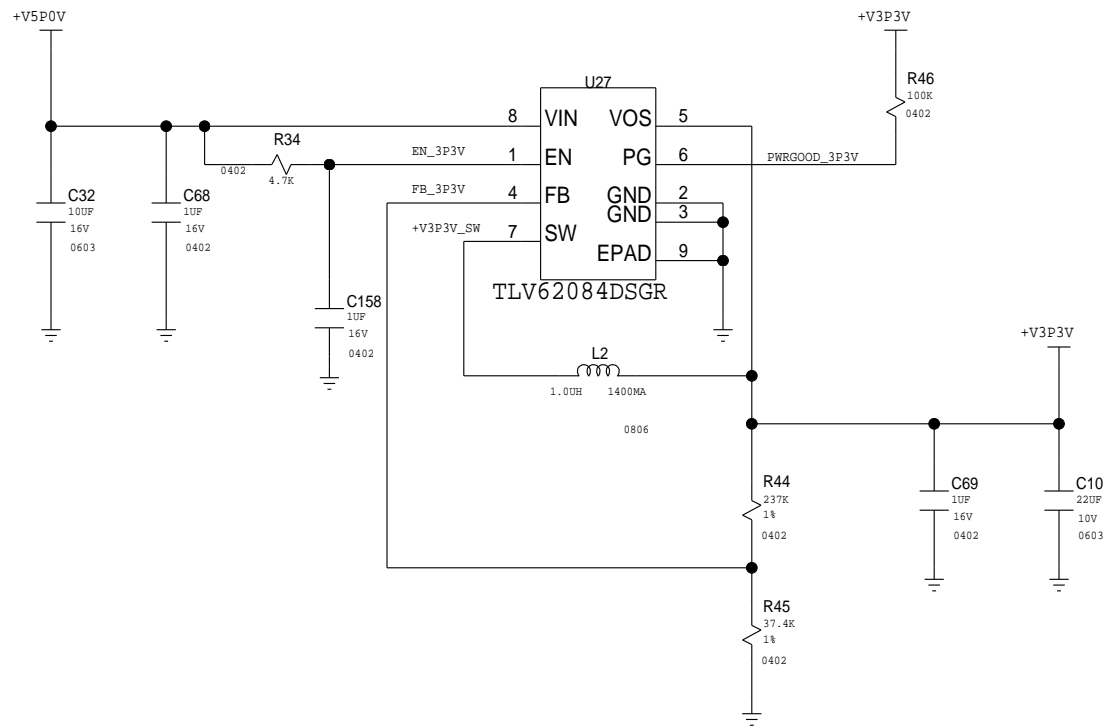
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gt96b.sch_1.8
Thu Mar 09 15:58:07 2017

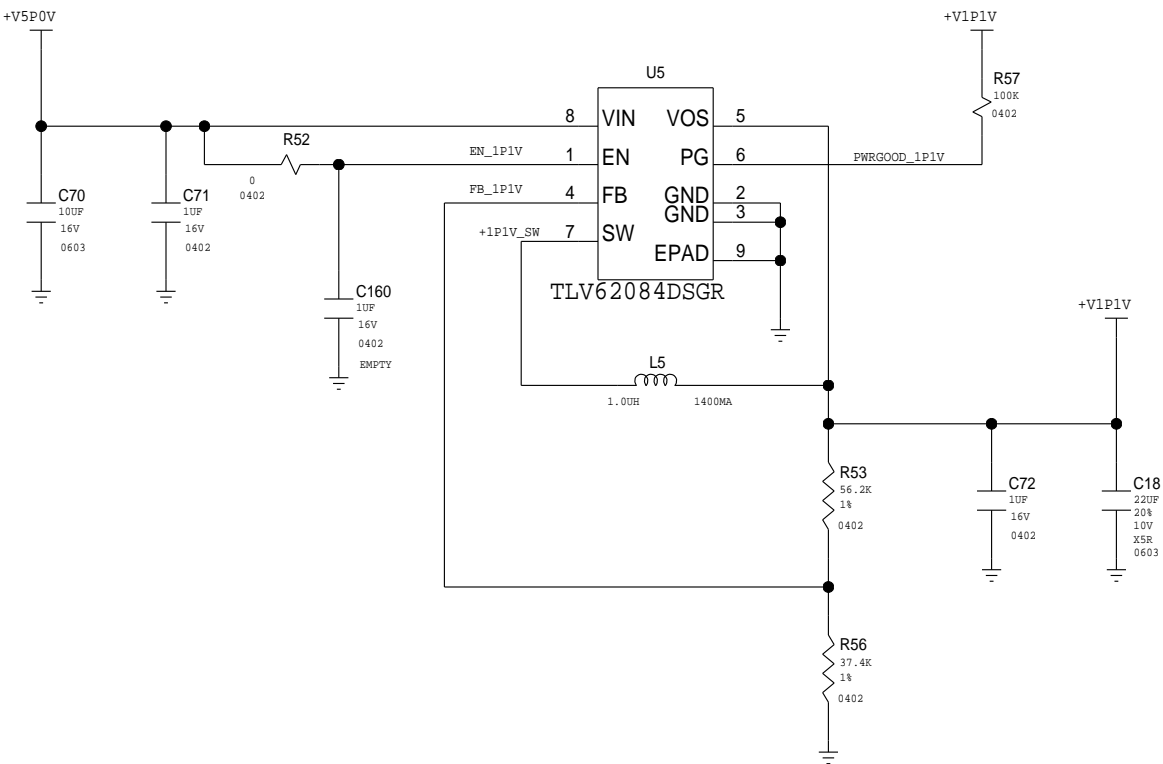
POWER: VSYS & 5V BUCK REGULATORS

VARIANT:	REV	PAGE
N/A	1.20.00	8/24

5.0V TO 3.3V BUCK REGULATOR



5.0V TO 1.1V BUCK REGULATOR FOR USB HUB



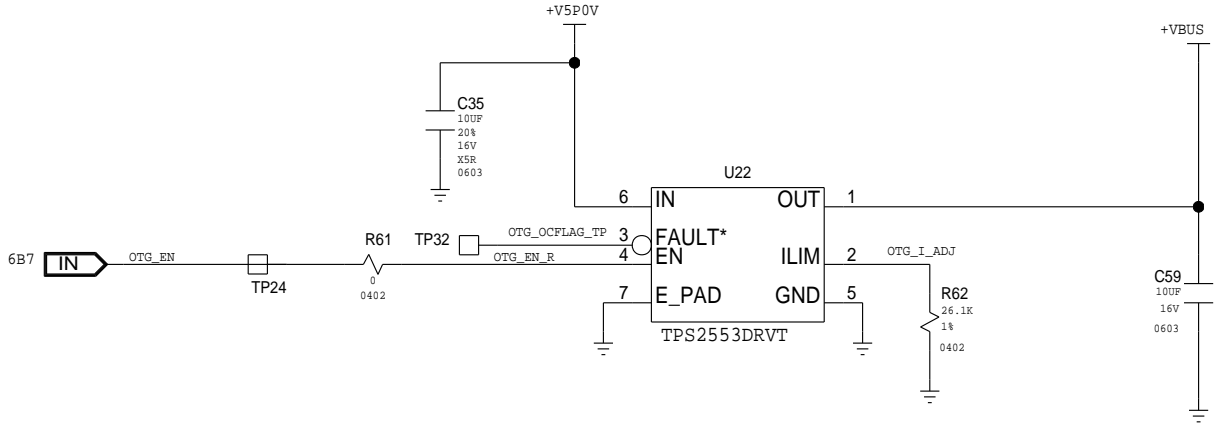
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gt96b.sch_1.9
Tue Mar 07 17:24:10 2017

POWER: 3P3V & 1P1V BUCK REGULATORS

VARIANT:	REV	PAGE
N/A	1.20.00	9/24

USB-C OTG LOAD SWITCH



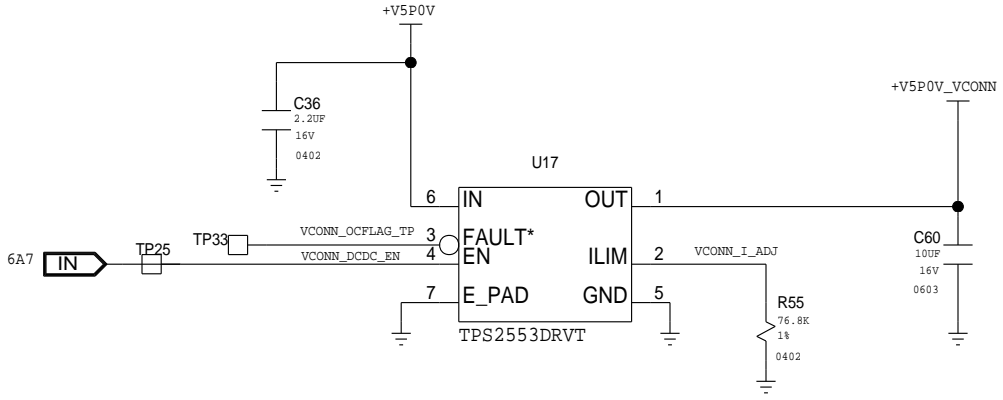
DESIGN NOTE:

```

ISET -> 26.1K = 1000MA CURRENT LIMIT
TO SUPPORT 900MA +VBUS OTG

```

USB-C VCONN LOAD SWITCH



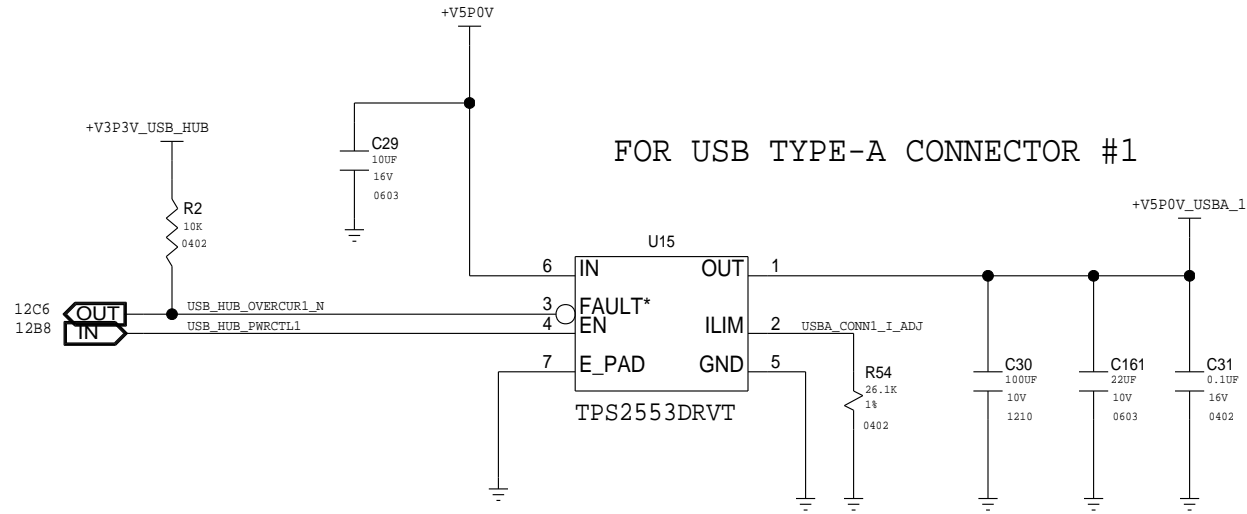
DESIGN NOTE:

```

ISET -> 76.8K
TO SUPPORT 300MA VCONN ON CC LINES

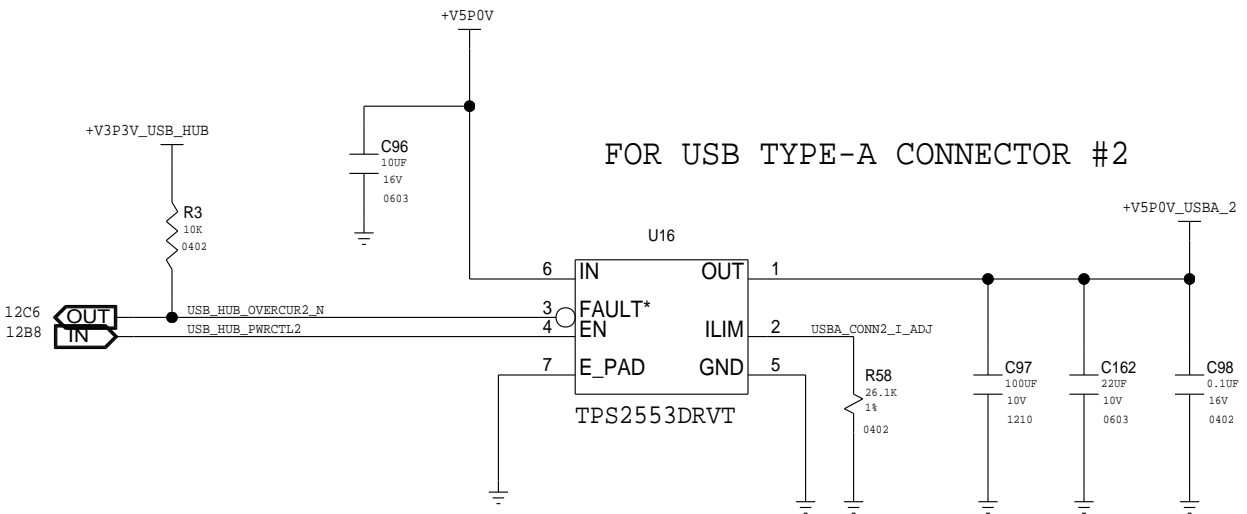
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USB 3.0 LOAD SWITCHES



DESIGN NOTE:

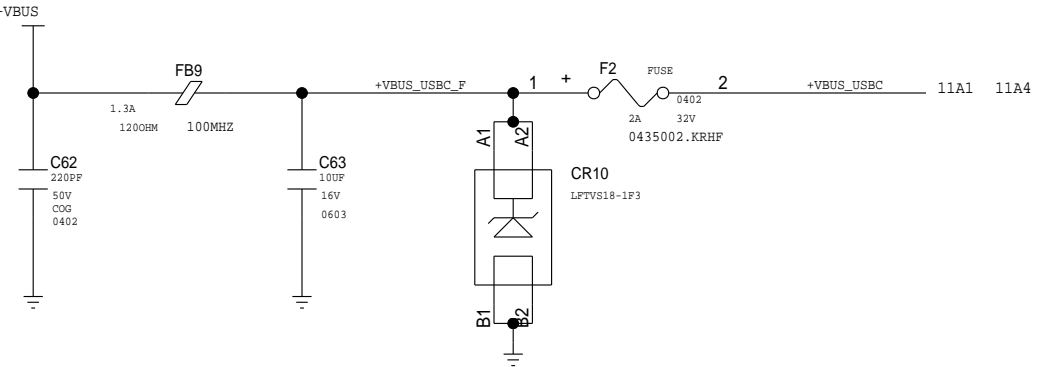
```
ILIM -> 26.1K = 1000MA CURRENT LIMIT
TO SUPPORT 900MA ON +V5P0V_USBA_1
FOR USB TYPE-A CONNECTOR #1
```



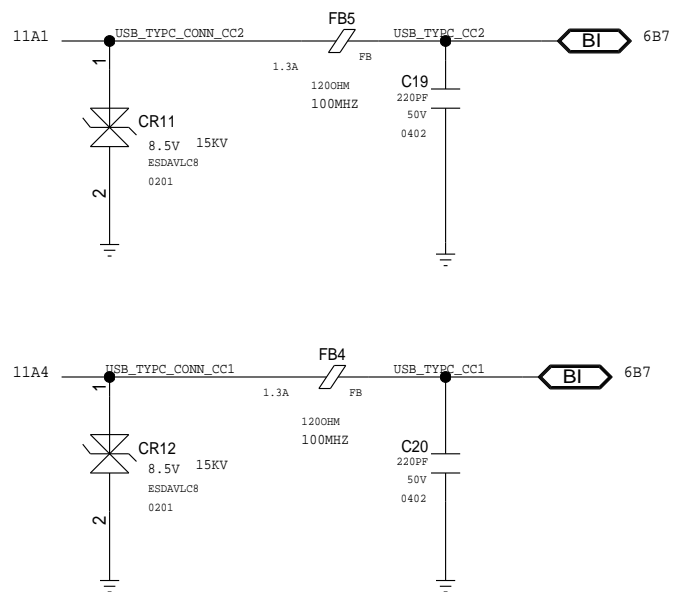
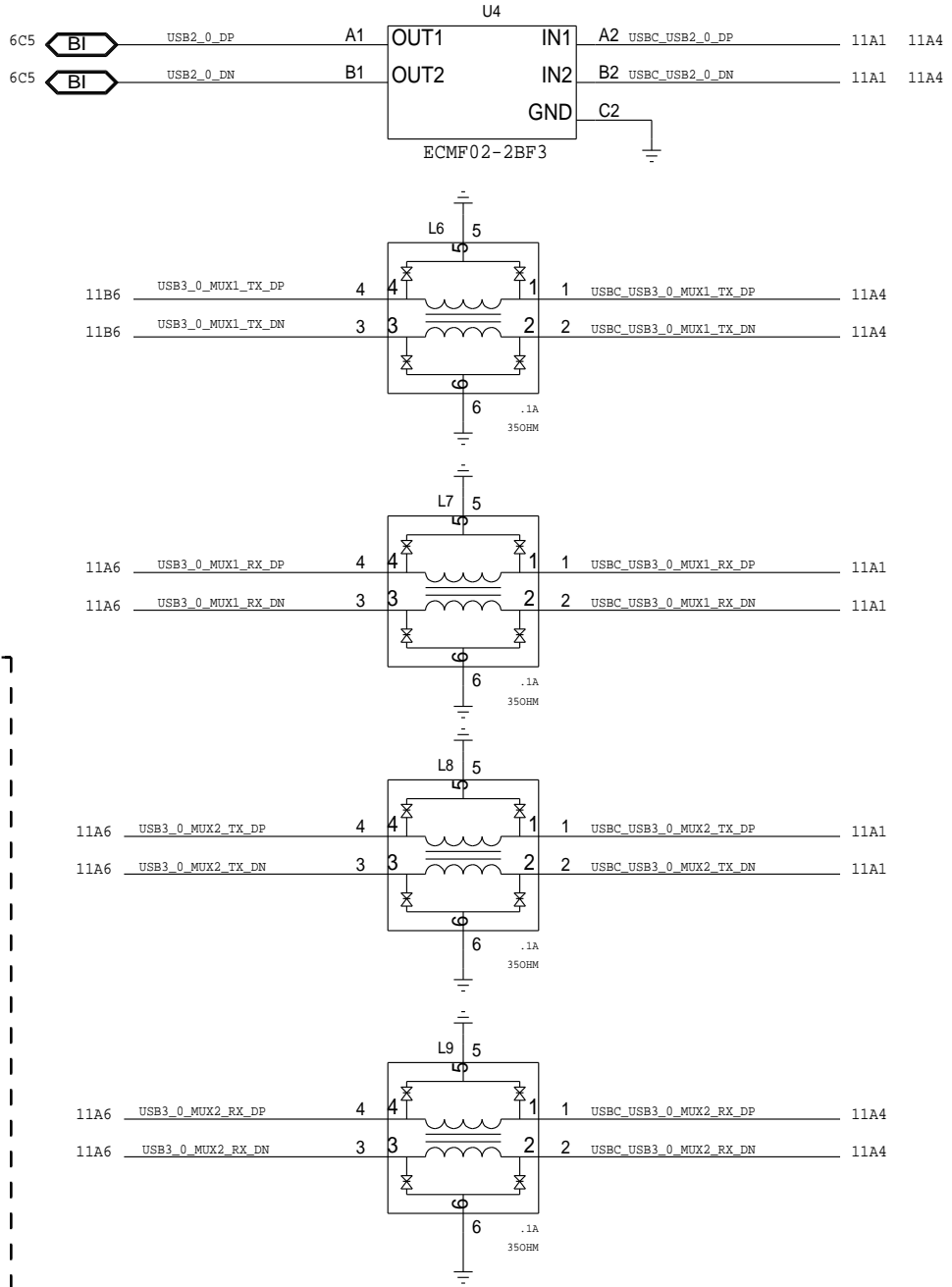
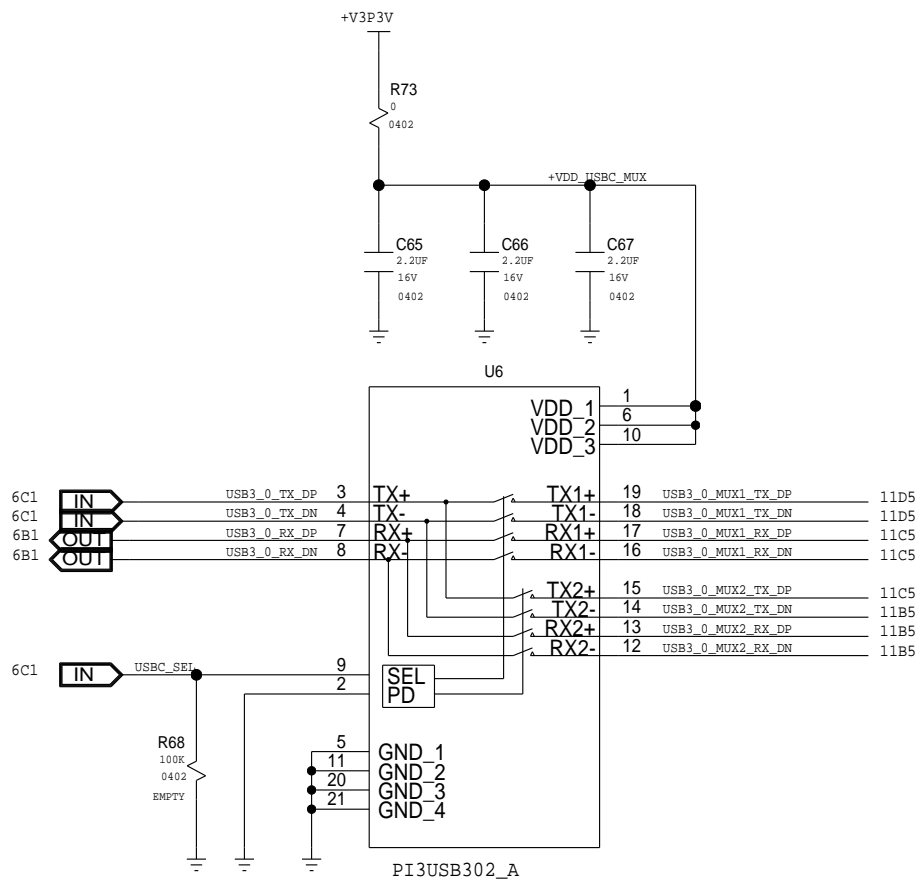
DESIGN NOTE:

```
ILIM -> 26.1K = 1000MA CURRENT LIMIT  
TO SUPPORT 900MA ON +V5P0V_USB  
FOR USB TYPE-A CONNECTOR #2
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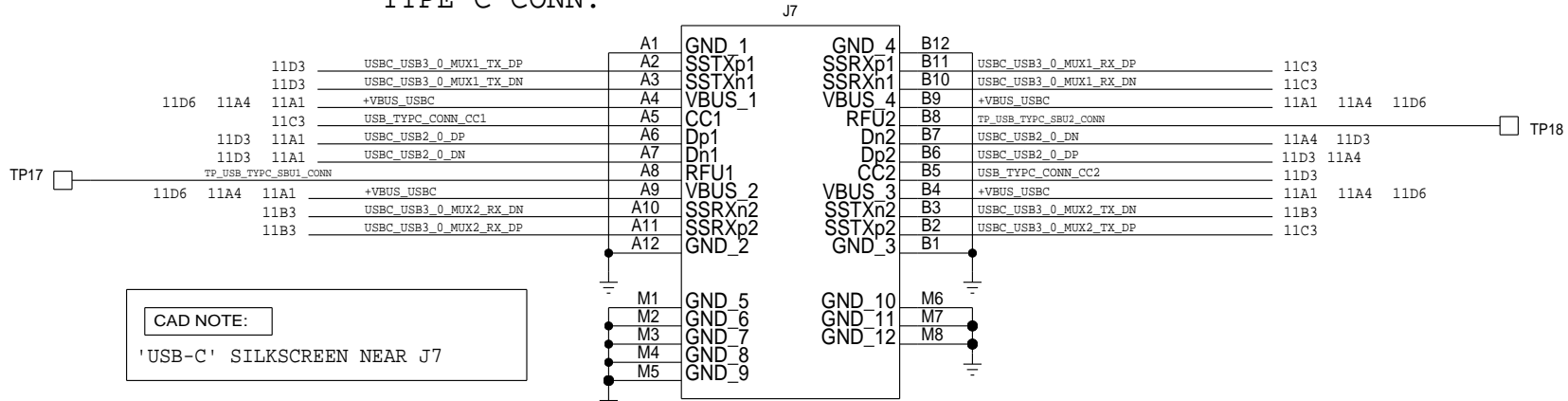
TYPE-C CMC, ESD FILTERS, DIODE PROTECT.



TYPE-C MUX



TYPE-C CONN.



CAD NOTE:
'USB-C' SILKSCREEN NEAR J7

BPAGE DRAWING

gt96b.sch_1.11
Thu Mar 09 16:06:29 2017

USB: USB TYPE-C

VARIANT:

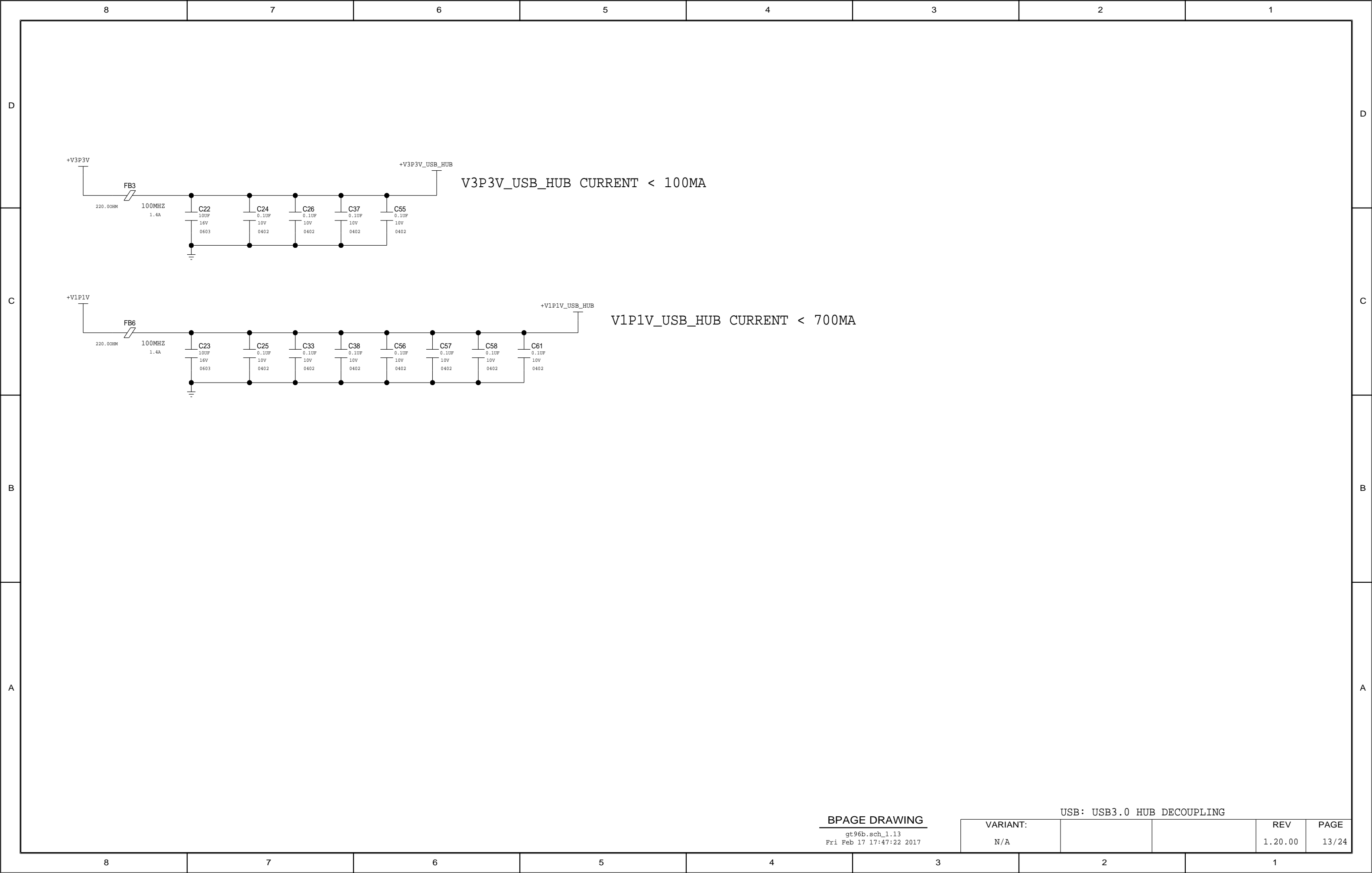
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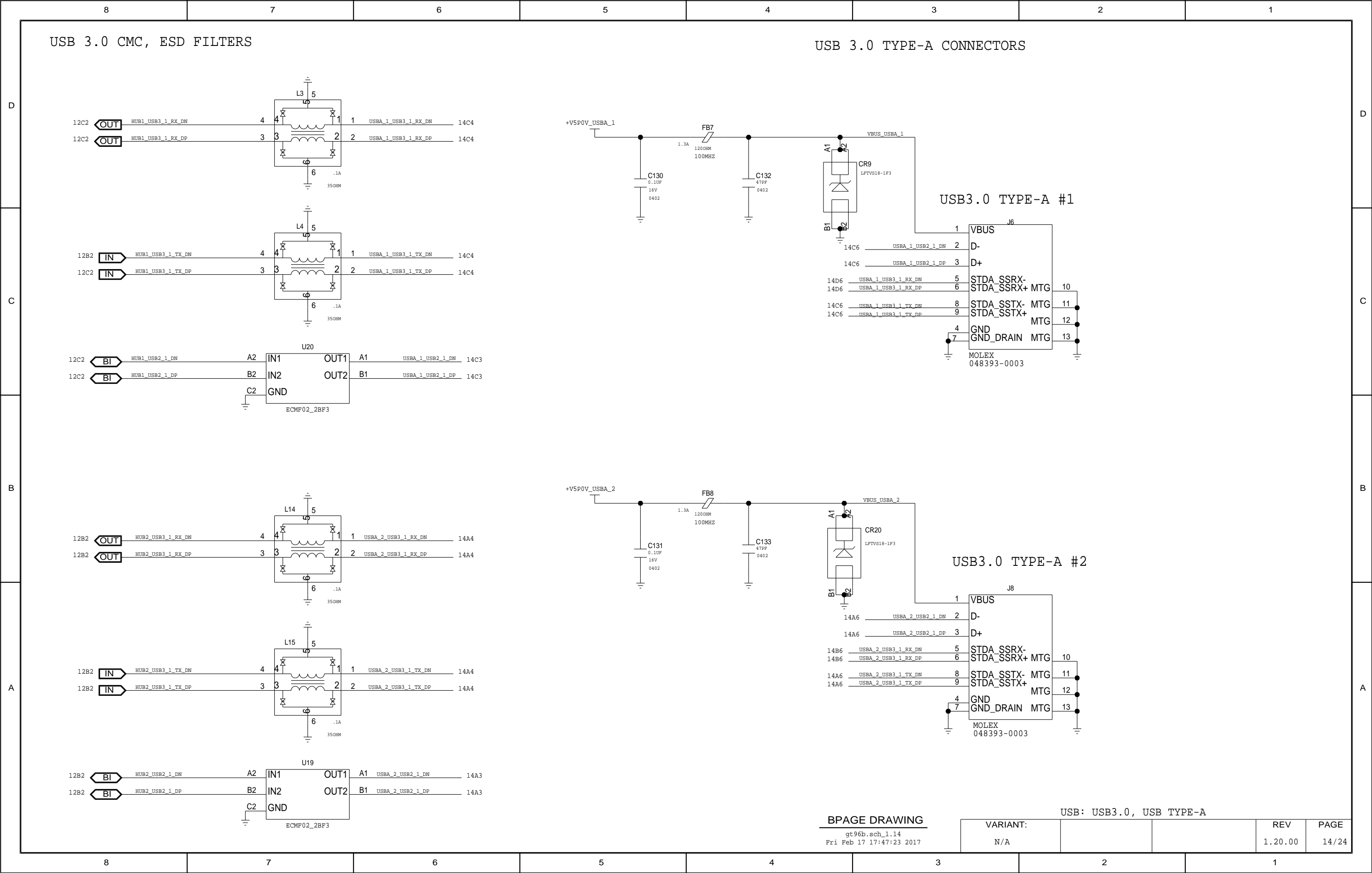
REV

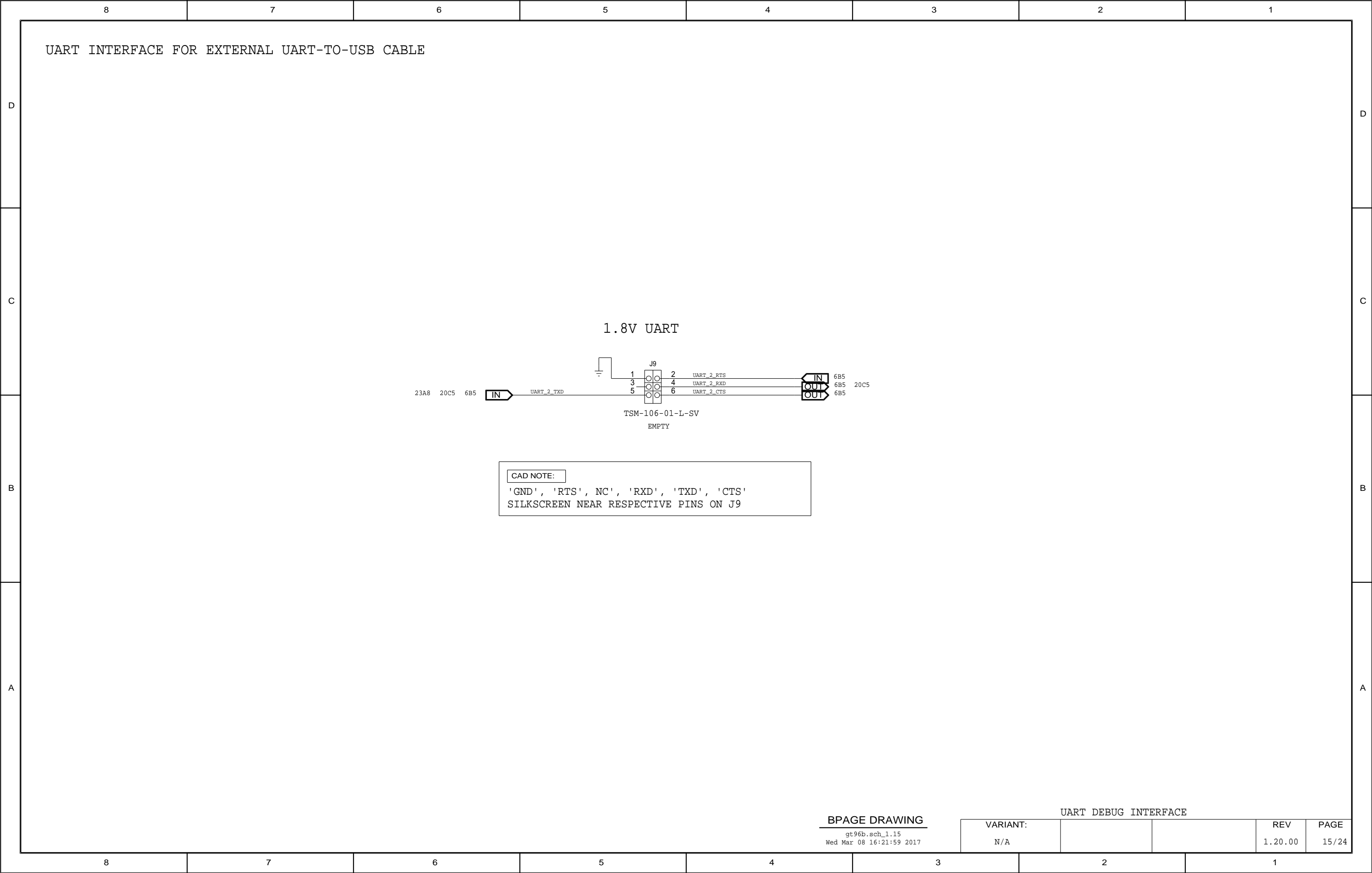
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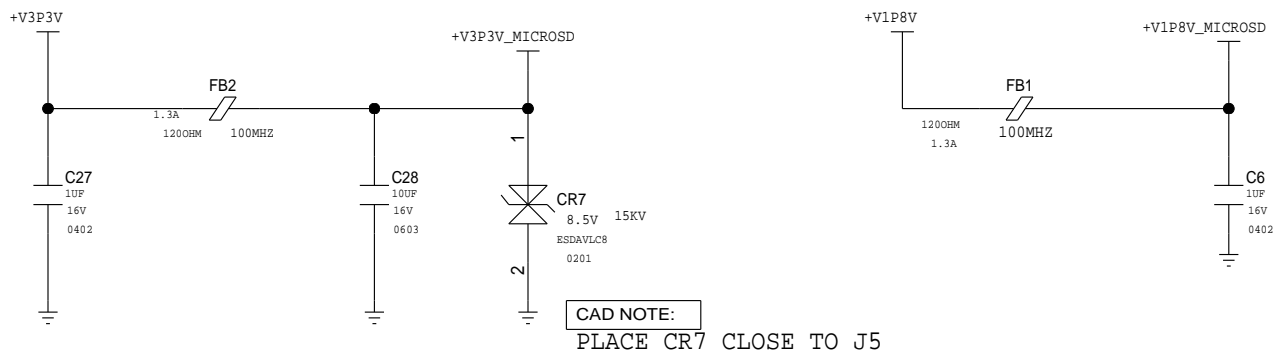
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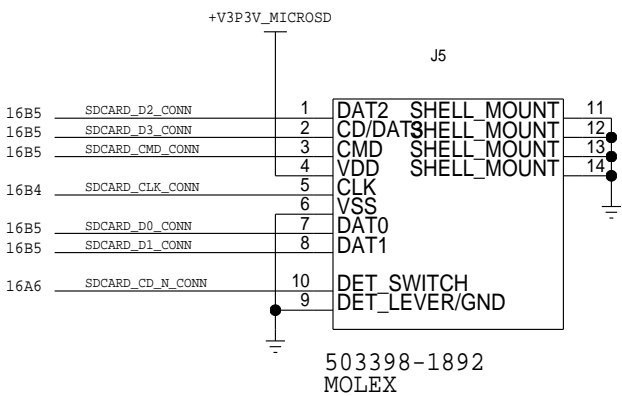
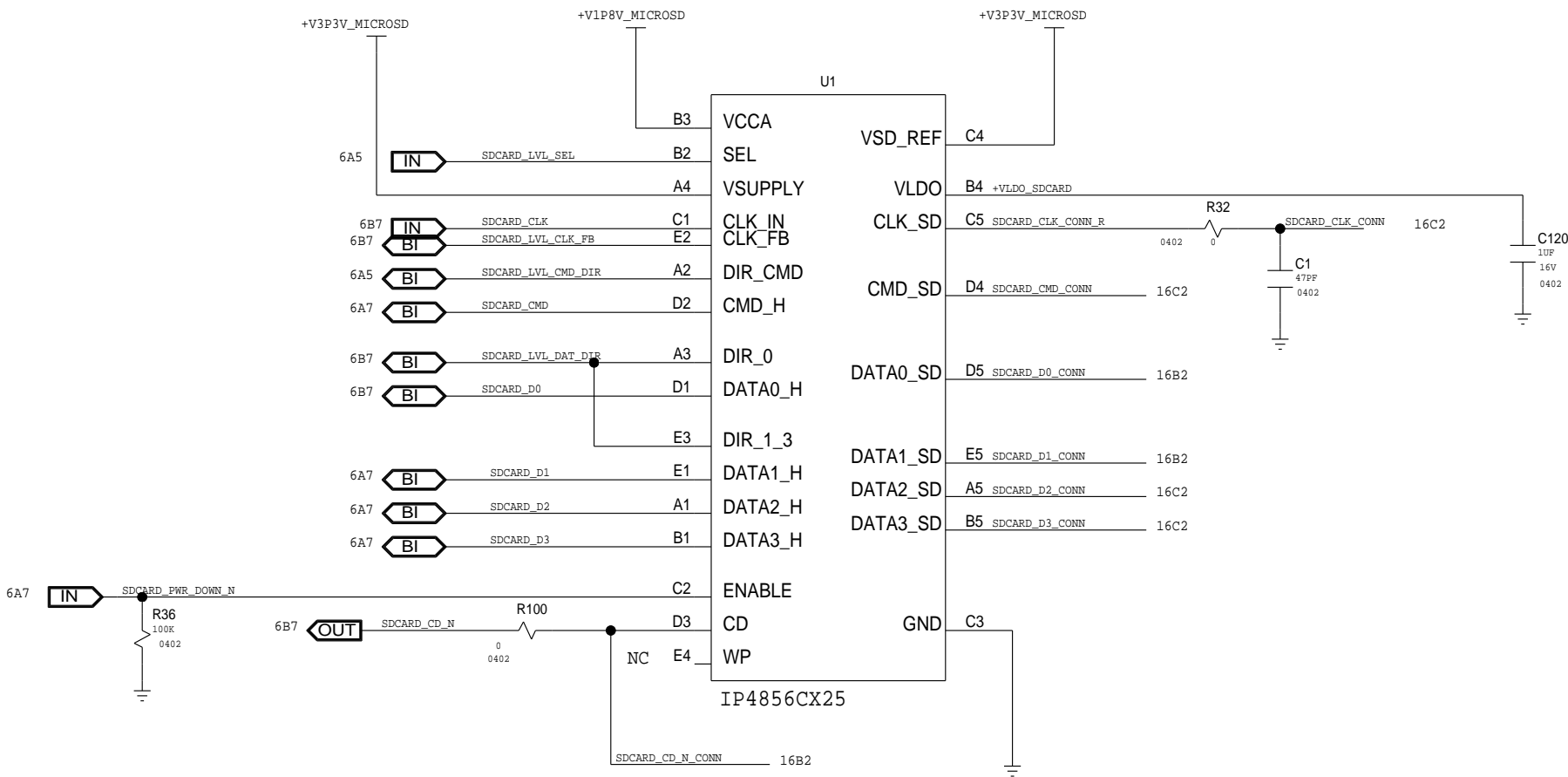




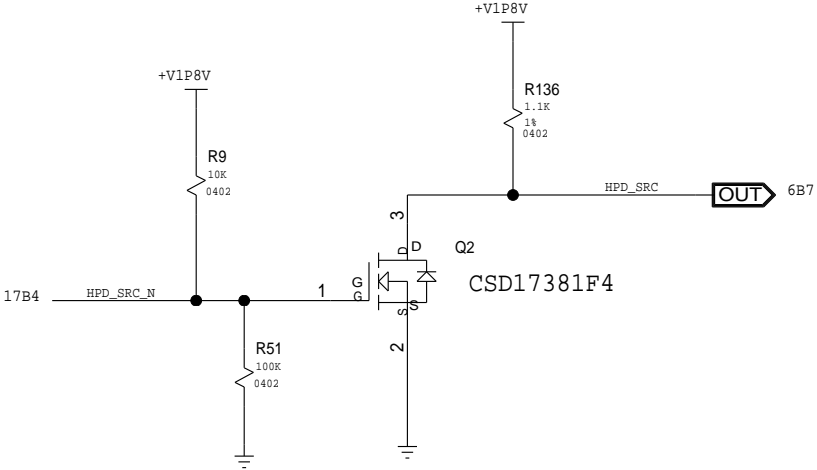
MICRO-SD LEVEL SHIFTER AND ESD, EMI FILTERING



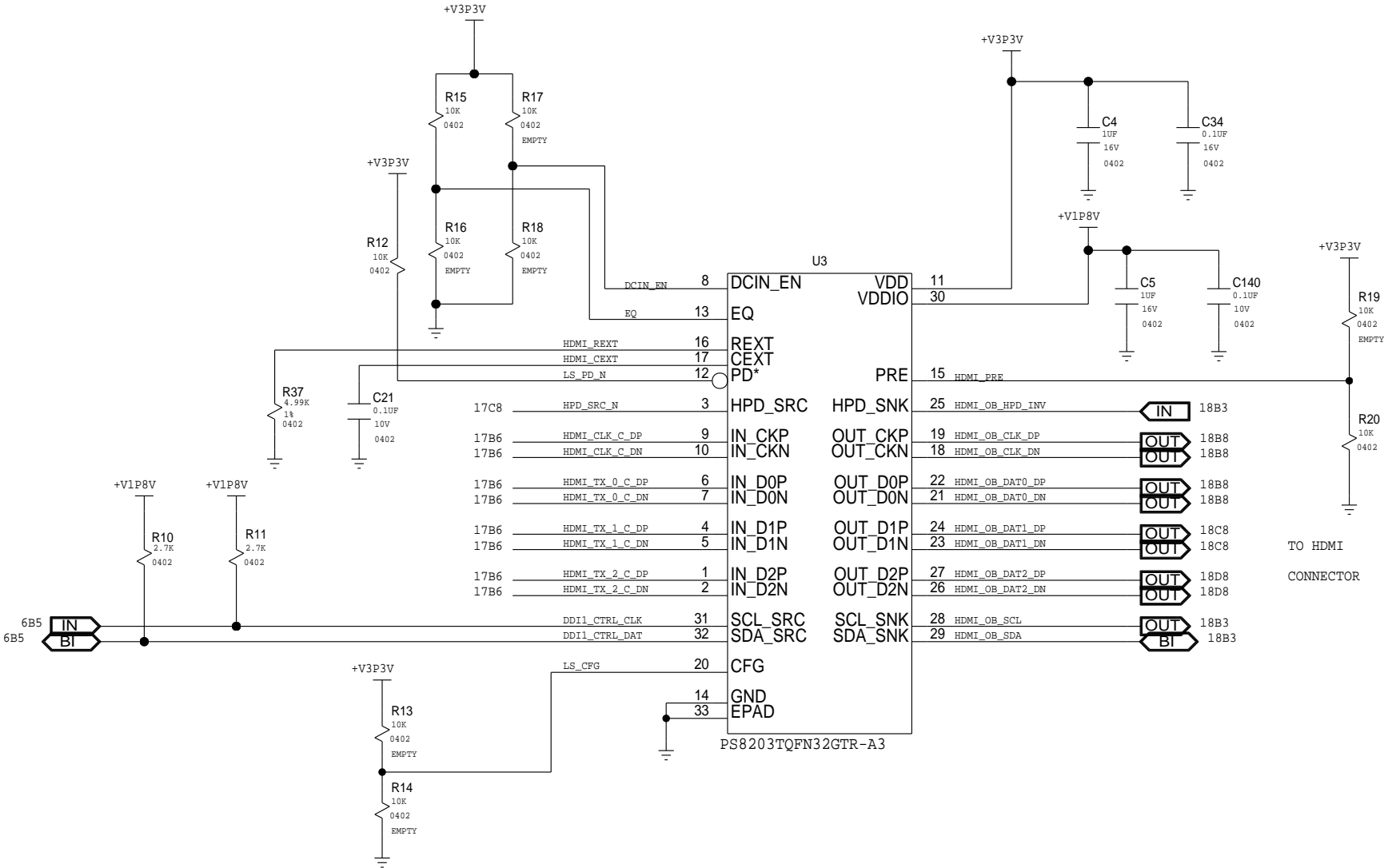
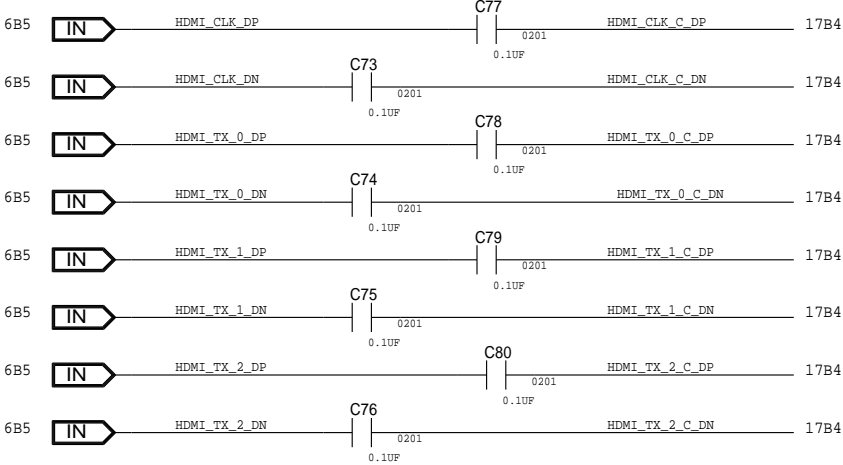
MICRO-SD CONN.



HDMI LEVEL SHIFTER & RE-DRIVER



TO SOC MODULE CONNECTOR



TO HDMI
CONNECTOR

BPAGE DRAWING

gt96b.sch_1.17
Tue Mar 07 18:01:55 2017

HDMI: HDMI LEVEL SHIFTER

VARIANT:

N/A

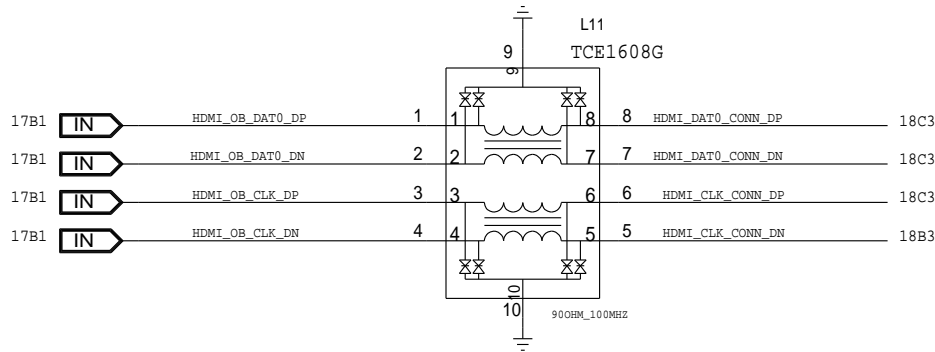
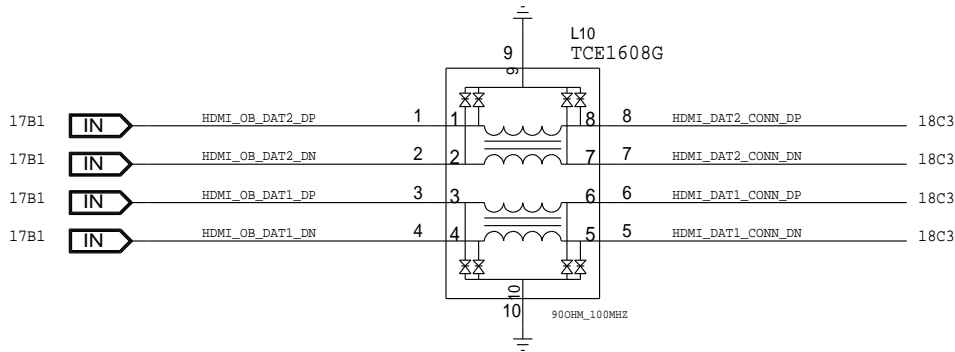
REV

1.20.00

PAGE

17/24

HDMI EMI FILTERING



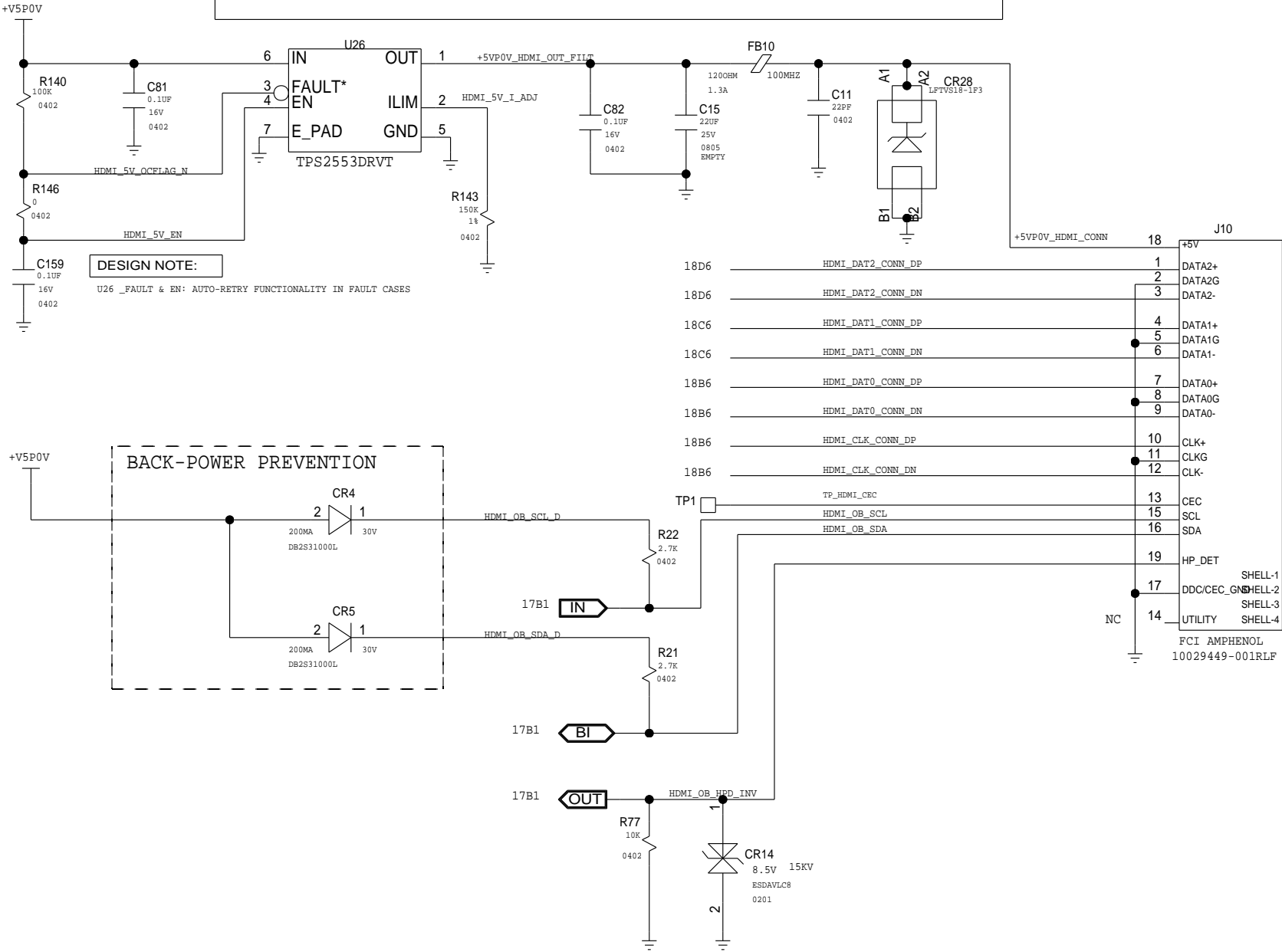
HDMI TYPE-A CONNECTOR

DESIGN NOTE:

U26 TO LIMIT OUTPUT CURRENT, FOR BACK-POWER PREVENTION,
AND TO KEEP OUTPUT VOLTAGE MIN. LEVEL WITHIN HDMI SPEC.

DESIGN NOTE:

ISET -> 150K TO KEEP HDMI OUTPUT CURRENT BELOW 210MA



BPAGE DRAWING

gt96b.sch_1.18
Thu Mar 09 09:48:07 2017

HDMI: HDMI TYPE-A CONNECTOR

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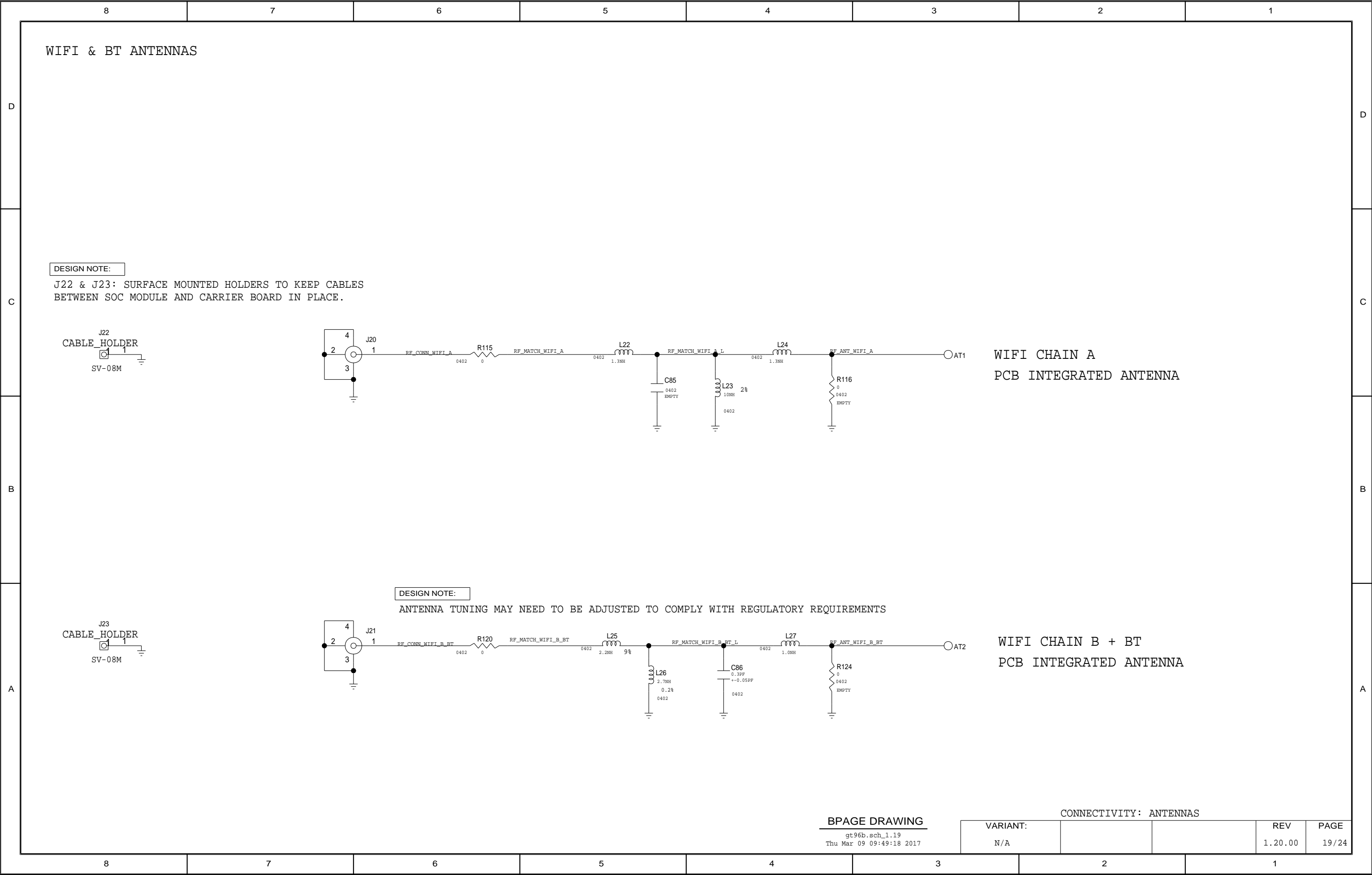
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REV

1.20.00

PAGE

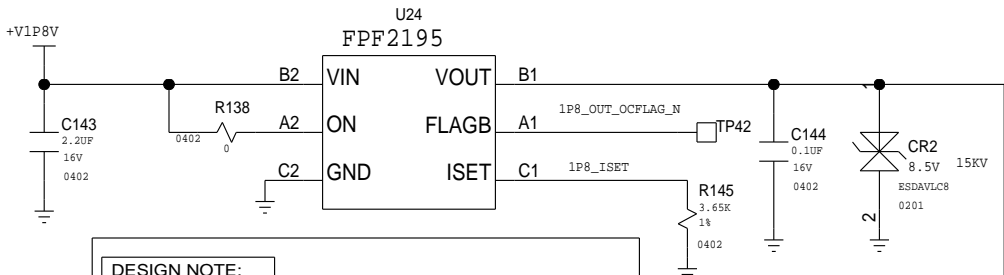
18/24



40PIN BREAKOUT CONNECTOR

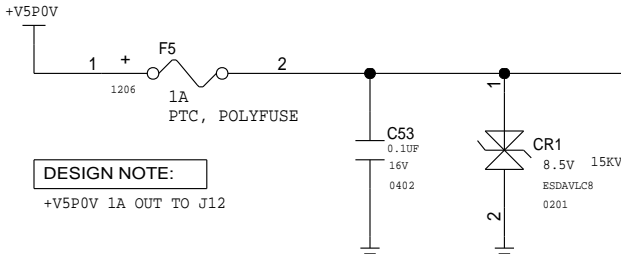
DESIGN NOTE:

USE U24 CURRENT LIMITING LOAD SWITCH INSTEAD OF RESETTABLE FUSE
DUE TO HIGH RESISTANCE OF LOW CURRENT RESETTABLE FUSE



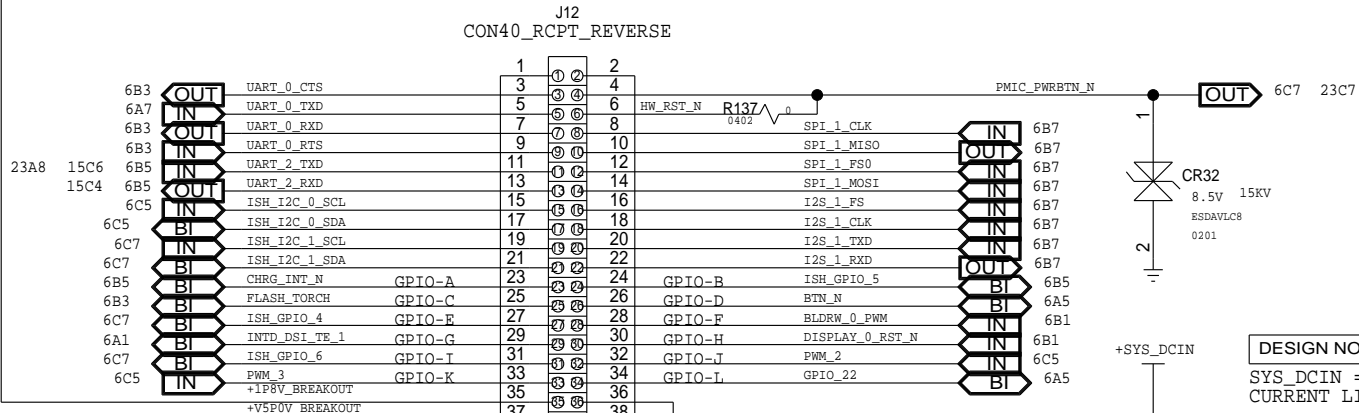
DESIGN NOTE:

ISET -> 3.65K = CURRENT LIMIT TO 115...190MA



DESIGN NOTE:

+V5P0V 1A OUT TO J12



DESIGN NOTE:

SYS_DCIN = 8...24V IN/OUT TO J12
CURRENT LIMIT BY 6A FUSE NEXT TO DC-JACK

IT'S RECOMMENDED TO HAVE SUPPLY INPUT CONNECTED
ONLY TO EITHER J4 OR TO SYS_DCIN (J12 PINS 36 & 38).
DO NOT CONNECT DCIN POWER SUPPLY INPUT TO BOTH
J4 & J12 AT THE SAME TIME.

DESIGN NOTE:

OPTION TO USE ALTERNATE FOR J12: TLE-120-01-G-DV-A TO FCI 55510-140LF, BASED ON AVAILABILITY

DESIGN NOTE:

SOC STRAPS, STATE AT RISING EDGE OF PMIC_PWRGOOD:
- UART_0_TXD (PIN-5) MUST BE HIGH-Z OR PULLED TO GND
- UART_2_TXD (PIN-11) LOW = DEFAULT, NORMAL BOOT
HIGH = FORCE DNX, LOAD FW FROM USB MEM.DEVICE

DESIGN NOTE:

GPIO A...L DEFAULT BIOS SETTINGS:

- GPIO-A: INPUT, WAKE CAPABLE INTERRUPT
- GPIO-B: OUTPUT, HIGH, NO INTERNAL PULL-UP, NO INTERNAL PULL-DOWN
- GPIO-C: OUTPUT, LOW, INTERNAL 20K PULL-UP
- GPIO-D: INPUT, LEVEL SENSITIVE INTERRUPT, ACTIVE LOW
- GPIO-E: OUTPUT, HIGH, NO INTERNAL PULL-UP, NO INTERNAL PULL-DOWN
- GPIO-F: OUTPUT, LOW, 20K PULL-DOWN
- GPIO-G: INPUT, 20K PULL-DOWN
- GPIO-H: OUTPUT, LOW, 20K PULL-DOWN
- GPIO-I: OUTPUT, HIGH, NO INTERNAL PULL-UP, NO INTERNAL PULL-DOWN
- GPIO-J: OUTPUT, LOW, 20K PULL-DOWN
- GPIO-K: OUTPUT, LOW, 20K PULL-DOWN
- GPIO-L: INPUT, EDGE SENSITIVE INTERRUPT, 20K PULL-UP

BPAGE DRAWING

gt96b.sch_1.20
Thu Mar 09 15:00:38 2017

I/O: 40-PIN BREAKOUT CONNECTOR

VARIANT:

N/A

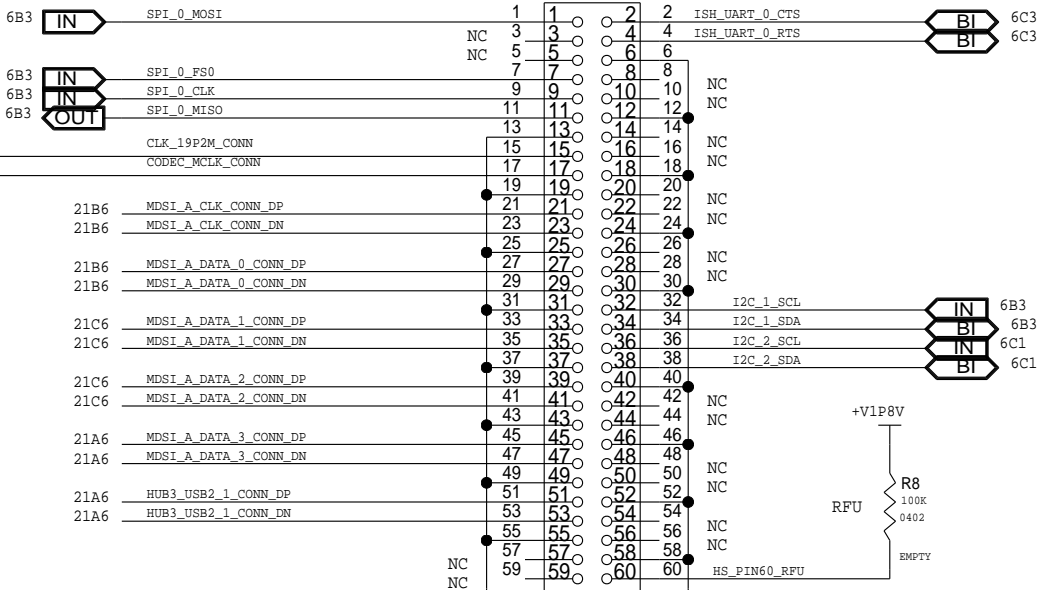
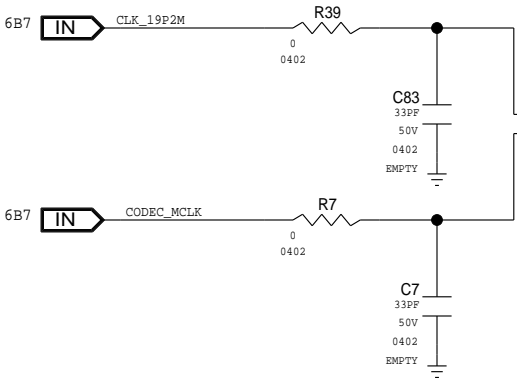
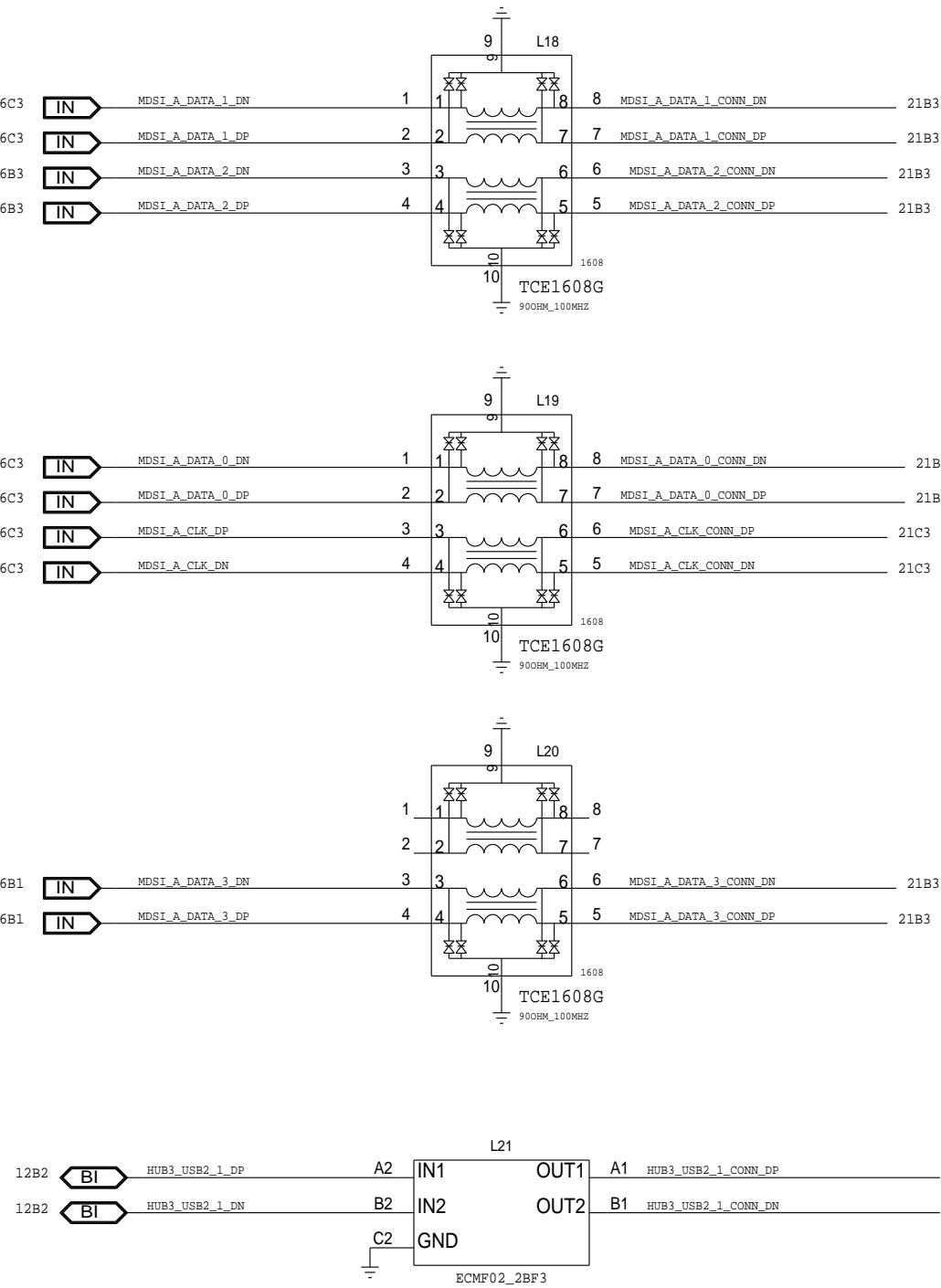
REV

1.20.00

PAGE

20/24

60PIN BREAKOUT CONNECTOR



DESIGN NOTE:

ISH_UART_0_CTS AND _RTS DEFAULT BIOS SETTINGS:
INPUT, 20K INTERNAL PULL-DOWN

TE CONNECTIVITY
5177985-2

DESIGN NOTE:

OPTION TO USE ALTERNATE FOR J13: FCI 61082-061409LF

BPAGE DRAWING

gt96b.sch_1.21
Wed Mar 08 16:18:05 2017

I/O: 60-PIN BREAKOUT CONNECTOR

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N/A

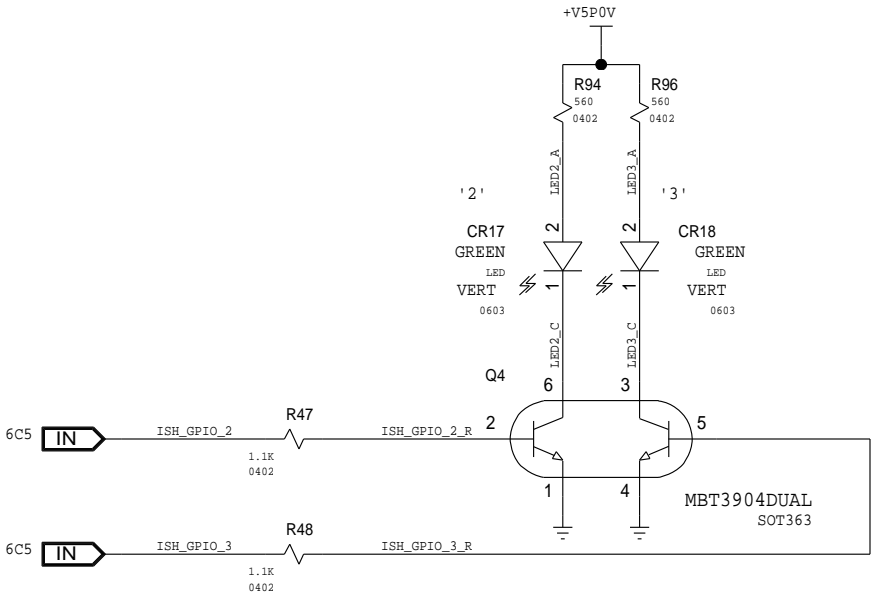
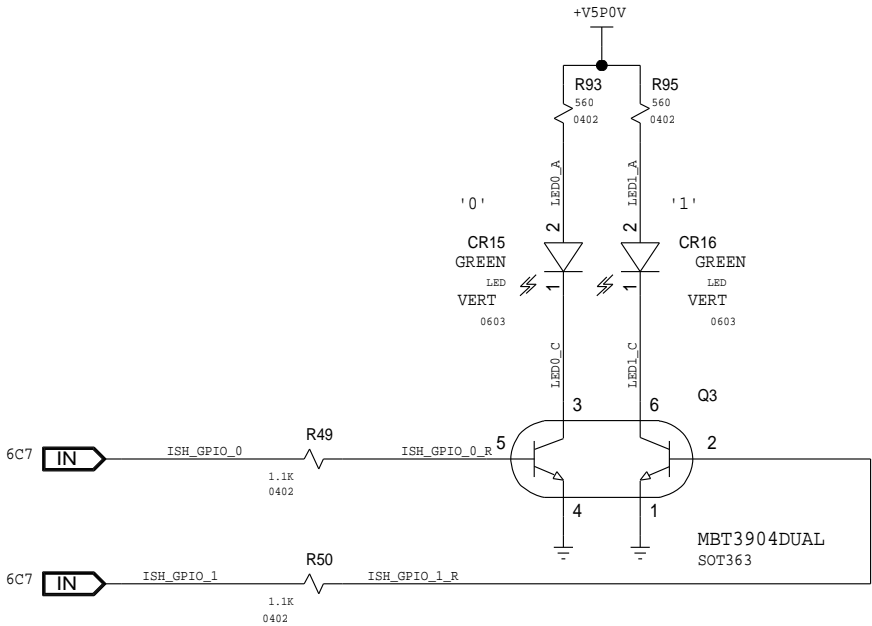
REV

1.20.00

PAGE

21 / 24

USER INTERFACE, GPIO LEDS



CAD NOTE:

PLACE CR15-CR18 TOP SIDE, BETWEEN J6 & J8 USB TYPE-A CONNECTORS

CAD NOTE:

SILKSCREEN: 'USER LEDS' AND '0', '1', '2', '3' NEAR
CR15, CR17, CR16, CR18, RESPECTIVELY

BPAGE DRAWING

gt96b.sch_1.22
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I/O: LEDS

VARIANT:

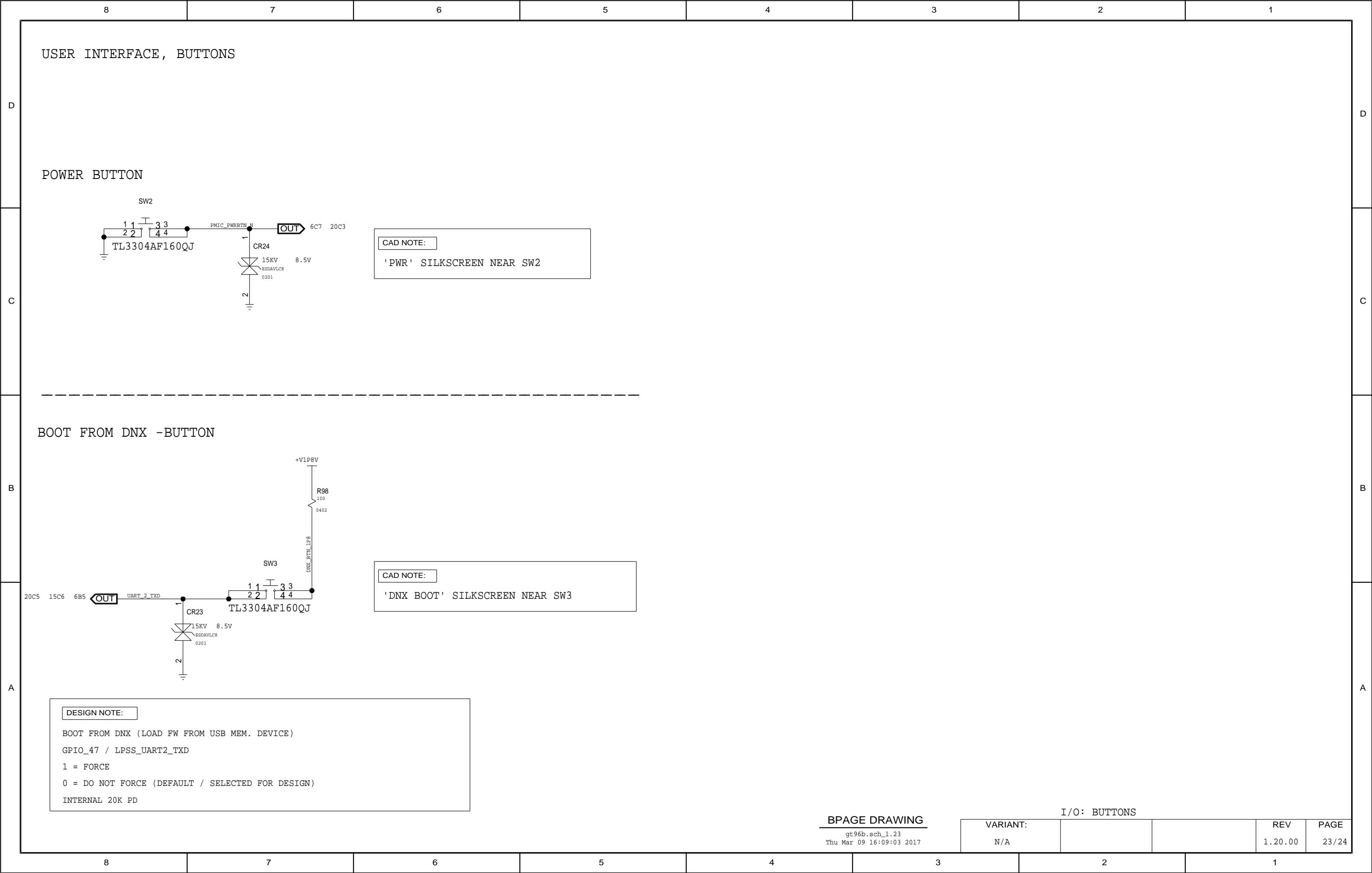
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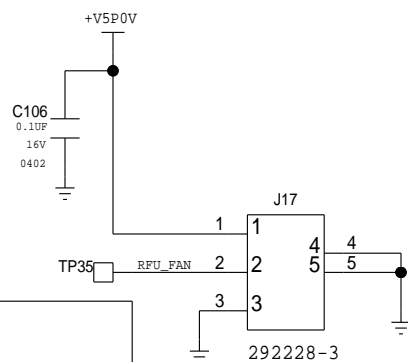
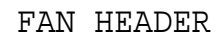
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PAGE

22 / 24



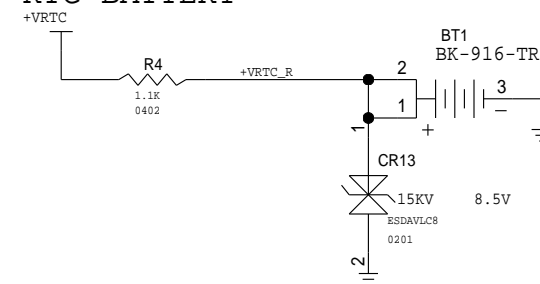


DESIGN NOTE:

5V FAN - NO SPEED CONTROL
SUNON
MB40100V2-000U-A99

CAD NOTE:

'FAN HEADER' SILKSCREEN NEAR J17.



DESIGN NOTE:

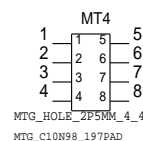
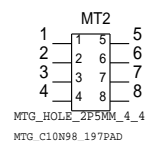
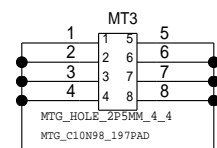
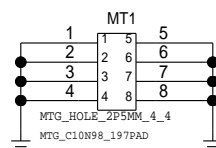
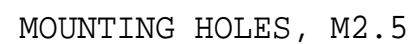
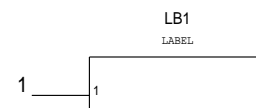
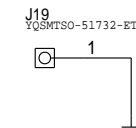
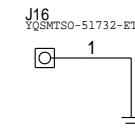
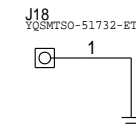
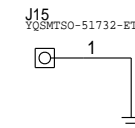
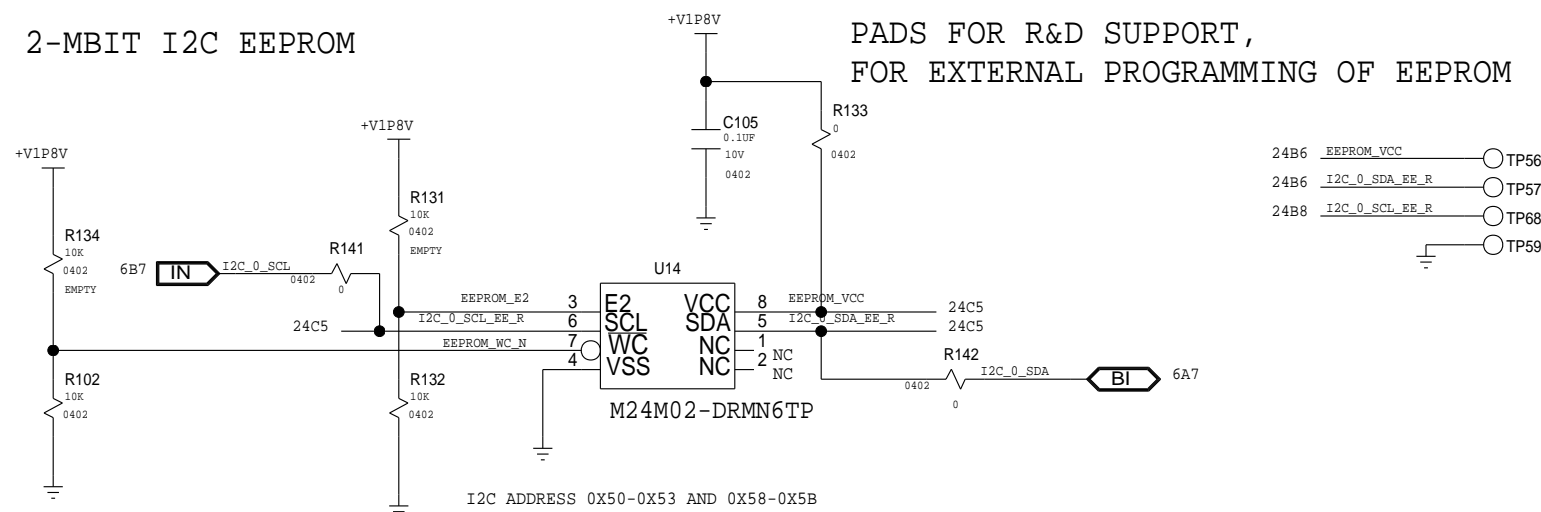
RTC BATTERY CIRCUITRY BT1, R4, CR13 ARE OPTIONAL
AND THEY CAN BE REMOVED IF RTC BATTERY IS NOT NEEDED.

CAD NOTE:

'RTC BATTERY' SILKSCREEN NEAR BT1

DESIGN NOTE:

FOR USE WITH 3V, 12MM COIN CELL BATT. HOLDER



DESIGN NOTE:

MT2 AND MT4 FLOATING, NOT CONNECTED, DUE TO LOCATION NEXT TO ANTENNAS

BPAGE DRAWING

gt96b.sch_1.24
Thu Mar 09 16:10:28 2017

MISC: EEPROM, FAN, RTC BATTERY

VARIANT:

N/A

REV

1.20.00

PAGE

24 / 24